

**TOWARDS HIGH EFFICIENCY
AND LOW COST
NANO-STRUCTURED
III-V SOLAR CELLS**

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Abstract

State-of-the-art III-V multijunction solar cells have achieved a record efficiency of 42%, the highest solar-electric conversion efficiency achieved by any technology. This has fueled great interest in the utility sector for large-scale deployment of solar cells. However, III-V solar cells have thus far proven too expensive for widespread terrestrial applications due to the combined cost of substrates, growth processes and materials. Here, we propose a novel III-V solar cell design based on the epitaxial growth of AlGaAs/GaAs on pre-patterned low-cost substrates to provide a path to cost-effective, large-scale deployment. This approach is based on our discovery that the surface kinetics of epitaxial growth by MBE is significantly altered when growing on three dimensional nanostructures instead of planar surfaces.

Based on our exploratory results, we present the device design, electrical and optical simulation, and materials growth and device fabrication and characterization of core-shell nanostructured III-V solar cells. We use both bottom-up and top-down approaches to prepare the nanostructured templates in shape of nanowires and nanopyramids. Finite-difference time-domain (FDTD) and Rigorous Coupled Wave Analysis (RCWA) simulation show that the nanostructures have enhanced absorption and much wider

incident acceptance angles than their planar counterpart, and outperform planar three-layer anti-reflective coatings. We first demonstrated high quality, single crystal III-V (GaAs and AlGaAs) polar material conformally epi grown on group IV (nanostructured Ge on Si substrate) nonpolar material via MBE and MOVPE (or MOCVD) with largely reduced anti-phase domains. We developed complete and mature routines to fabricate a working, single crystalline III-V solar cell on a nanostructured template. The I-V characterization of the fabricated nanostructured GaAs solar cell proves the concept and shows the great potential of making high-efficiency nano-structured III-V solar cells on low-cost substrates.

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Chapter 1 Introduction

1.1 Motivation

1.1.1 World Energy Challenge

Today, the world is in need of greater alternative energy sources than ever before. As of 2010, the world population is 6.9 billion and consumes 30 Terawatts power. By 2050, the population is projected to be over 10 billion and 60 Terawatts power will be consumed [1]. The burning of fossil fuels for energy production is still by far the largest source. However, those nonrenewable energy forms are not sustainable. Predictably, a considerable gap between energy demand and supply of nonrenewable energy will take place around 2020, as illustrated in Figure 1.1. [2]

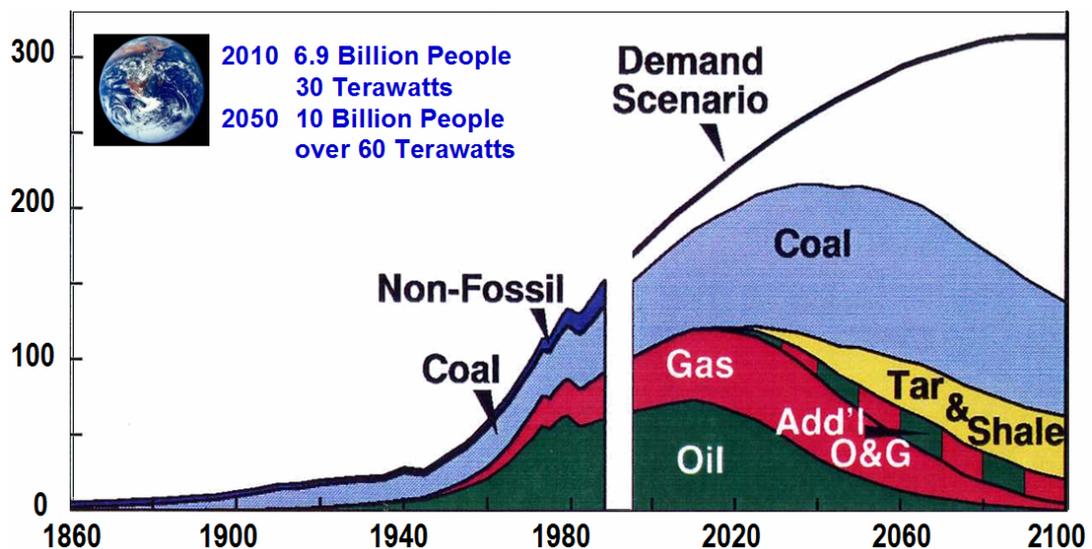


Figure 1.1. Millions of barrels per day (oil equivalent) consumed by the world population. Adapted from [2] and Professor James S. Harris's lecture notes [3].

Figure 1.1 shows millions of barrels per day (oil equivalent) consumed by the world population. We see the clear trend of world energy demand increasing rapidly, while the sum of all nonrenewable energy sources, such as coal, gas, oil, tar and shale start to decline around the year 2050 [2].

1.1.2 Solar Energy and Solar Cells

Among all the forms of renewable energy, solar cells are the only candidate that is likely to provide a significant fraction of our future power. 165,000 Terawatts of sunlight hit the Earth, thus we only need to convert 0.025% of the incident solar energy to feed the global energy demand today [4]. Table 1.1.2 shows the total solar energy, wind, biomass and human energy consumption for the year of 2005 [5]. The total solar energy absorbed by Earth's atmosphere, oceans and land masses is approximately 3,850,000 exajoules (or EJ, 1 EJ = 10^{18} J) per year [6], see Table 1.1.2 below. The absorbed solar energy by Earth in one hour is enough for the world to use in one year (data in 2005) [11].

Table 1.1.2 Solar energy and other renewable energy forms

Yearly Solar Fluxes, Wind, Biomass & Human Energy Consumption	
Solar	3,850,000 EJ [6]
Wind	2,250 EJ [7]
Biomass	3,000 EJ [8]
Primary energy use (2005)	487 EJ [9]
Electricity (2005)	56.7 EJ [10]

Solar cells are safe and have no undesirable environmental impacts. Using solar cells

instead of burning coal to generate electricity is a much easier way to reduce carbon emissions than replacing gasoline in vehicles. Practically, solar cells provide electricity exactly when we need it the most (on hot sunny days when people run their air conditioners) [12].

More importantly, solar cells appear to be the best remedy to reduce carbon dioxide and other “green house” gas emissions into the atmosphere. The current levels of carbon dioxide in the atmosphere hit the historical records [13]. Petit, J.R., et al reported the recent evidence in Nature 1999 that carbon dioxide concentration in the atmosphere and the mean temperature for the past half a million years has a strong correlation [13].

According to Reference [14], an article in Nature (1998) [14], M. I. Hoffert pointed out that we need at least 50 TW of carbon-free power production by 2050 to stabilize the carbon concentration in the atmosphere. The Lewis research group at California Institute of Technology reported that solar energy is the only form of energy abundant enough to meet the world’s energy requirements in the next half century after a systematic analysis of all currently available renewable power (including solar, wind, geothermal, and biomass, etc.) [15].

Therefore, our nanostructured solar cell research fits in this global theme of “renewable energy”. To be specific, we are aiming to significantly improve solar cell efficiency and reduce the cost.

1.2 Solar Cell Efficiency

Efficiency is one of the most important figures of merit for solar cells. Figure 1.1 shows the best research-cell efficiencies from the year 1976 to 2010[16].

There are four categories of solar cells indicated by different colors in the plot: Multijunction III-V (GaAs, Ge/GaAs/InGaP, etc.) Solar Cell, Crystalline Si Cells, Thin-Film Technologies, Emerging PV. Table 1.2 summarizes general categories of solar cell technologies.

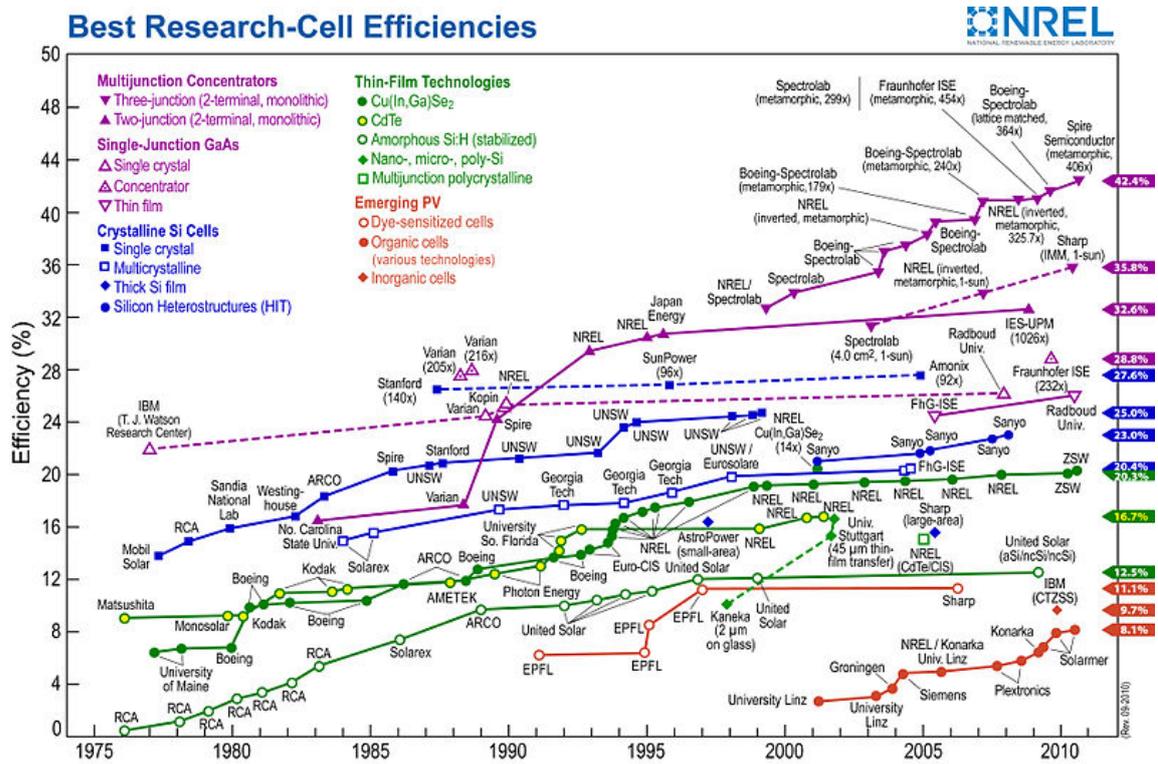


Figure 1.2 NREL Compilation of Best Research Solar Cell Efficiencies [16]

Table 1.2 General Categories of Solar Cell Technologies

Silicon	Monocrystalline or single crystalline silicon (mono-Si sc-Si); Poly- or multicrystalline silicon (poly-Si or mc-Si):
----------------	---

	Ribbon silicon
Thin Films	Amorphous Si (a-Si) CdTe (Cadmium Telluride) CIGS (Copper-Indium Gallium Selenide)
III-V Solar Cell	Single-junction GaAs Multi-junction (Ge/GaAs/InGaP) Concentrating Photovoltaics, CPV)
Other Emerging PV	Nano-crystalline and Nano-structured Solar Cells New Concepts (MEG, Multi-Exciton-Generation) DSSC (Dye-Sensitized Solar Cell) Organic/Polymer Solar Cells

Notably, multijunction III-V solar cells dominate the highest efficiency records for most of this period. However, when it comes to cost, multijunction III-V solar cells are the most expensive among all of the solar cell categories.

1.3 Cost-efficiency Map and Generations of Solar Cells

Cost is the other most important figure of merit for solar cells. It is critical to put efficiency and cost together to compare different solar cell technologies. Figure 1.1.4 shows efficiency vs. cost mapping for different generations of solar cells.

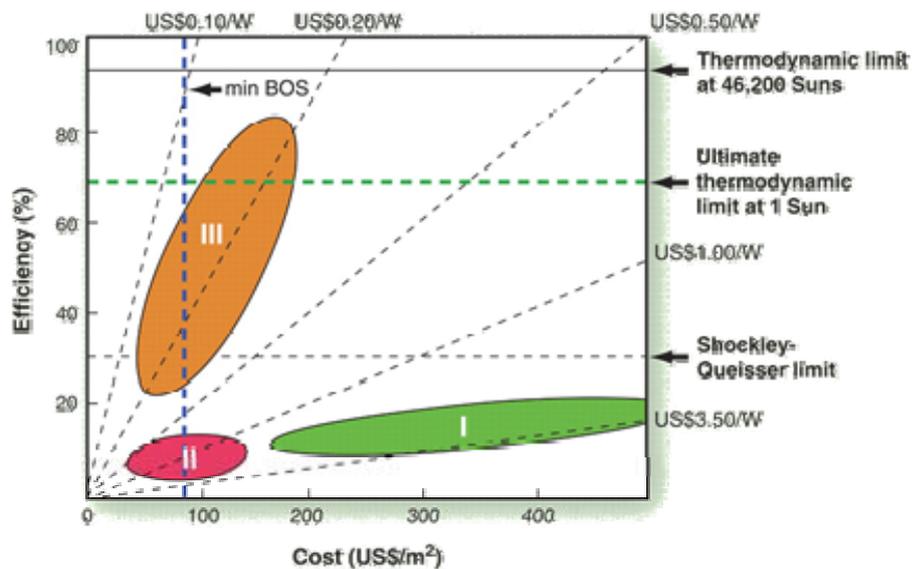


Figure 1.3 Cost - efficiency map for different generation solar cells [17], adapted from M.A Green,

2004 [17]. I, II, III, denotes the Generation I, Generation II, Generation III solar cell.

The terms “generations of solar cell” was coined by Dr. M. A. Green [17]. Although it is not entirely an official definition, it is widely cited. Table 1.3 summarizes the 3 generations of solar cells.

Table 1.3 Solar Cell Generations

1st Generation	Crystalline Silicon: medium efficiency but moderately high cost
2nd Generation	Thin-film: less material, cheaper substrate, less expensive manufacturing equipment; overall low cost but low efficiency.
3rd Generation	Still a vibrant research effort up to now: advanced concepts and material, new physics mechanism and breakthrough. Overall high efficiency with no compromise on low cost. Still an active research area.

1.3.1 The First Generation

First generation solar cells are the larger, silicon-based, photovoltaic cells that have, and still do, dominate the solar panel market. These solar cells, using silicon wafers, account for 86% of the solar cell market. They are dominant due to their high efficiency, but their manufacturing costs are high, which is a problem that second generation cells hope to remedy. Figure 1.3.1 shows the first generation solar cell. (a) is a schematic of a solar cell structure and illustrates how power is extracted from the cell with illumination of sun light. (b) is a photograph of a silicon solar cell module. (c) is the Passivated Emitter Rear Locally Diffused (PERL) solar cell developed at UNSW and

holds the world record for high efficiency in Silicon solar cells [18].

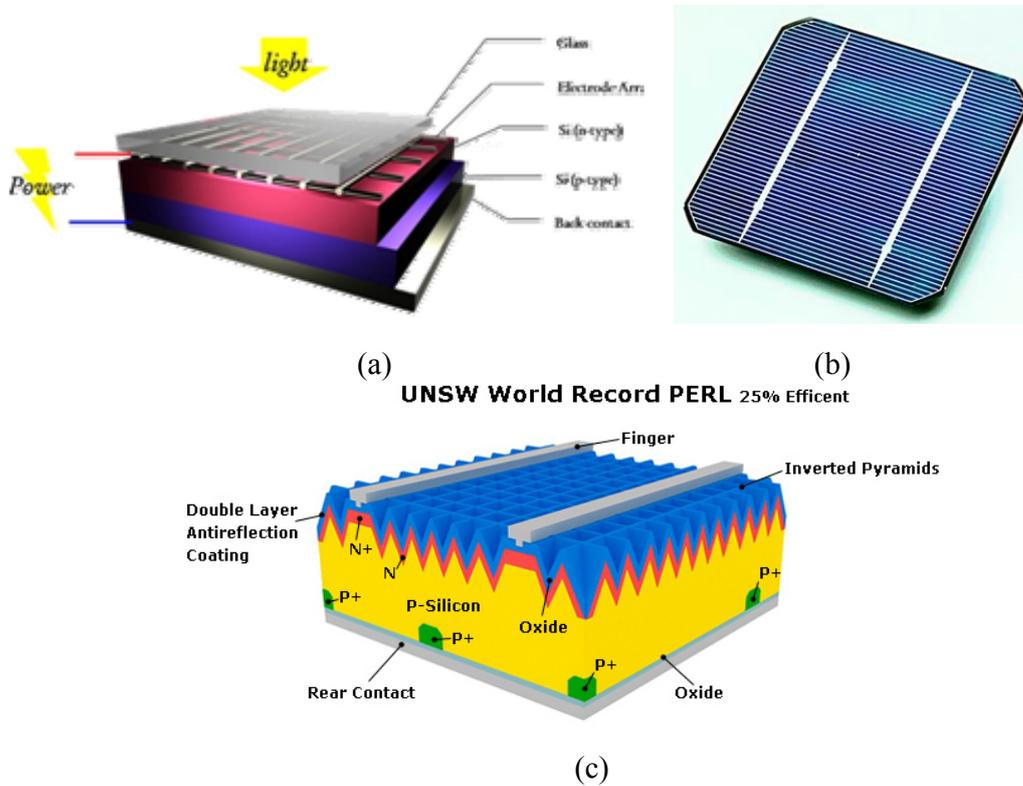


Figure 1.3.1. First generation solar cell. (a) Schematics of a solar cell structure (b) A photograph of a silicon solar cell. (c) The Passivated Emitter Rear Locally Diffused (PERL) solar cell [18] illustrating the processing sophistication that has emerged over the last 40 years.

1.3.2 The Second Generation

Second generation cells, also called thin-film solar cells, are significantly cheaper to produce than first generation cells but have lower efficiencies. Lower cost manufacturing methods are employed and less material and less expensive substrates are used. They have potential to be flexible and integrated directly into roofing material.

However, the major limitation is their lower efficiencies. For example, below is a list of typical thin-film solar cells and their production and best efficiencies:

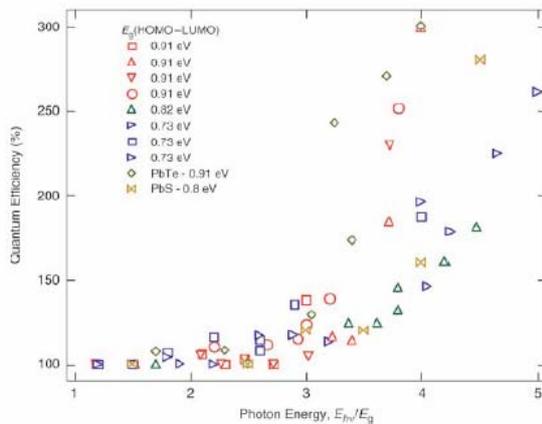
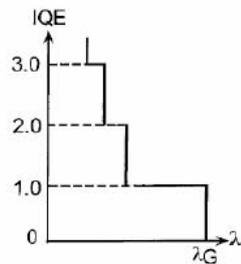
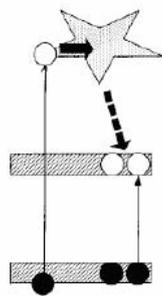
Table 1.3.2 list of typical thin-film solar cells

CIGS (CuInGaSe₂)	World record: 19.5 % Production: 9%-11%
amorphous Si	World record: 13.2 % not completely stable Production: 6-8%
CdTe	World record: 16.5 % Production: 8%-10%

1.3.3 The Third Generation

Third generation solar cells are the cutting edge of solar technology. Still being in the research phase, third generation cells have moved well beyond silicon-based cells which contain a wide range of potential solar innovations including polymer solar cells, nano-crystalline cells, multi-exciton generation (MEG) solar cells, etc.

Figure 1.3.3 shows a schematic of the MEG process in some material system under certain conditions. The MEG literally means one incident photon can excite more than one electron-hole pair. In this case, the quantum efficiency is larger than 100%! [19]



A limiting efficiency of 85.4% has been calculated

Nano Lett. 5 p. 865, 2005

J. Am. Chem. Soc. 128 p. 3241, 2006

Phys. Rev. Lett. 92 186601, 2004

Figure 1.3.3. An example of new physical mechanism which might lead to a third generation solar cell: Multi Exciton Generation (MEG) [19]

1.4 III-V Multijunction Solar Cells

III-V multijunction solar cells are the unchallenged world record holder for high efficiency photovoltaics among all the solar cell technologies mentioned above and beyond. State-of-the-art III-V multijunction solar cells have achieved a record efficiency of 42% [20][21][22], the highest solar-electric conversion efficiency achieved by any technology. This high-efficiency largely thanks to the bandgap tunability of the III-V materials systems, namely, the III-V materials can be epitaxially grown on lattice matched substrates with very low crystal defect density and the lattice parameter can be controlled by varying the stoichiometry of binary (ternary or quaternary) systems which

result in different band gaps at the same time [23]. In this way, more than one p-n junction can be serially epitaxially grown on top of the next (forming a tandem), each one absorbing a different certain portion of the solar spectrum. Therefore, the tandem multiple p-n junctions can harness the solar spectrum more efficiently than a single junction does. [23]

Figure 1.4.1 illustrates the bandgap energy vs. lattice constant for most III-V (and II-V) compound semiconductors [24]. In the line Ge - GaAs - AlAs, the lattice constants are similar, and the line GaP - InP has an intersession with the line Ge - GaAs - AlAs. This feature can be used for Ge/GaAs/InGaP and Ge/GaInAs/GaInP multijunction solar cells.

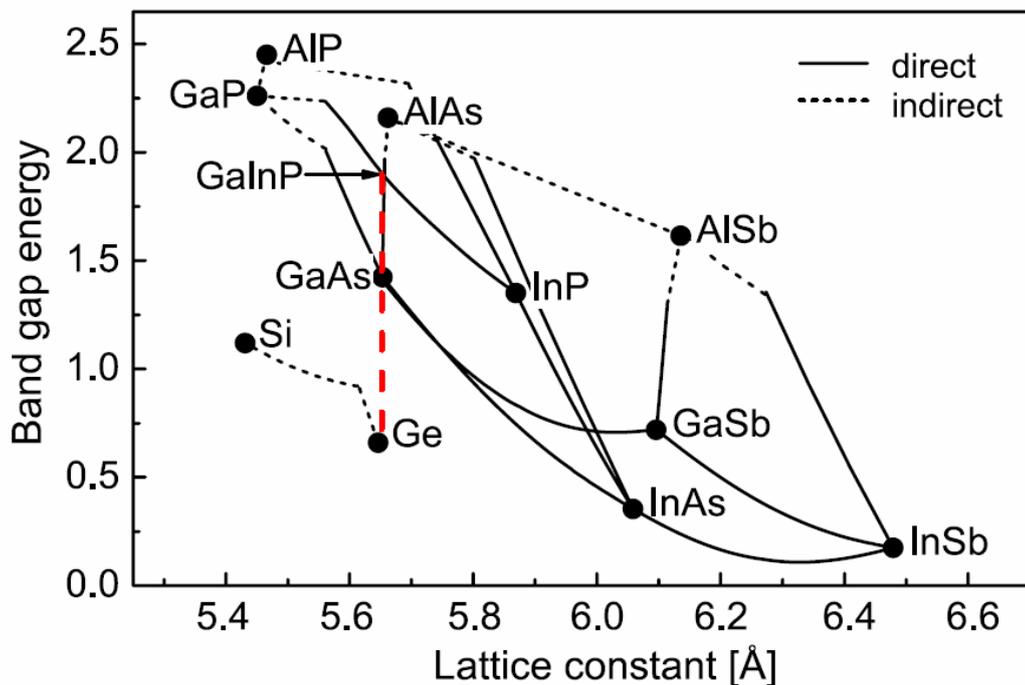


Figure 1.4.1 Band gap of most group III-V and IV semiconducting materials versus their lattice

constant. Materials with matched lattice constant, such as, Ge-GaAs-GaInP are such a combination and they have produced the record solar cell efficiency. [24]

As shown in Figure 1.4.2, the single-junction solar cell can only absorb a certain portion of solar spectrum with $\lambda < E_g$, E_g is the energy band gap of the solar cell active absorption material. In the case of silicon, the maximum theoretical efficiency is only 28% (Figure 1.4.2 a) [25], while for a multi-junction cell (Figure 1.4.2 b), each junction with different energy band gap can absorb different portion of the solar spectrum, thus the maximum theoretical efficiency can be 86.8% [25] much higher than the best case of single junction!

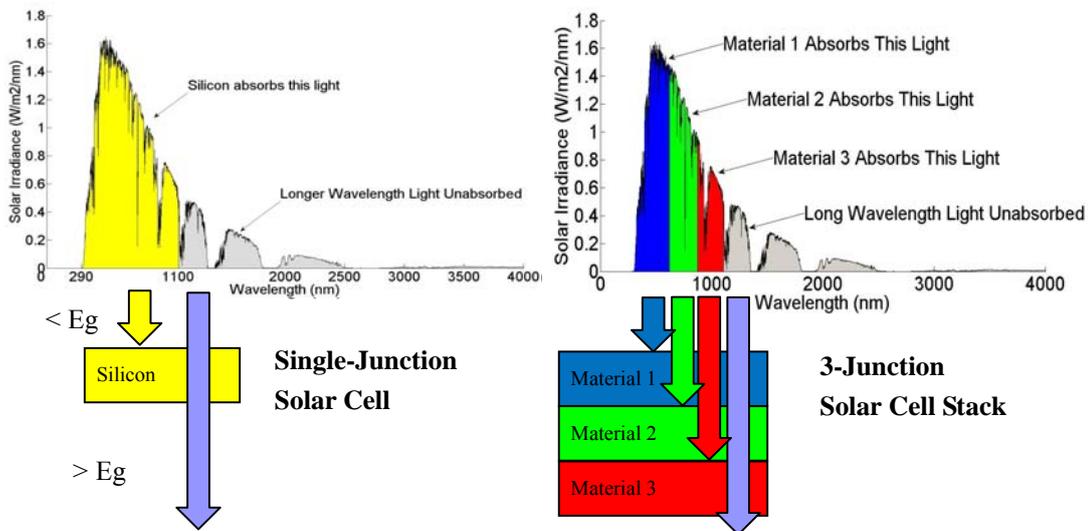


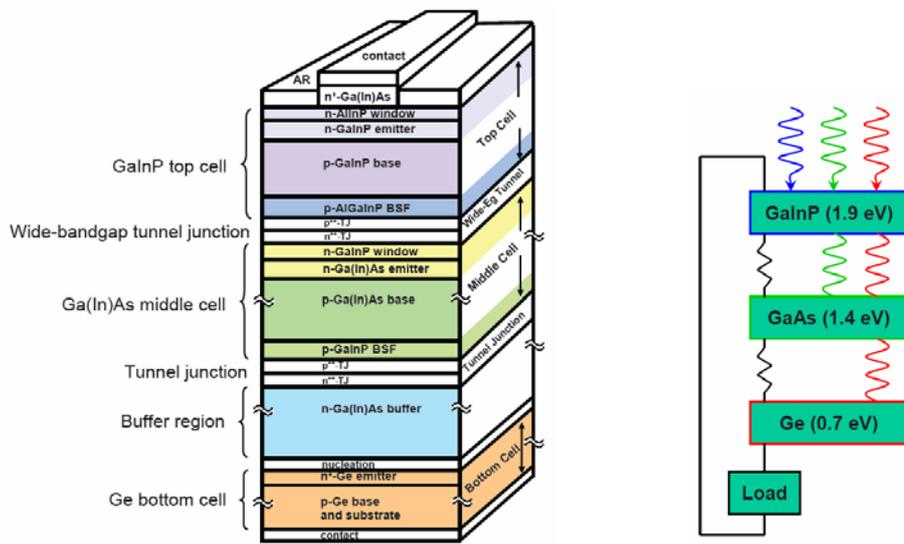
Figure 1.4.2 Light absorption for (a) Single-junction solar; (b) Multijunction solar cell

1.5 State-of-the-Art III-V Solar Cell

The current world record efficiency solar cell is a triple-junction device fabricated on a germanium substrate, and has power conversion efficiency of 42% at approximately

500-suns concentration [22,26]. The middle gap is composed of InGaAs with 1% indium to better lattice match to the germanium bottom junction, and the top junction is composed of InGaP. The bandgap combination for this cell is roughly 0.6, 1.4, and 1.9 eV. In an attempt to achieve more ideal bandgap combinations, many researchers have been investigating metamorphic compositions of InGaAs and InGaP on Ge [27]. Law, et al. reported in 2005, that 26.6% efficiency was possible with a dual-junction metamorphic InGaAs/InGaP solar cell (with 1.6% lattice-mismatch between films and substrate) [28]. The bandgap combination of this cell was 1.1 eV and 1.65 eV, very close to the ideal dual-junction combination. [27]

Practically, Dr. Richard R. King and his team at SpectraLab have achieved over 40% solar-electric conversion efficiency [22]. The triple junction solar cell structure is illustrated in Figure 1.5 (a).



(a)

(b)



(c)



(d)

Figure 1.5 (a) Schematics of the structure of the state-of-art triple junction solar cell. (b) Schematics of different portions of the solar spectrum being absorbed in each junction of the multijunction solar cell. (c) The application of multijunction solar cell in space. (d) The application of multijunction solar cell in solar utility station.[29]

1.6 Our Proposal

Figure 1.5(a) or similar structure represents the state-of-the-art III-V multijunction solar cells that have achieved world record efficiencies. This has fueled great interest in the utility sector for large-scale deployment of solar cells. However, III-V solar cells have thus far proven too expensive for widespread terrestrial applications due to the combined cost of (1) Latticed-matched single crystal substrates (Ge, or III-V); (2) III-V materials and manufacturing process; (3) concentrator and 2-axis sun tracking system, etc. Figure 1.6 shows the position of III-V multijunction solar cell in the map of cost-efficiency of three generations of solar cell. It is on the far right of the X-axis and top of the Y-axis which mentions the high efficiency but extremely high cost, the “dual property” of the III-V multijunction solar cell.

Stepping away from conventional III-V technology, we propose a novel type of high efficiency, single crystal, thin film, III-V multijunction solar cell based on epitaxial growth on nanostructures on low-cost substrates to provide a path to high efficiency and low cost for large-scale deployment. We look at the each cost component of the III-V solar cell system, e.g., the cost of substrate, III-V material used in the growth process, concentrator and 2-axis sun tracking system, and try to reduce the cost accordingly. Our goal is to move the point A (high-efficiency and high-cost) of existing multijunction cell to the point B (high-efficiency and low-cost) in the classic cost-efficiency map of solar cells.

This approach is based on our discovery that the surface kinetics of epitaxial growth by MBE are significantly altered when growing on three dimensional nanostructures instead of planar surfaces. These growth kinetics enable uniform, single crystal growth of low-defect, lattice mismatched materials on nanostructures with high aspect ratios [30].

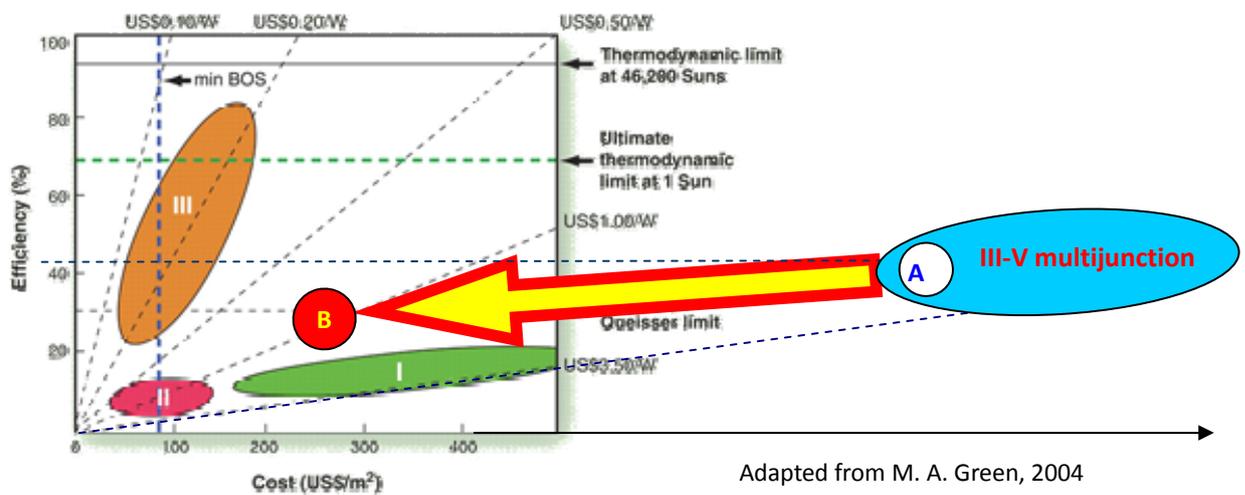


Figure 1.6 Multijunction solar cell's position in the classic cost-efficiency map. The current III-V multijunction solar cell is far out on the right of the x-axis in this map and the only means it has to be cost competitive is with high solar concentration.

Table 1.6 compares the conventional III-V multijunction solar cell and our proposed nano-structured III-V multijunction solar cell, and how we achieve these advantages.

Table 1.6 Comparison Table of conventional III-V cell and proposed cell

Conventional III-V multijunction solar cell	Proposed nano-structured III-V multijunction solar cell
Manufacture cost: Reduced	
Expensive single-crystal Ge or III-V substrate	Si or flexible low-cost substrates with nano-structured templates
Expensive thick layers (absorber and buffer) of III-V compound material	Nanostructure to thin absorption layers; reduce thickness of buffer layer
Expensive multi-layer anti-reflection coating	Light trapping to eliminate the need of anti-reflection coating
System and installation cost: Reduced	
Heavy, bulk, need concentrators and 2 axis sun-tracking systems	Light-weighted, potentially flexible, wide acceptance angle, no sun-tracking
High-efficiency: Retained	
Multiple junctions for aboard spectrum absorption, but the number of junctions limited by lattice mismatch problems	New conditions for lattice mismatched material growth; III-V nano materials, favorable for multijunction configuration

1.7 Dissertation Overview

Chapter 1 gives a high-level introduction of research motivation, solar energy and solar cell, cost-efficiency map and generations of solar cells, cost problems in III-V multijunction solar cell, our new discoveries and our proposal to address these problems

of III-V.

Chapter 2 surveys a general background about solar cell technology, the definition of solar cell terminology, nanotechnology and its application in solar cell (including amorphous Si case and CdTe case), core-shell structure, and our enabling factors and possible extra benefits for multijunction cells.

Chapter 3 presents the optoelectronic device design, nanostructure design and electrical simulation and optical Simulation (FDTD and RCWA) for the size dependence, spectral reflectance vs., angular dependence.

Chapter 4 reviews the details of nanostructure template preparation, bottom-up and top-down approaches as two strategies to produce nanostructure templates. First, for the bottom-up approach, we start with VLS (Vapor-Liquid-Solid) growth of nanowires and exhibit our nano-templates made by bottom-up approach. And we encountered problems with bottom-up approaches, for instance, the Au catalyst removal problem and density and uniformity problem associated with the nature of random process of VLS growth.

Then we found that the top-down approach is a better alternative. By adapting some innovative nano-sphere mask coating on semiconductor wafers (e.g. LB (Langmuir-Blodgett) process, spin coating or dip coating), we can use Reactive Ion Etching (RIE) and wet etching to fabricate various nanostructure with pitch, spacing,

shape, aspect ratio and orientation of facets being well tuned.

Chapter 5 highlights the material growth part of this project. We first review the fundamental of MBE (Molecular Beam Epitaxy) and the surface kinetics on 2-D substrates. Then we present the new condition and new dynamics of surface kinetics on 3-D nano-template substrates and showcase the MBE growth results of GaAs on 3-D nanostructure including nanowires and nano-pyramids.

In MBE growth, the growth rate is one of the most critical parameters. For the first time, we derived the equation of growth rate for nanowire structure and generalize to nano-cone or nano-pyramid.

In our project, MBE is an excellent tool for research and prototyping a prove-of-concept device, while MOVPE is widely used in industry for mass production. We have developed mature recipes for single-crystal GaAs overgrowth on nanowires; while for growth on nano-pyramids, it is a compromise to get both good conformality and good crystal quality. We have experimented and developed a two-step growth recipe for grow both good conformal and good single crystal GaAs on Ge nanopyramid and GaAs nano-pillars.

We also noticed the phenomena of anisotropic growth of GaAs on GaAs nano-template and found an explanation for it. And we compared the anti-phase domains in MBE vs. that in MOVPE.

In Chapter 6 we report the device fabrication and I-V characterization of our solar cell device. First, the contact is very important for nanostructured solar cells. We have tried ITO (Tin doped Indium Oxide), metal finger (pad) contact and nanowire transparent contact. For nanostructured solar cell devices, shorting and leaky problems are common phenomena. We use PMMA to create an insulation layer and etch the top tip region for contact and current collection, while the remaining layer is to isolate the metal contact from the active device region. And the final device fabrication procedure is listed.

Then we measure the I-V characteristics in dark and 1 Sun illumination using a solar simulator. We describe overcoming the shorting problem which always exists in nanostructured solar cells. Comparing a planar structure solar cell with same absorption thickness (200nm), the nanostructured III-V solar cell shows an overall increased efficiency and significantly increased short circuit current [31]. This is much better overall performance compared to the relevant literature [32].

As the first prove-of-concept device, there is more room to improve. We study the equivalent solar cell circuit and suggest the future work to improve the solar cell's fill factor, open circuit voltage and efficiency.

Chapter 7 summarizes the conclusion of the dissertation and the author's contribution.

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Chapter 2 Background

2.1 Solar Cell Technology Overview

2.1.1 Definition of Solar Cell and Photovoltaics

Solar Cells are a type of solid-state device that converts the energy of sunlight into electricity by the photovoltaic effect. Photovoltaics is a field of science and engineering developing practical applications of the photovoltaic effect to produce electricity from light or specifically refers to the generation of useful electrical power from sunlight.[1]

2.1.2 A Brief History

The photovoltaic effect was discovered in 1839 by French physicist A. E. Becquerel [2]. However, it was not until 1883 that the first solar cell was built, by Charles Fritts, who coated selenium with a thin layer of gold to form metal-semiconductor junctions. The efficiency of this simple-version solar cell device was only around 1% [3]. The modern solar cell was developed in 1954 at Bell Laboratories [4]. The first practical high-efficiency solar cell was developed by Daryl Chapin, Calvin Souther

Fuller and Gerald Pearson in 1954 using silicon p-n junctions formed by diffusing different types of dopants.[5]

At first, the cost of the equivalent electricity produced from the cells was very high. In the 50's and 60's solar cell devices were mainly used on satellites in space because of the special need for power in communications and surveillance satellites and space stations. During the energy crisis in the 1970's, solar cells began to be proposed as an alternative to fossil fuels for energy production on Earth [1]. In the past half century, tremendous improvement of the solar cell technologies has been achieved and numerous semiconductor materials have been used to create new types of solar cells, including amorphous-Si, CdTe, CuInGaSe, organic polymers and III-V compound materials [6].

2.1.3 The Physics of Solar Cells

The most commonly known solar cells are configured as P-N junctions made from various semiconductor materials. P-N junctions are elementary "building blocks" of most semiconductor electronic and optoelectronic devices, such as diodes, transistors, solar cells, photodetectors, LEDs, and integrated circuits. P-N junctions are the active region where the electronic or optoelectronic action of the device takes place [7] [8].

Figure 2.1.3 shows a schematic of the band diagram of a P-N junction with light illumination.

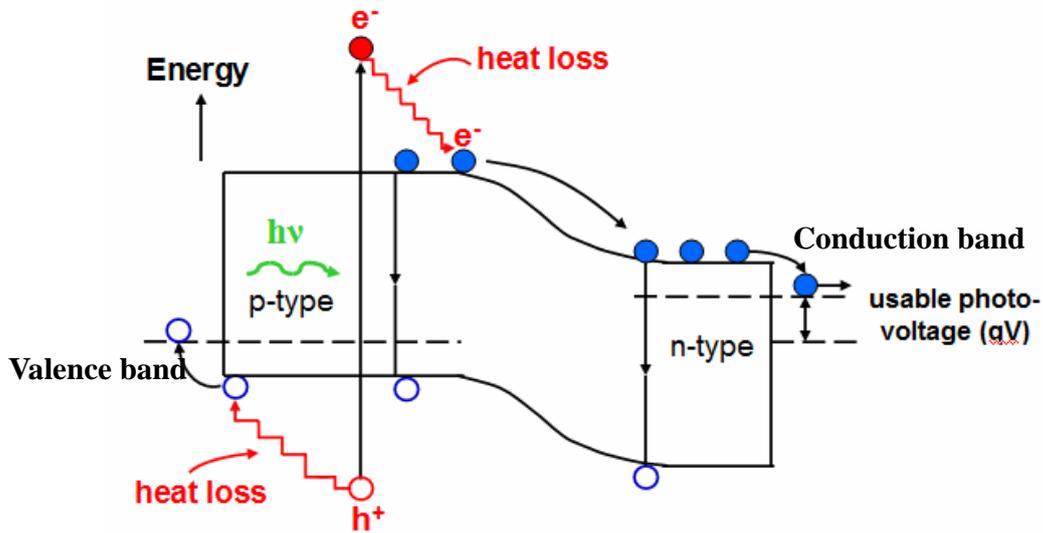


Figure 2.1.3 Band diagram of a P-N junction under illumination [8]

When a photon is incident on a semiconductor material, it can either [8][9]:

- (A) reflect off the surface;
- (B) pass straight through the semiconductor if its photon energy is lower than the bandgap energy of the semiconductor;
- (C) be absorbed by the semiconductor material, if the photon energy is higher than the bandgap energy of the semiconductor and create an electron-hole pair. [9]

Solar cells utilize the (C) scenario. In this way, it generates an electron-hole pair and the difference of photo energy and bandgap energy is dissipated as heat.

When a photon is absorbed, its energy is transferred to an electron in the crystal lattice where “valence band” and “conduction band” are mathematical abstractions of the allowed energy states for electrons [8][13]. The characteristic of the valence band in semiconductors is that before absorbing the photon, the electron was in the valence band

and tightly bound in covalent bonds between conjunctural atoms, and therefore not mobile. After illumination, the energy is given to the electron by the photon, which "excites" it into the conduction band [8][13], where it is free to move around within the semiconductor. Therefore, the covalent bond by which the electron was previously bonded now has one "missing" electron, which is mathematically abstracted as a "hole". The presence of a missing covalent bond allows the bonded electrons of neighboring atoms to move into the hole, leaving another hole behind, and in this way a hole can propagate along the lattice. Thus, it can be said that photons absorbed in the semiconductor create free electron-hole pairs. [8][9][10]

A photon need only have greater energy than that of the band gap of the absorbing semiconductor in order to excite an electron from the valence band into the conduction band. The spectrum of the solar radiation is close to that of a black body with a temperature of about 5,800 K. The Sun emits electromagnetic radiation across most of the electromagnetic spectrum [9]. As a result, much of the solar radiation reaching the Earth is composed of photons with energies greater than the band gap of an absorbing semiconductor, such as silicon. These higher energy photons will be absorbed by the solar cell, while the difference in energy between these photons and the silicon band gap is converted into heat (via lattice vibrations, mathematically modeled as phonons) rather than into usable electrical energy.[9] [10]

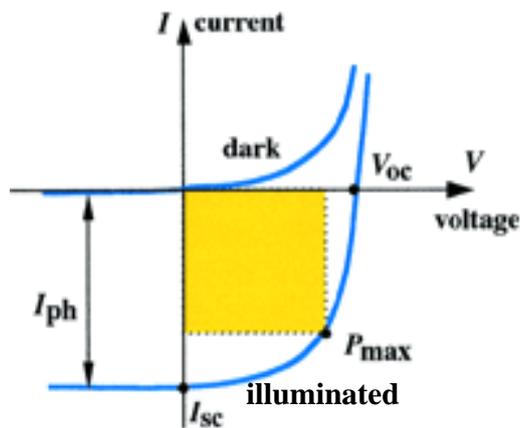
2.1.4 Definition of Solar Cell Terms

Solar cells operate in the 4th quadrant of the I-V characteristic (i.e. in the forward voltage, reverse current bias region) such that power is extracted rather than input to the device. The most frequently used figure-of-merit for solar cells is sunlight-electrical power conversion efficiency, which is defined as the electrical power produced by the cell divided by the entire solar power incident on the device.

An idealized I-V curve for a solar cell is shown in Figure 2.1.4. The illuminated I-V curve can be described by: [10]

$$I = I_s \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] - I_L$$
$$I_s = qAN_c N_v \left(\frac{1}{N_A} \sqrt{\frac{D_n}{\tau_n}} + \frac{1}{N_D} \sqrt{\frac{D_p}{\tau_p}} \right) \exp(-E_g/kT) \quad (2.1.4)$$

where I_s is the photodiode reverse saturation or “dark” current, I_L is the photocurrent, N_A and N_D are the acceptor and donor doping densities, respectively, E_g is the bandgap, D_n and D_p are the electron and the hole diffusivities, respectively, n_{p0} and p_{n0} are the electron and hole minority concentrations of the p- and n-type material, respectively, at equilibrium (far from the junction), L_n and L_p are the electron and hole diffusion lengths, respectively and are related by τ_n and τ_p , the electron and hole lifetimes.[11]



$$FillFactor = \frac{P_{max}}{V_{oc} I_{sc}}$$

$$P_{max} = V_{oc} I_{sc} FF$$

$$Efficiency = \frac{V_{oc} I_{sc} FF}{P_{in}}$$

$$= \frac{P_{max}}{P_{in}}$$

Fig. 2.1.4. Ideal photocurrent-voltage characteristic of a P-N junction device and definition of photovoltaic cell terms, adapted from Prof. Mike McGehee's MatSci 302 lecture notes.[12]

Other than conversion efficiency, there are several additional figures of merit for a solar cell I-V curve, including open circuit voltage (V_{oc}), short circuit current (I_{sc}), and fill-factor (FF). The related terms are defined as:

P_{in} : Incident solar power, the average solar irradiance, which varies greatly not only day to night, but around the globe. The standard for calibration is defined as the normalized global average illumination defined as AM1.5 spectrum, which integrates to 1000 W/m^2 , and corresponds to noon on a sunny day in a temperate latitude (the elevation of the sun is 42°) [8].

P_{max} : Maximum power point, which also marks the optimum operating current and voltage, and defines the fill-factor through the relation, $P_{max} = I_{sc} \cdot V_{oc} \cdot FF$. [12]

V_{oc} : Open circuit voltage, the measured voltage under illumination with zero current

I_{sc} : Short circuit current, the measured current under illumination with the terminals

shorted

FF: Fill Factor, defined as:

$$FillFactor = \frac{P_{max}}{V_{oc} I_{sc}}$$

And finally, efficiency is defined as:

$$Efficiency = \frac{V_{oc} I_{sc} FF}{P_{in}} = \frac{P_{max}}{P_{in}}$$

Open-Circuit Voltage [11]

The open circuit voltage is related to the bandgap of the material and the built-in voltage, the illumination intensity, the reverse saturation current, the diode ideality factor and the device parasitic resistances, etc.

The larger the bandgap, the larger the built-in voltage of a p-n junction, which produces a solar cell with a larger V_{oc} .

A higher illumination intensity will cause the illuminated curve in Figure 2.1.4 to be translated downwards, resulting in an increased V_{oc} , because of the exponential nature of the P-N junction's I-V characteristic.

From Equation 2.1.4, one can see an increase in the reverse saturation current will reduce V_{oc} by increasing the dark current at all voltages, and thus when the illuminated curve is shifted downwards it will cross the voltage axis at a smaller value of voltage.

Lastly, the diode ideality as well as the series resistance affect the shape of the I-V curve, which affects the fill-factor and the open-circuit voltage.[11] [13]

Short-Circuit Current [11]

The short-circuit current is directly related to the absorption of solar cell device, since only light that is absorbed can be converted into current. In addition, the depletion width and the carrier diffusion lengths also greatly affect short-circuit current. If the depletion width is wider, and/or the diffusion length is longer, then a larger fraction of the photo generated electron-hole pairs will be swept by the built-in electric field in the depletion region, thus collected as current. On the other hand, if the depletion width is narrower and the diffusion lengths are shorter, then only a smaller fraction of the electron-hole pairs will be swept by the electrical field in the depletion region before electron-hole recombination. This recombination event occurs as a result of an excess electron in p-type material recombining with a hole, or an excess hole in an n-type material recombining with an electron. Since the depletion width is directly related to the background doping density, the short-circuit current is also affected by the background doping concentration in the depletion region.[8][11][13]

Fill-Factor [11]

The fill-factor is determined by the optimal power point on the I-V curve, which is the point where the product of current and voltage is at its maximum value, and is defined

as $FillFactor = \frac{P_{max}}{V_{oc} I_{sc}}$

The fill-factor therefore relates to the ideality of the shape of the curve, the series and shunt resistance. Photocurrent flowing through the series and shunt resistance of the device will draw power from the cell and degrade the fill-factor of the device. For this reason, fabrication of contact electrodes of the solar cells need to specially designed to minimize the series resistance and maximize the shunt resistance [11][13].

2.2 Nanotechnology

A nanostructure is an object with a feature size of nano-scale between 0.1 and 100 nm, which is between molecular and microscopic (micrometer-sized) structures [14]. Because of nanostructure's unique properties, there are tremendous research and development focusing on nanotechnology. [24]

The first use of the concepts found in “nano-technology” was in "There's Plenty of Room at the Bottom", a talk given by physicist Richard Feynman at an American Physical Society meeting at California Institute of Technology (Caltech) on December 29, 1959 [15]. “Feynman described a process by which the ability to manipulate individual atoms and molecules might be developed, using one set of precise tools to build and operate another proportionally smaller set, and so on down to the needed scale. In the course of this, he noted, scaling issues would arise from the changing magnitude of various physical phenomena: gravity would become less important, surface tension and van der Waals attraction would become increasingly more significant, etc.[14] This

basic idea appeared plausible, and exponential assembly enhances it with parallelism to produce a useful quantity of end products.” [14][15]

The term "nanotechnology" was coined by Professor Norio Taniguchi at Tokyo University of Science in a paper of 1974 [16] as follows: "'Nano-technology' mainly consists of the processing of, separation, consolidation, and deformation of materials by one atom or by one molecule." The basic idea of this definition had been explored in much more depth by Dr. K. E. Drexler in the 1980s, who promoted the technological significance of nano-scale phenomena and applications through the books “Engines of Creation: The Coming Era of Nanotechnology”[17] and “Nanosystems: Molecular Machinery, Manufacturing, and Computation” [17]. “Engines of Creation” is considered the first book on the topic of nanotechnology. [14]

2.3 Nanotechnology in Solar Cell

Nanotechnology has been proposed as a potential means to improve high-efficiency, lower the cost of solar cells and/or enable some novel applications [18-26]. Here are a few examples related to this dissertation.

2.3.1 Amorphous Si Case

Jia Zhu, Zongfu Yu, Shanhui Fan and Yi Cui, et al, at Stanford University reported the case of amorphous Si solar cell, using nanostructure to enhance light trapping and

improve the overall efficiency in Nano Letters (2009) [20] and Nano Letters (2010) [21].

As shown in Figure 2.3.1 (c), the schematic of the cross-sectional structure of nano-dome solar cells reported in [21]. It is a single p-i-n junction nanodome a-Si:H (hydrogenated amorphous silicon) solar cells consist of 100 nm thick Ag as a back reflector, 80 nm thick transparent conducting oxide (TCO) as both bottom and top electrode, and a thin a-Si:H active layer of 280 nm (from top to bottom: p-i-n, 10-250-20 nm).[21] The nanodome solar cells were fabricated on nanocone substrates (Figure 2.3.1 (a)). Nanocone glass or quartz substrates were first fabricated by Langmuir-Blodgett assembly of close packed monodisperse SiO₂ nanoparticles followed by reactive ion etching, a novel way of making nanostructure template developed in Professor Yi Cui group at Stanford University [20][22]. The base diameters and spacing of nanocones can be controlled in the range of 100-1000 nm, which is comparable to the sunlight wavelengths. Nanocones with a base diameter of 100 nm, spacing of 450 nm and height of 150 nm are reported in this study.

The solar cell layers were conformally deposited on top of the nano-cone substrate as well as on a flat substrate for comparison. After deposition, the nanocone pattern is largely transferred to the top layer and nanocones become nanodomains, as shown in scanning electron microscopy (SEM) images (Figure 2.3.1 (b)). [20]

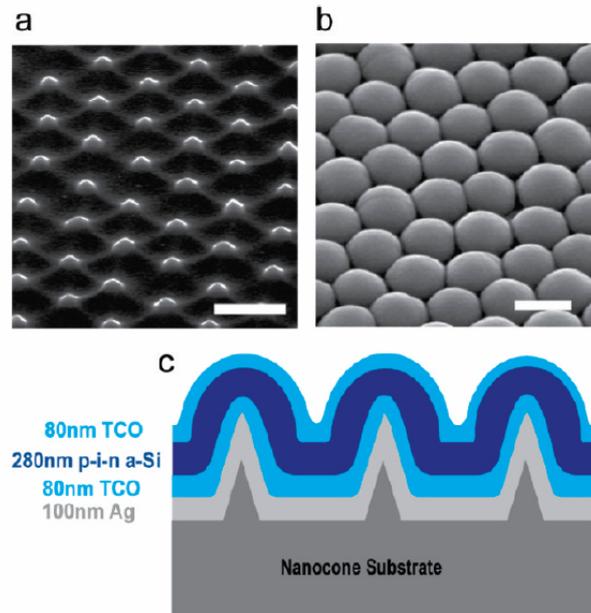


Figure 2.3.1 SEM images taken at 45 degree on (a) nanocone quartz substrate; and (b) amorphous Si nanodome solar cells after deposition of multi-layers of materials on nanocones. Scale bar 500 nm. (c) Schematic showing the cross-sectional structure of nanodome solar cells. [20]

According to the paper [21], the nanodome solar cell devices show that the power conversion efficiencies are 25% higher than the flat film device counterpart which is made under otherwise identical conditions. An example is shown in Figure 2.32 (b) left, in which the nanodome device exhibits a power efficiency of 5.9% (open circuit voltage, $V_{oc} = 0.75$ V; short circuit current, $J_{sc} = 17.5$ mA/cm²; fill factor, $FF = 0.45$) while the flat device exhibits an efficiency of 4.7% ($V_{oc} = 0.76$ V, $J_{sc} = 11.4$ mA/cm², $FF = 0.54$). This significant improvement of power efficiency comes from a large short circuit current of nanodome solar cell devices (17.5 mA/cm²) which is even higher than that (15.6 mA/cm²) of the world record single junction a-Si:H solar cells with substrate

configuration [27] with initial power efficiency of 10.6%. The short-circuit current of nanodome devices is only slightly lower than the theoretical value (20.5 mA/cm²) [28] limited by the band gap.

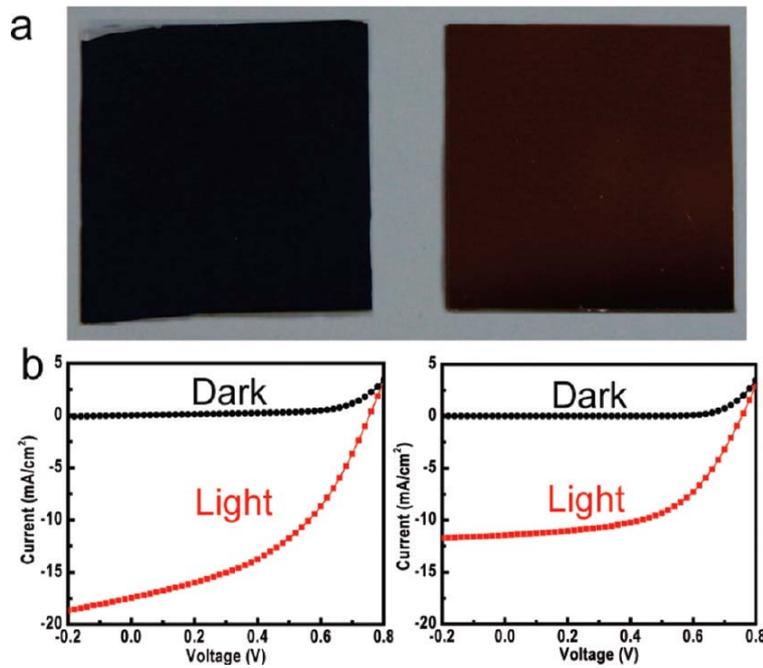


Figure 2.3.2. Power conversion of a-Si:H nanodome solar cells. (a) Photographs of nanodome solar cells (left) and flat film solar cells (right). (b) Dark and light *I-V* curve of solar cell devices for nanodomes (left) and flat substrates (right).[20]

The authors believe that they can still improve the efficiency of nanodome devices in the future by improving the open circuit voltage and fill factor via better materials deposition.

2.3.2 CdTe Case

Zhiyong Fan and Ali Javey et al at UC Berkeley reported “Three-dimensional nanopillar-array photovoltaics on low-cost and flexible substrates” in NATURE MATERIALS 8, 648 - 653 (2009) [26]. In this paper, the photovoltaic material system is CdS/CdTe.

The paper reports the direct growth of highly regular, single-crystalline nanopillar arrays of optically active semiconductors on aluminum substrates that are then configured as solar-cell modules (Figure 2.3.3)[26]. One of the most attractive properties is the flexibility of the solar cell, as shown in Figure 2.3.4. The efficiency remains almost constant when the bending radius is from 2 cm to 9 cm.

Figure 2.3.3 shows a 3D CdS/CdTe solar nanopillar (SNOP) cell uses highly periodic anodic alumina membranes (AAMs). (a) is the energy band diagram of a CdTe/CdS photovoltaic. (b) is the cross-sectional schematic diagram of a SNOP cell, illustrating the enhanced carrier collection efficiency. (c) is the fabrication process flow of the SNOP-cell.

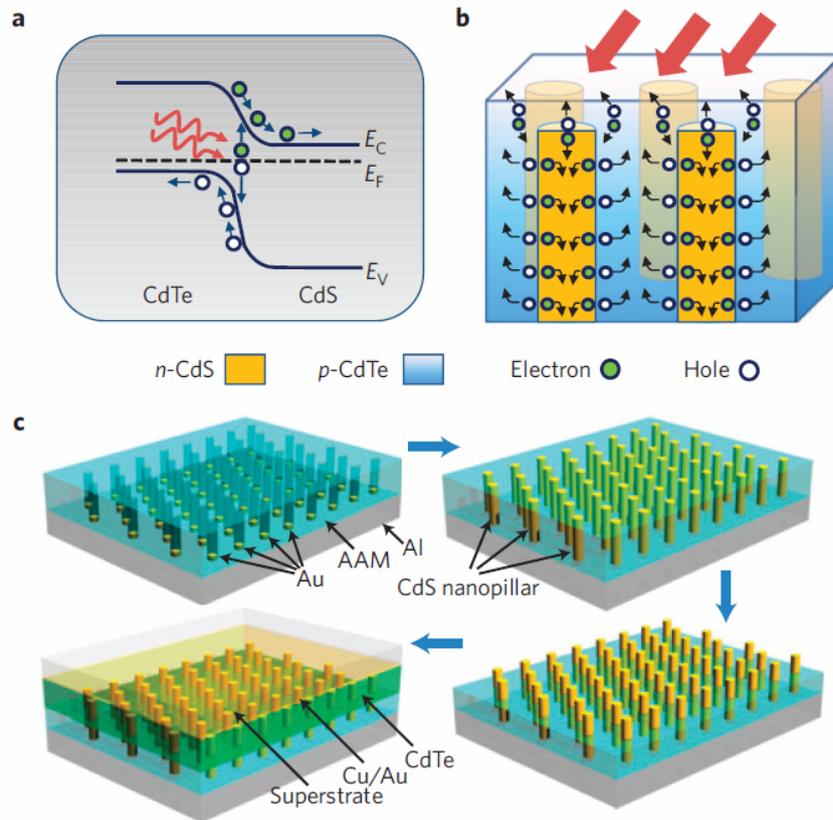


Figure 2.3.3. CdS/CdTe Solar NanoPillar (SNOP) Solar Cells. a) Energy band diagram of a CdTe/CdS photovoltaic. b) Cross-sectional schematic diagram of a SNOP cell, illustrating the enhanced carrier collection efficiency. c) SNOP-cell fabrication process flow.

Figure 2.3.4 shows the mechanical flexibility of the SNOP cells. (a) is the schematic diagram of the bendable SNOP module embedded in PDMS and (b) is the optical image of the actual device. (c) and (d) present the theoretical simulation of the strain for a flexible SNOP cell (PDMS thickness around 4 mm), showing only around 0.01% maximum strain in the nanopillars. (e) is the $I-V$ characteristics of a flexible cell for

various bending radius. (f) is the performance characterization of a flexible SNOP cell, showing minimal change in V_{oc} and efficiency on bending of the substrate. The inset shows photography of the set-up for bending the flexible modules.

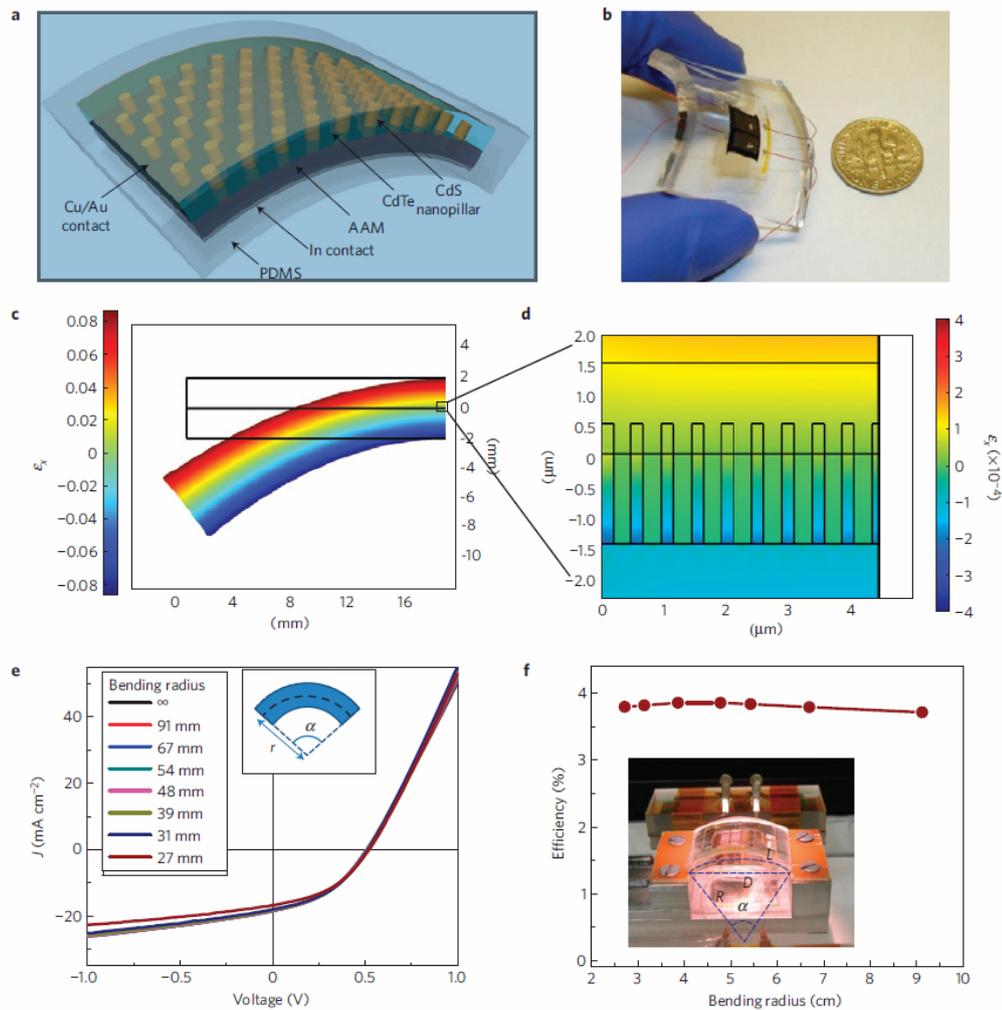


Figure 2.3.4. Mechanically flexible SNOP cells. (a) schematic diagram and (b) optical image of a bendable SNOP module embedded in PDMS. (c) and (d), theoretical simulation of the strain for a flexible SNOP cell. (e), I - V characteristics of a flexible cell for various bending radius. (f). Performance characterization of a flexible SNOP cell. The inset shows a picture of the set-up for bending the flexible modules.

2.3.3 Core-shell Structure

In recent years, Harry A. Atwater group at California Institute of Technology proposed a core-shell structure (or radial P-N junction) “Radial PN Junction Nanorod Solar Cells: Device Physics Principles and Routes to Fabrication in Silicon”. [25][29]: “A nano-rod with a PN junction in the radial direction allows for separation of the requirements of light absorption and carrier extraction in two orthogonal directions. The cell can be thick in one dimension for optimal light absorption, while thin in another, for optimal carrier collection” [29]. As shown in Figure 2.3.5, (a) is a schematic of a traditional planar single junction solar cell. (b) is a schematic of a radial junction nano-rod solar cell. (c) is schematic and cross-section of the radial pn junction nanorod cell. Light is incident on the top surface. The light grey area is n-type, the dark grey area p-type.

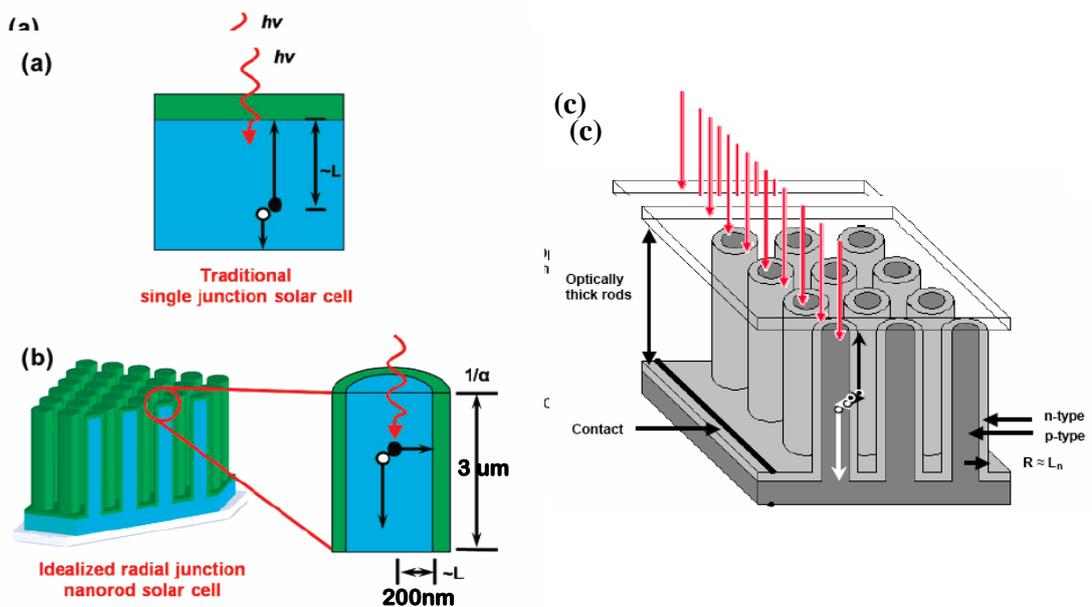


Figure 2.3.5. (a) A schematic of a traditional planar solar cell; (b) schematic of a radial junction nanorod solar cell. (c). schematic and cross-section of the radial P-N junction nanorod cell. [29]

2.4 Our Discovery and Enabling Factor

We accidentally discovered that the surface kinetics and epitaxial growth by MBE/MOVPE largely altered when growing on nanostructures compared to flat surfaces in the conventional III-V material growth. This discovery enables uniform, single crystal growth of low defect density materials on nanostructures with high aspect ratios thus enables the applications of nanostructure to III-V solar cells and new design paradigm in multijunction solar cells in our research group at Stanford University for the first time. [30] [31]

We have also found that the GaAs layers can be grown on Ge nano-structures independent of substrate material, enabling the usage of flexible, less expensive substrates, as illustrated in Figure 2.4.1 (a,b). For most conventional III-V epitaxy, single-crystal substrates such as GaAs or InP are required; this process eliminated that need, reducing the material cost of III-V solar cells.

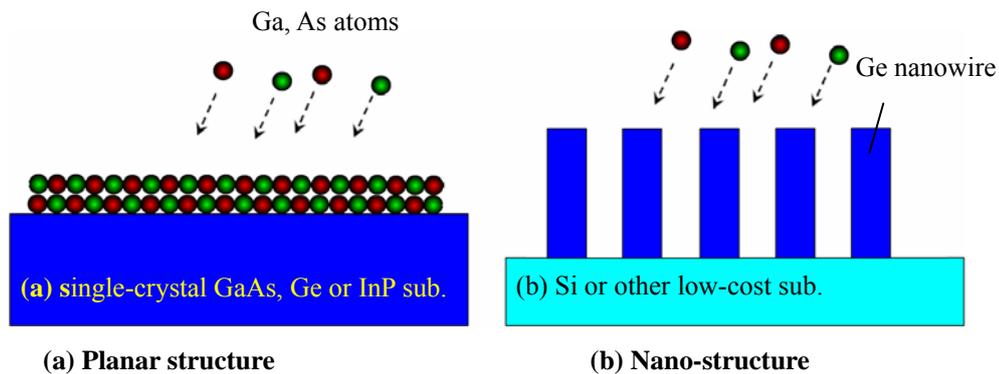


Figure 2.4.1(a) GaAs or Ge single-crystal substrates are required in the conventional III-V epitaxial growth; (b) III-V epitaxial growth on nanostructure, with good sidewall adhesion.

Our exploratory results shows that uniform, conformal, single-crystal growth of low defect lattice matched or mismatched multijunction materials over 3-dimensional nano-structures on cheap substrate (such as silicon or other low cost flexible material) is possible, as shown in Figure 2.4.2.

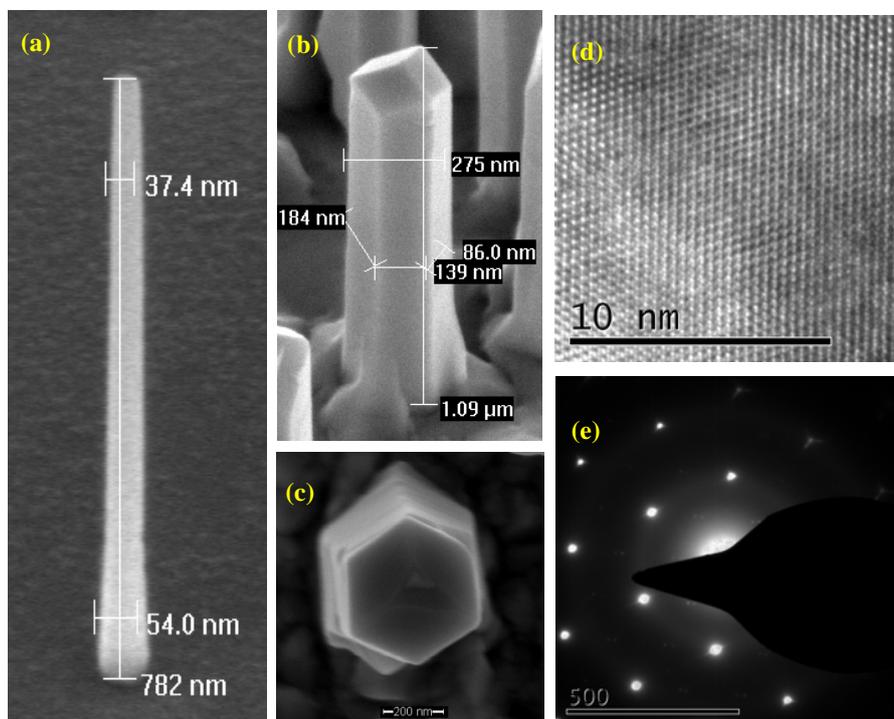


Figure 2.4.2 (a) Ge nanowire grown on silicon substrate. (b) SEM 45 degree view of GaAs core-shell structure conformally overgrown on Ge nanowire. (c) SEM top view image shows the hexagonal shape of GaAs core-shell structure. The single crystalline core-shell structure is also evident in (d) SAED (Selected Area Electron Diffraction) pattern and (e) HRTEM (High-Resolution Transmission Electron Microscopy).

2.5 Possible Extra Benefits for Multijunction

The enabling factor of growing III-V material on 3-d nanostructure might give extra benefits for multijunction configuration. As shown in Figure 2.5 (a) there is large lattice mismatch between Ge subcell and InGaAs subcell. A grading structure has to be added to make the lattice matching transition. It is the same necessity in Figure 1.5 (a) to add the buffer region. This grading buffer region costs additional raw material and causes unfavorable series resistance.

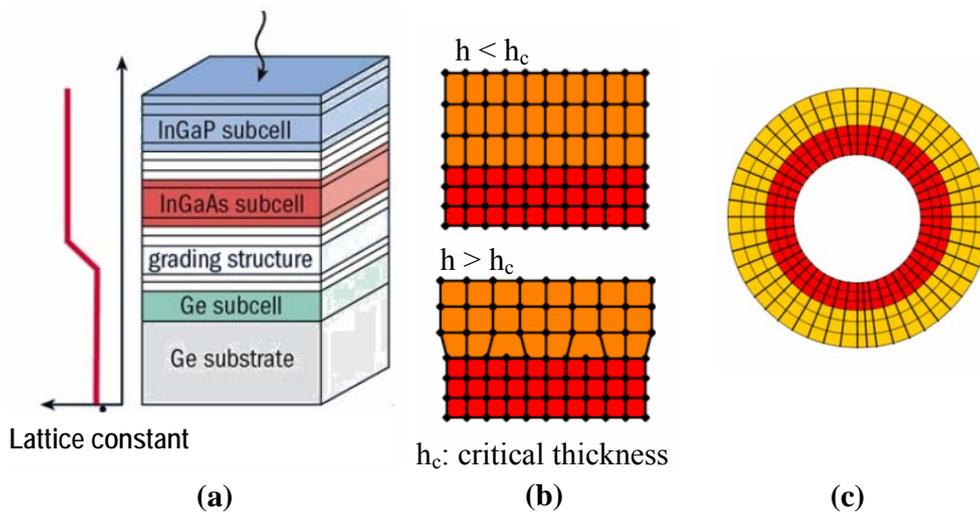


Figure 2.5 (a) Grading buffer layers in multijunction SCs. (b) Lattice mismatch in planar structure (side view). (c) Lattice mismatch in 3D nanowire structure (top view).

Figure 2.5 (b) shows the lattice mismatch process in planar structure (side view). Different color indicates different material with different lattice constants. h_c is the critical thickness, when the epitaxial thickness h is less than h_c , the stress caused by the lattice difference is still accommodable; while h is greater than h_c , the accumulated stress

have to be released, thus dislocation and defects are formed. Therefore, it is critical to gradually change the material composition carefully to avoid the defects caused by lattice mismatch.

Figure 2.5 (c) shows that it is more tolerant to lattice mismatch in 3-D nano-scale heterostructure than that of the planar bulk heterostructure. In the 3-D nano-scale core-shell heterostructure, the spacing increases in radial direction thus more atoms can fit in. It eliminates or reduces less thickness of buffer layers. In later chapters, we will also demonstrate that less anti-phase domain in the 3-D growth of GaAs on Ge nanostructure compared to the planar growth of GaAs on planar Ge substrate.

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Chapter 3 Device Design

Our first exploratory growth was using MBE to grow GaAs on Ge nanowires. Nanowires are quite common nanostructures that have been reported extensively in the literature [1][2]. Our MBE and MOVPE recipes were developed for the growth of GaAs on Ge nanowires. Fortunately, in our investigation we discovered that nano-pyramids have several superior properties compared to nanowires. In this chapter, we examine and compare nanowire and nanopyramid structures, focusing on the electrical and optical properties of these two types of designs. The actual nano-patterning and MBE/MOVPE material growth will be presented in Chapters 4 and 5.

3.1 Nanostructured Solar Cell Device Design

Nanotechnology “is likely to change the way almost everything - from vaccines to computers to automobile tires to objects not yet imagined - are designed and made” [3]. As a deployment of this philosophy, nanowires and other nanostructures have recently emerged as a possible route to lower-cost, higher-efficiency solar cells [15][16][17]. By decoupling the optical path length for incident light from the distance between the

contacts for photogenerated carriers, nanowire solar cells can enhance carrier collection efficiency [18]. Nanowire arrays also demonstrate excellent light trapping properties [19].

Most arrays are fabricated from c-Si [17], low-cost CdTe [16] or a-Si [19]. Single-nanowire solar cells based on GaAs have also been reported [20][21]. III-V materials have several advantages over other materials, particularly a much shorter absorption depth and a wide range of variable band gaps and lattice constants that can be used to adjust cell parameters. [4]

In our nanostructured III-V solar cell design, we utilize nanotechnology to lower the cost of substrate and retain high standard efficiency of III-V solar cell. Figure 3.1.1 illustrates such design concept. (a) shows a nanowire configuration: Ge nanowire is grown on SOI (Silicon on Insulator) via VLS (Vapor Liquid Solid) method with Au as a catalyst. The Au is removed before loading into the MBE/MOVPE chamber. Then the 1st P-N junction is conformally grown on the Ge nanowire, followed by a tunnel junction and the 2nd P-N junction. Lastly an ITO (Tin doped Indium Oxide) layer is conformally coated to connect all the other individual nanowire units [4].

The material growth of the GaAs/Ge core-shell structure is achieved by MBE and MOVPE, resulting in structures illustrated in a SEM 45 degree view shown in Figure 3.1.1 (b). The clear facets on the tips and sidewall are direct evidence of high quality single-crystalline. We will utilize these facet features in the optical simulation, as also shown in Fig. 3.3 (b), the tip of the nanowire solar cell is faceted instead of round shape.

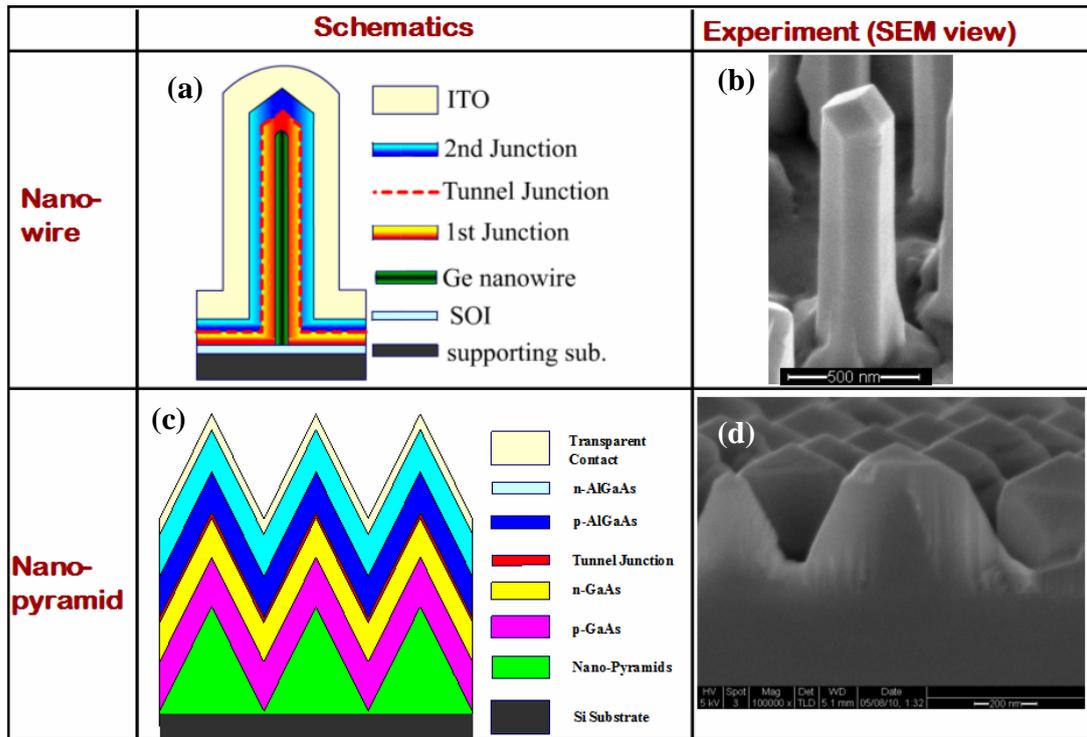


Figure 3.1.1 Design of multijunction AlGaAs/GaAs/Ge solar cell on cheap substrate in (a) (b) nanowire and (c) (d) nano-pyramid configurations.

However, there is a corner case in the nanowire configuration that the full potential of multijunctions is not reachable, e.g., when the sun light is at normal incidence, it is hard to determine exactly which band gap material that the light passes through first, as shown in Figure 3.1.2(a), the red arrow indicates the normal incidence. While for other skew incident angles, (as indicated in the blue arrow), it is obvious that the light passes through the wider band gap material first and then smaller band gap material, which is exactly the purpose of the multijunction concept.

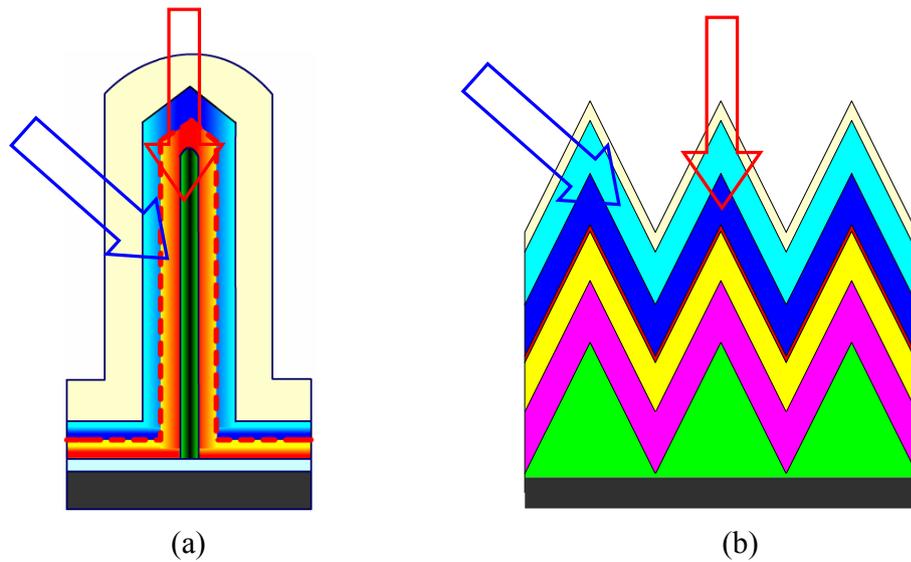


Figure 3.1.2 Normal incidence and skew incidence cases in nanowire and nano-pyramid configurations.

To compensate for the shortcoming of nanowire solar cell, we initialize the nano-pyramid solar cell configuration. Figure 3.1.1 (c) shows a nano-pyramid GaAs/Ge solar cell on a cheap substrate.. The supporting substrate can be low-grade silicon or another cheap material. The Ge nano-pyramid template is formed by the method described in Chapter 4. The 1st P-N junction (GaAs) is conformally grown on the nano-pyramids, followed by a tunnel junction.. Then the 2nd P-N junction (AlGaAs) is conformally grown on top of the tunnel junction. Finally, a transparent contact layer is deposited to connect all pyramid arrays and collect all the current generated from the each pyramid unit. Figure 3.1.1 (d) shows the proof-of-concept MOCVD (Metal-Organic Chemical Vapor Deposition) growth of a high quality GaAs/Ge core-shell structure.

For this nano-pyramid configuration, normal incidence is not a problem any more. As shown in Figure 3.1.2 (b), even at normal incidence, the light still passes through the

wider band gap material first and then smaller band gap material.

Another superior property about these nanostructured solar cells is the mechanical flexibility as their total thickness is about 2 μm and the spacing between each individual wire/pyramid is around 200-300nm. Fig. 3.1.3 illustrates the flexible nanowire/nanopyramid arrays.

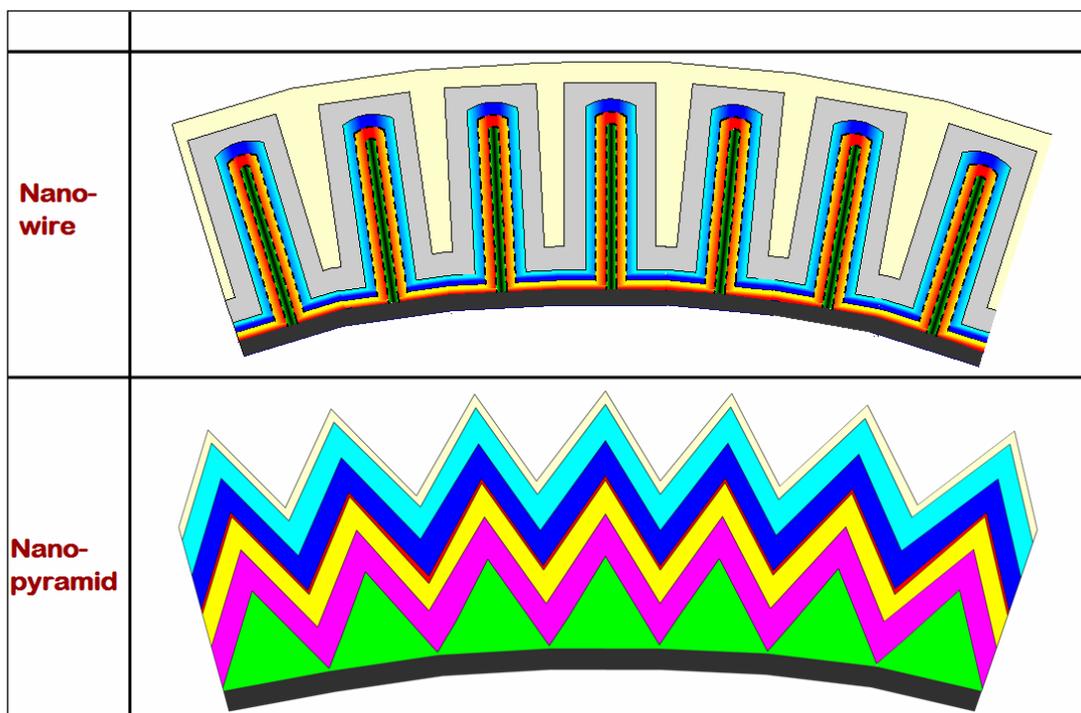


Figure 3.1.3 Nanowire/nanopyramid solar cell bonded to a flexible substrate.

3.2 Electrical Simulation

The advantage of the nano-scale core-shell structure is decoupling the light absorption and carrier extraction directions. TCAD simulations [5] demonstrate that the electrical field is conformally distributed along the interfaces of the layers and confirms

that the minority carriers can be swept towards the direction that is normal to the interface and collected by the electrodes.

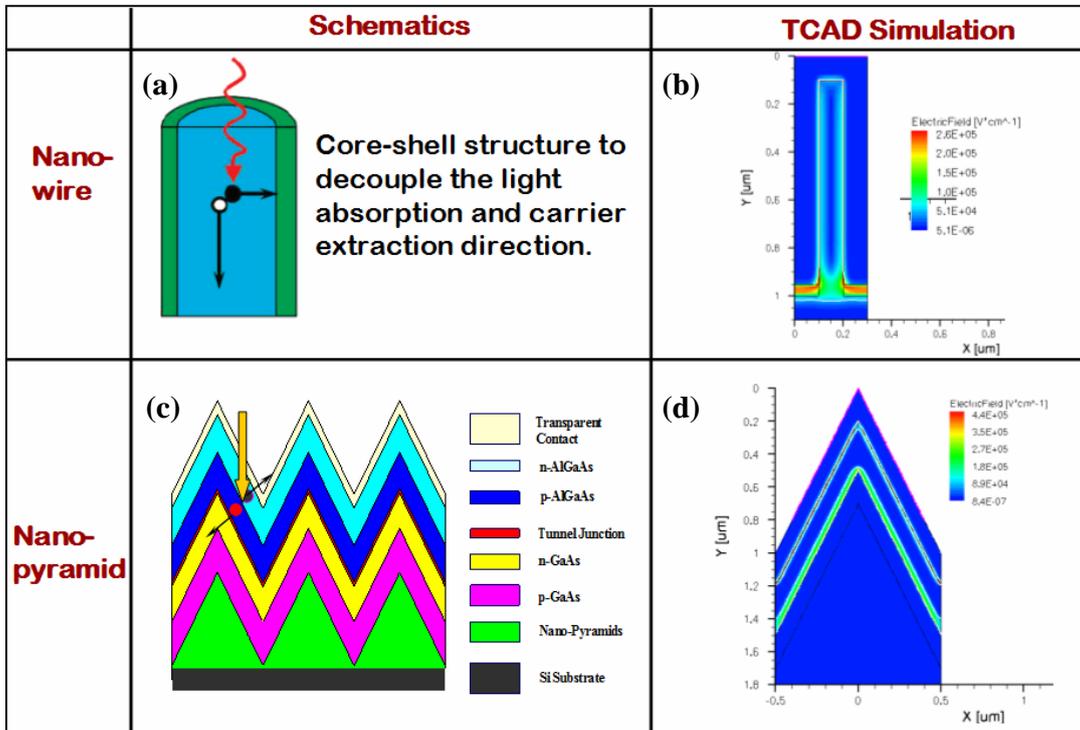


Figure 3.2. TCAD electrical simulations of nanowire and nanopyramid solar cells

Figure 3.2 illustrates the differences of the nanowire and nanopyramid. Figure 3.2 (a) is a schematic of the nanowire core-shell structure to decouple the light absorption and carrier extraction directions which are orthogonal in the nanowire case: light comes in vertically, while the electron (or holes) moves at the direction normal to the surface of the nanowire wall, which is horizontal. (b) is a TCAD simulation of the electrical field, the contour plot shows the conformality of electrical field profile to enable the carrier extraction direction to be in the lateral direction. Figure 3.2 (c) is a schematic of the

nanopyramid core-shell structure to decouple light absorption and carrier extraction directions: light comes in vertically, while the electron (or holes) moves at the direction normal to the slope of the pyramid. (d) is TCAD simulation of the electrical field, the contour plot shows the conformality of electrical field profile to enable the carrier extraction direction an acute angle with the light absorption.

3.3 Optical Simulations

Nanowire structures can greatly improve the light absorption over a wide range of spectra and incident angle due to the gradual effective refractive index changing and multiple reflection trapping [19]. Reflection not only affects the absorption power in the solar cell, but also affects the V_{oc} as well as filling factor, which causes a decrease in efficiency [4].

When the feature size of the nanostructure is comparable to the wavelength of light, some interesting nano-photonics phenomena become apparent. Conventional geometric optics is no longer valid; FDTD (Finite-difference time-domain) or RCWA (Rigorous Coupled Wave Analysis) methods are needed to study sub-wavelength effects.

3.3.1 FDTD Simulations

Finite-difference time-domain (FDTD) [6][7][8] is a computational electrodynamics modeling technique used to simulate Maxwell's Equations. It is a

time-domain method with solutions which can cover a wide frequency range with a single simulation run. FDTD is a grid-based differential time-domain numerical modeling method. The time-dependent Maxwell's equations (in partial differential form) are discretized using central - difference approximations to the space and time partial derivatives. The resulting finite-difference equations are solved in a leapfrog integration [9], a simple method for integrating differential equations: the electric field vector components in a volume of space are solved at a given instant in time; then the magnetic field vector components in the same spatial volume are solved at the next instant in time; and the process is repeated over and over again until the desired transient or steady-state electromagnetic field behavior is fully evolved[6].

We use a commercially available software package called Lumerical [10] to solve the sub-wavelength nano-photonics problem. The simulated structures are in the range from a few nanometers to tens of microns.

Figure 3.3 (a) shows the strong light coupling in nanowires with diameters comparable to the wavelength of light, reported in Nature Nanotechnology, Vol. 5 (2010) [11] and Nature Materials, July 2009 [12].

Figure 3.3 (b) shows FDTD simulation of the optical field distribution in a 1500 nm x 500 nm nanowire. At the wavelength of 800 nm, there is strong absorption in the nanowire; while at the wavelength of 1200nm, which is already beyond the GaAs absorption band edge, it still shows a strong resonance effect. However, for planar

structures, it has essentially no absorption in such a long wavelength region.

Figure 3.3 (c) shows the light coupling schematic in nanopyramid configuration. (d) is a FDTD simulation of optical field distribution in a nanopyramid (base width = 500 nm, height = 500 nm). One typical snapshot of the continuous wave simulation at the wavelength of 800 nm shows strong absorption.

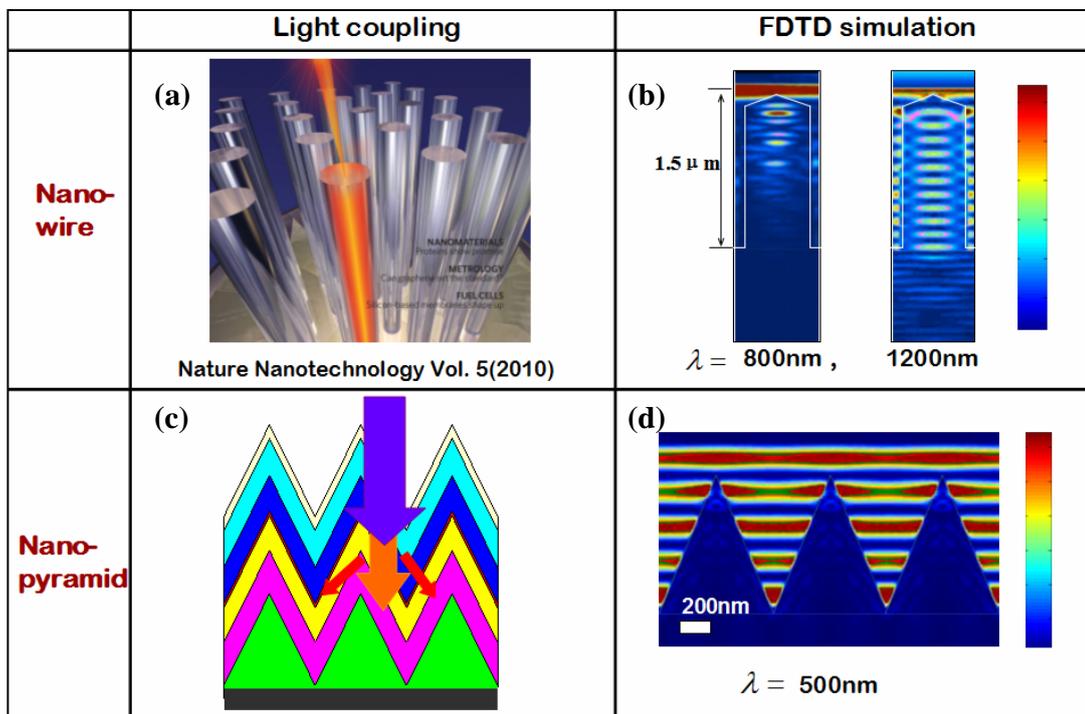


Figure 3.3 FDTD simulation shows strong optical coupling in the nanowire and nanopyramid, structures even at wavelengths beyond the semiconductor's absorption edge.

3.3.2 RCWA Simulations

Rigorous Coupled Wave Analysis (RCWA) is another powerful tool for sub-wavelength photonic simulation [13][14]. It is a fast, flexible optical grating solver which calculates an exact solution to the Maxwell equations for the diffraction of light from an optical grating, with arbitrary profile and materials defined by the user [13]. This

suits our needs for both planar structures and 3-D structures using the multilayer discretization approximation.

We worked with Dr. Zongfu Yu in Professor Shanhui Fan's research group at Stanford University [22][23] to implement the RCWA simulation for our nanostructures [4].

Figure 3.3.2.1 shows the process of discretization of a nano-pyramid. Figure 3.3.2.1 (a) is the side view of the pyramid, while Figure 3.3.2.1 (b) is top view for each layer, where $\epsilon_{ps 1}$ and $\epsilon_{ps 2}$ are the reflective index for air and absorber materials, respectively.

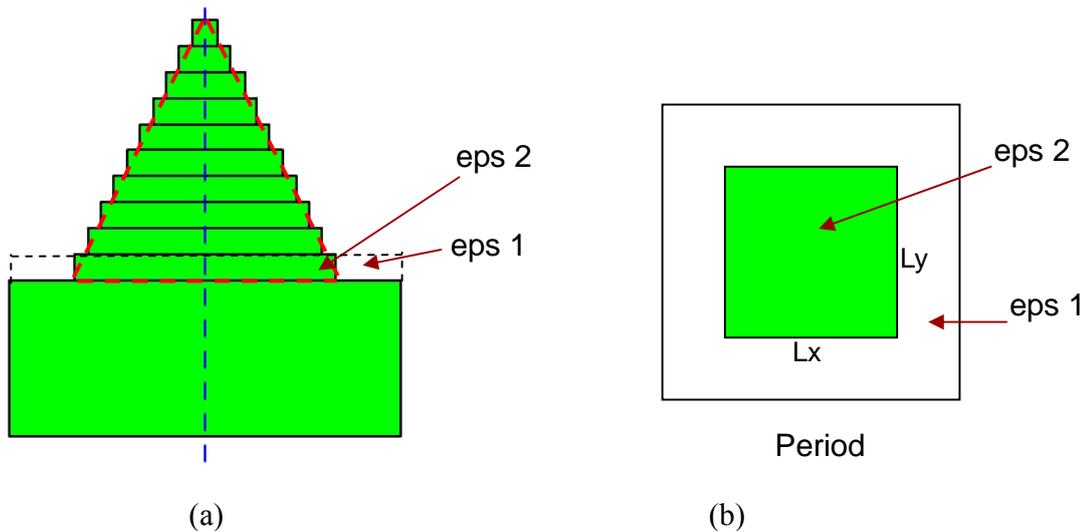
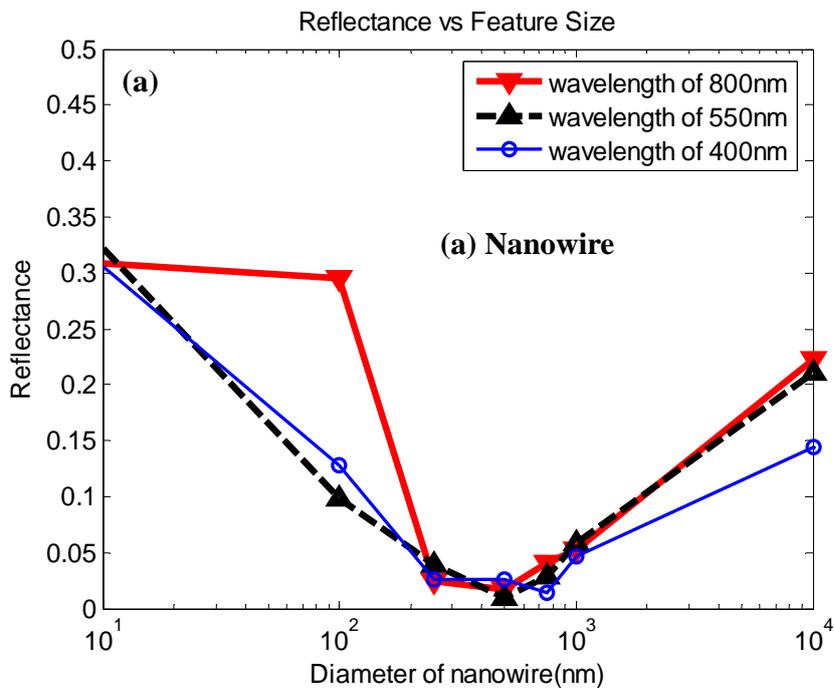


Figure 3.3.2.1. Structure definition for Multi-layer RCWA simulation for nanopyramid structure. Definition of the $\epsilon_{ps 1}$ and $\epsilon_{ps 2}$, the refractive indecies and L_x L_y , the geometrical factors of the structure as indicated in the figure.

(i) Size Dependence

In our design, we first need to decide what size of nanowire gives optimal optical properties, e.g. suppress reflection and enhance absorption of sun light. We simulate the reflection over different feature size for both nanowire and nanopyramid. The feature size is defined as diameter for nanowire and bottom width for nanopyramid. The result is shown in Fig. 3.3.2.

For the nanowire case, we sampled wavelengths of 400nm, 550nm and 800nm, the reflectance is all below 5% when the diameter of nanowire is in the range of several hundred nanometers. For the nanopyramid case, the minimum reflectance (nearly 0%) occurs from 200 nm to 500 nm of feature size for all three different wavelengths of 400nm, 550nm and 800nm.



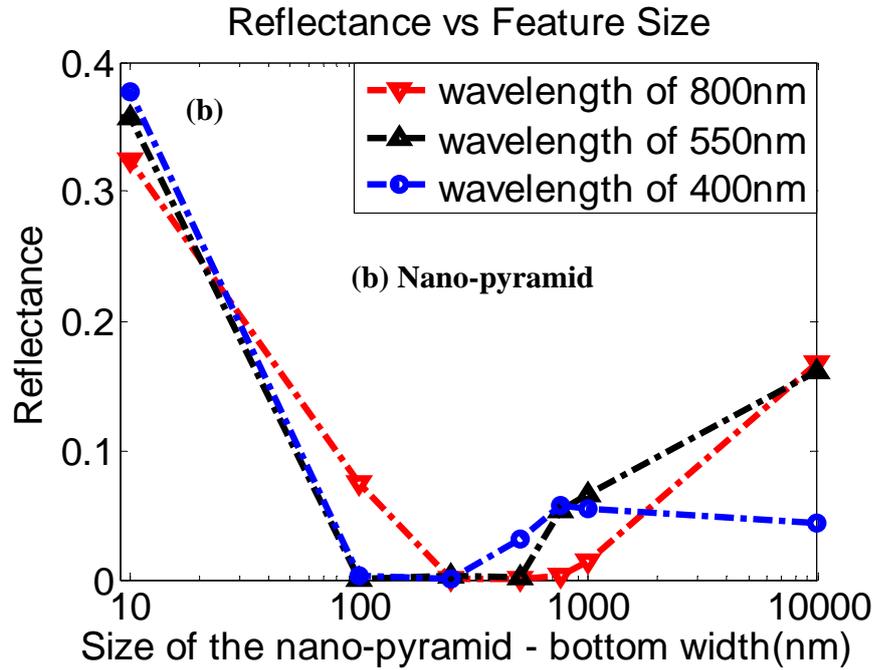


Figure 3.3.2.2. Rigorous Coupled Wave Analysis (RCWA) simulation of size dependence. Y axis is reflectance, X axis is feature size (defined as diameter for (a) nanowire and bottom width for (b) nanopyramid).

(ii) Spectral Reflectance

As solar cells work under continuous sun spectrum, it is important to study the spectral response of reflection, absorption and transmission. Figure 3.3.2.3 shows our RCWA simulation of reflection vs. spectra for planar (bulk) GaAs (a), GaAs nanowire array (b) and nanopyramid array (c). For bulk GaAs, the reflectance is about 30% to 40% in most wavelength range. For GaAs nanowire, the reflectance is reduced 2 to 3 times; while for GaAs nanopyramid, the reflectance is reduced dramatically to less than 3%.

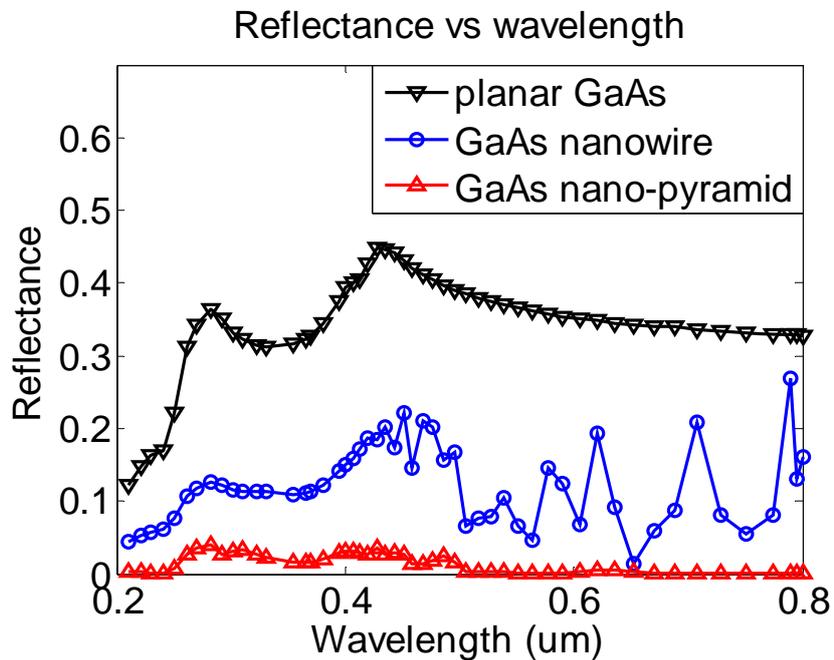


Figure 3.3.2.3. Reflectance vs. Spectrum for planar (bulk) GaAs (black), GaAs nanowire array (blue) and nanopyramid array (red)

(ii) Angular Dependence

For real world applications of solar cells, it is important to consider the absorption versus sunlight incident angle. Figure 3.3.2.4 illustrates the sun light incident angle for different times of a day and different latitudes of the Earth.

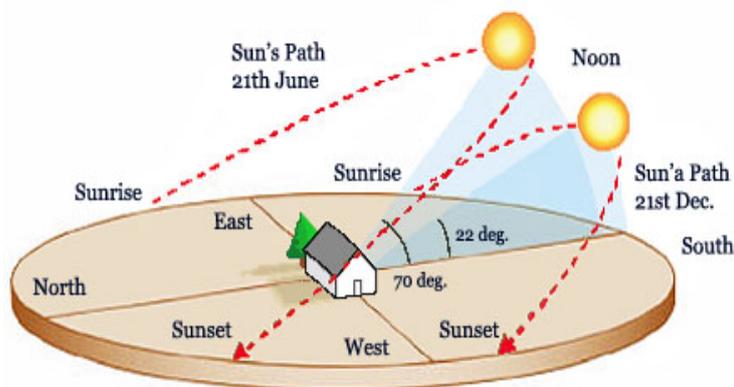


Figure 3.3.2.4 The sun light incident angle for different time of a day and different latitude of the Earth.

One of the most attractive properties of our nanostructured solar cells is the large acceptance angle to receive sunlight. Figure 3.3.2.5 shows the absorption vs. incident angle for (a) planar (bulk) GaAs, (b) three layer ARC (Anti-Reflection Coating) and (c) GaAs nanowire array (d) nanopyramid array.

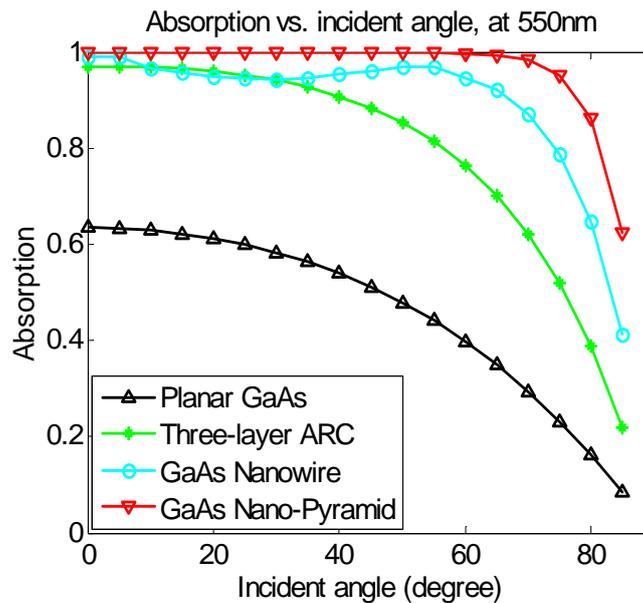


Figure 3.3.2.5 Angle dependence simulation. Absorption vs. incident angle for planar (bulk) GaAs (black), three layer ARC (Anti-Reflection Coating) (green) and GaAs nanowire array (turquoise) nanopyramid array (red).

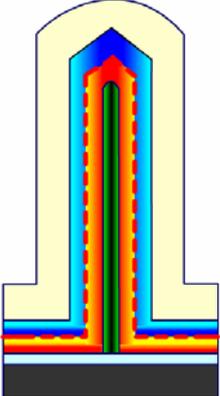
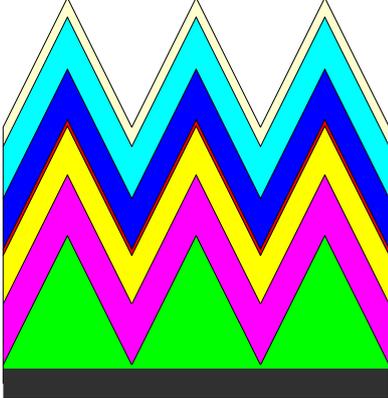
Based on this simulation, over one day (24 hours), the nano-pyramid GaAs solar cell generates 2.08 X energy of that of planar GaAs solar cell!

3.4 Summary

This chapter presented the optoelectronic nanostructured device design, electrical simulation and optical Simulation (FDTD and RCWA) for the size dependence, reflectance vs. spectrum, and angle dependence for nanowire / nanopyramid

configurations, the comparison is given in Table 3.4.

Table 3.4 Comparison of solar cell design of nanowire and nanopyramid

		
Surface/Volume Ratio	More	Less
Surface recombination	More	Less
Multijunction configuration	Problematic when normal incidence	More favorable for multijunction
Absorption	Good	Better
Incidence acceptance angle	Wide	Wider
Overall	Good	Better

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Chapter 4 Nanostructured Template Preparation

4.1 Two Strategies: Bottom-up and Top-down

In general, there are two strategies to make nanostructures: bottom-up and top-down. The bottom-up approach literally means that nanostructures start from molecular precursors and by a nano-synthesis process, form disordered nanostructures as shown in Figure 4.1(a). In the top-down approach, nanostructures are created by lithography and etching from bulk material, forming ordered nanostructures, as shown in Figure 4.1(b).[1]

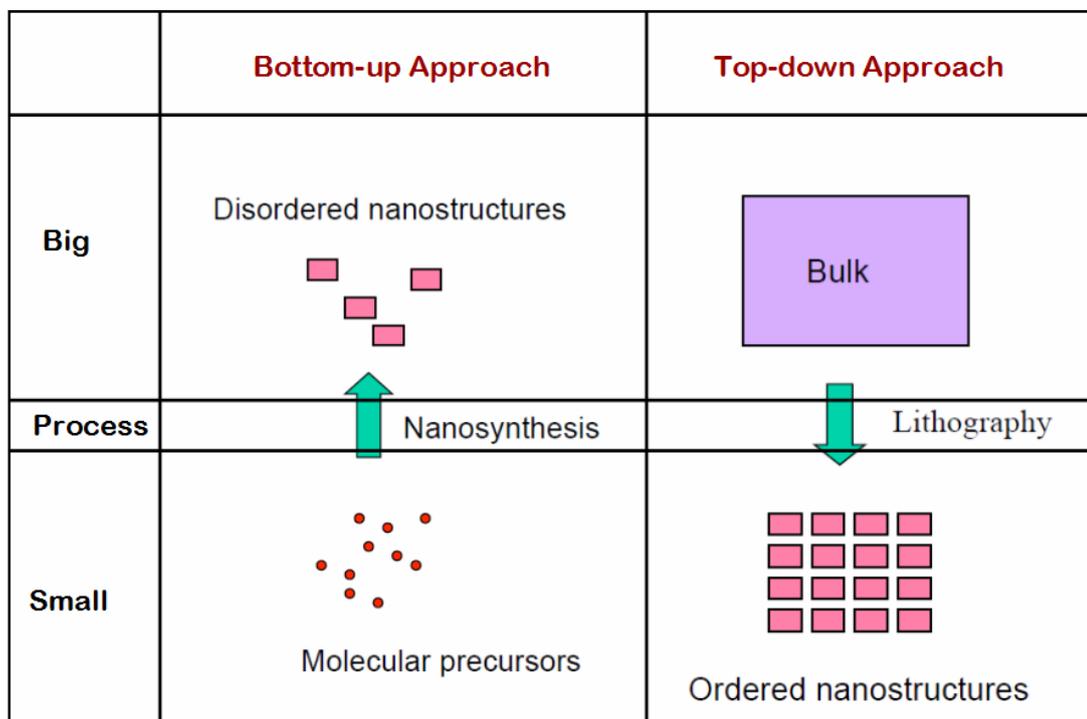


Figure 4.1 Bottom-up vs. Top-down strategies for nanostructure fabrication. Adapted from Professor Yi Cui's MatSci316 slides [1].

4.2 Bottom-up Approach

In the bottom-up approach we utilized, nanostructures are synthesized by the VLS (Vapor Liquid Solid) method [2][3] with nanoscale catalysts, in our case, the catalysts are Au nano-particles.

4.2.1 VLS Growth of NW

The vapor-liquid-solid method (VLS) is a mechanism for the growth of one-dimensional structures, such as nanowires, from chemical vapor deposition [2].

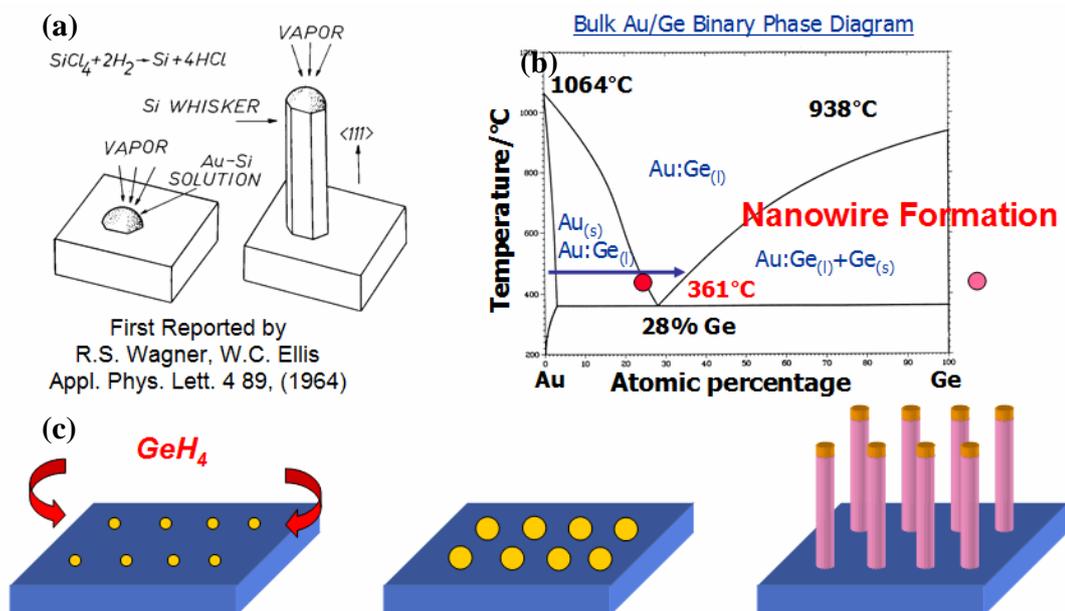


Figure 4.2.1.1 (a) Schematic illustration of Si nanowire growth from the reaction of SiCl_4 and H_2 vapor phases [3]. (b) Phase diagram of Au and Ge. (c) Schematic illustration of Ge nanowire growth by VLS method with Au as catalyst.

“Growth of a crystal through direct adsorption from the gas phase on to a solid surface is generally very slow. The VLS mechanism circumvents this by introducing a

catalytic liquid alloy phase which can rapidly adsorb a vapor to super-saturation levels [4], and from which crystal growth can subsequently occur from nucleated seeds at the liquid-solid interface. The physical characteristics of nanowires grown in this manner depend, in a controllable way, upon the size and physical properties of the liquid alloy.” [2]

The diameters of the nanowires are mainly controlled by the diameters of the Au nanoparticle catalyst [5]. Au nanoparticles can be synthesized with controlled diameters, as demonstrated in the pioneering work by Professor Yi Cui (as a PhD student) and Professor Lieber at Harvard University [5]. Figure 4.2.1.2 (a) is an example of such a Ge nanowire. (b) is a schematic illustrating the control of diameters of the nanowires. (c) is a TEM bright field image of Au catalyst and Si nanowire tip. (d) is a high resolution TEM image of the body of a Si nanowire, showing the lattice structure.

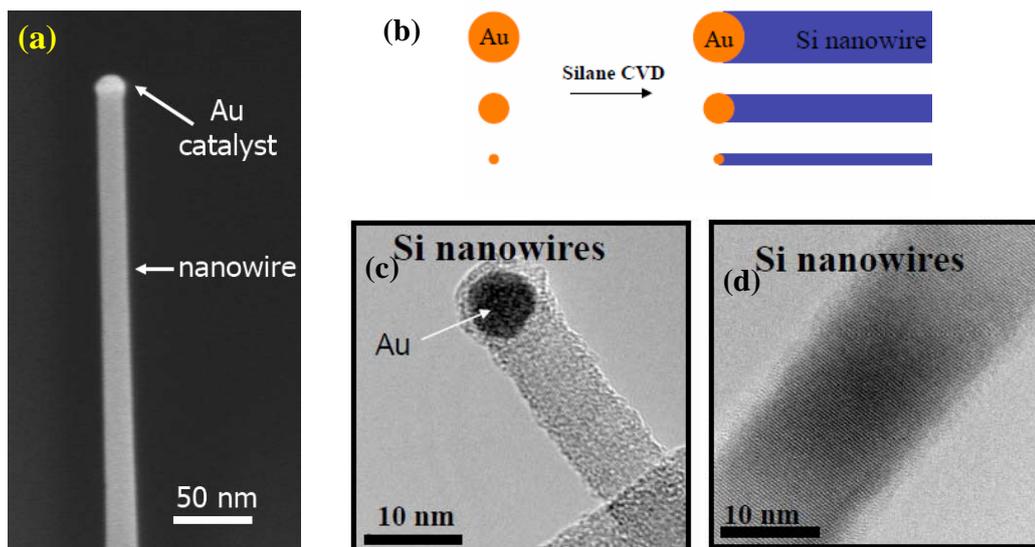


Figure 4.2.1.2 (a) An example of Ge nanowire [6] (b) Nanowire diameter control is achieved by the

Au catalyst diameter. (c) TEM of Au catalyst and Si nanowire tip. (d) TEM high resolution of Si nanowire body. [1]

In the research project described in this dissertation, we worked with Professor Paul McIntyre in Material Science and Engineering Department for Ge nanowire growth [6][7][8]. Figure 4.2.1.3 (a) shows a picture of the nanowire reactor facility used for Ge nanowire growth. The system is located in Paul Allen Center for Integrated Systems at Stanford University. Figure 4.2.1.3 (b) shows a schematic drawing of the cold wall, lamp heated, chemical vapor deposition (CVD) system. The growth gases are germane (GeH_4 , for Ge nanowire growth) and silane (SiH_4 , for Si nanowire growth). The carrier gas is hydrogen. The chemical reaction formula is [9][10]:

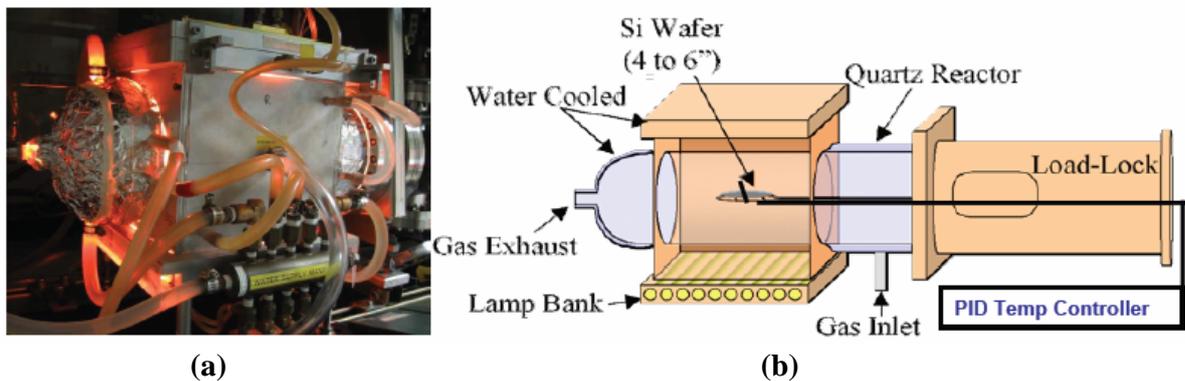


Figure 4.2.1.3 (a) Photograph of the nanowire reactor facility used for Ge nanowire growth; (b) Schematic drawing of the cold wall, lamp heated, Chemical Vapor Deposition (CVD) nanowire growth system.

Based on previous studies of the density of nanowires and time of gold colloid deposition on silicon substrates [7][8], the density of Ge nanowires can be well controlled by the surface condition of substrate and the duration of the gold colloid deposited on the substrate. Figure 4.2.1.4. (a) is a SEM micrograph showing gold colloid deposition from a 2 min exposure of hydrogen-terminated Si (111) to 40 nm gold colloid solution containing 0.1M HF. (b) is the cross-section SEM of Ge nanowire grown epitaxially on Si (111) from 40 nm gold colloids (nano-particle) deposited using the HF-addition method showing predominantly vertically oriented Ge NW of uniform diameter and length. (b) is a plot of 40 nm gold colloid density vs deposition time on Si (111) substrates. The solid line is a guide to the eye based on the square root time dependence of gold colloid deposition density that has been previously observed for a related system. [7].

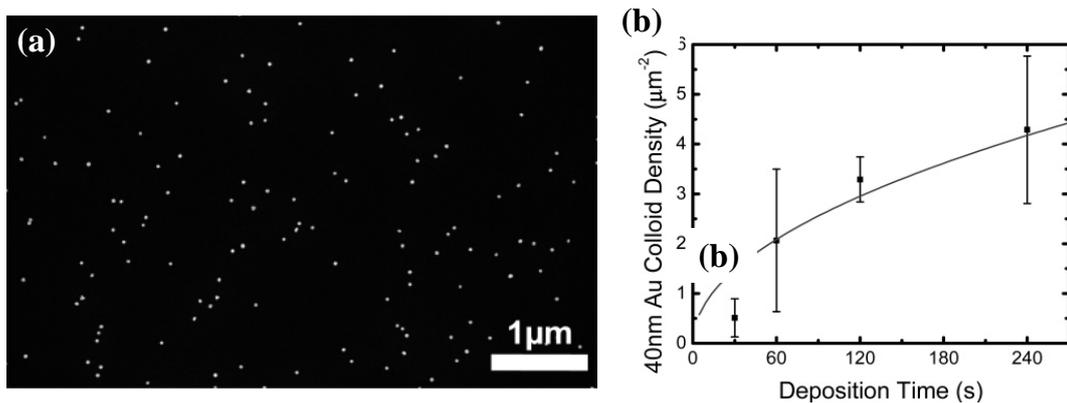


Figure 4.2.1.4. (a) SEM pictures showing gold colloid deposition from 2 min exposure of hydrogen-terminated Si(111) to 40 nm gold colloid solution containing 0.1M HF. (b) Plot of gold colloid density versus deposition time on Si (111) substrates. [7].

Working with Shu Hu and Shurti Thombare in Professor Paul McIntyre's group at Stanford University, we have demonstrated the efficacy of a controlled temperature program during CVD to obtain highly parallel and epitaxial Ge $\langle 111 \rangle$ nanowires on Ge $\langle 111 \rangle$ and Si $\langle 111 \rangle$ wafers (Figure 4.2.1.5 (a)) at temperatures below 400°C [7]. Deposition occurs by the VLS mechanism from an undercooled Au-Ge liquid which is fed by the selective decomposition of GeH₄(g) at the liquid surface. Our results show that growth along all but the vertical $\langle 111 \rangle$ direction can be suppressed and a very high fraction of vertical nanowires can be obtained by careful control of the temperature during initiation of the epitaxy (Figure 4.2.1.5 (b)). [29]

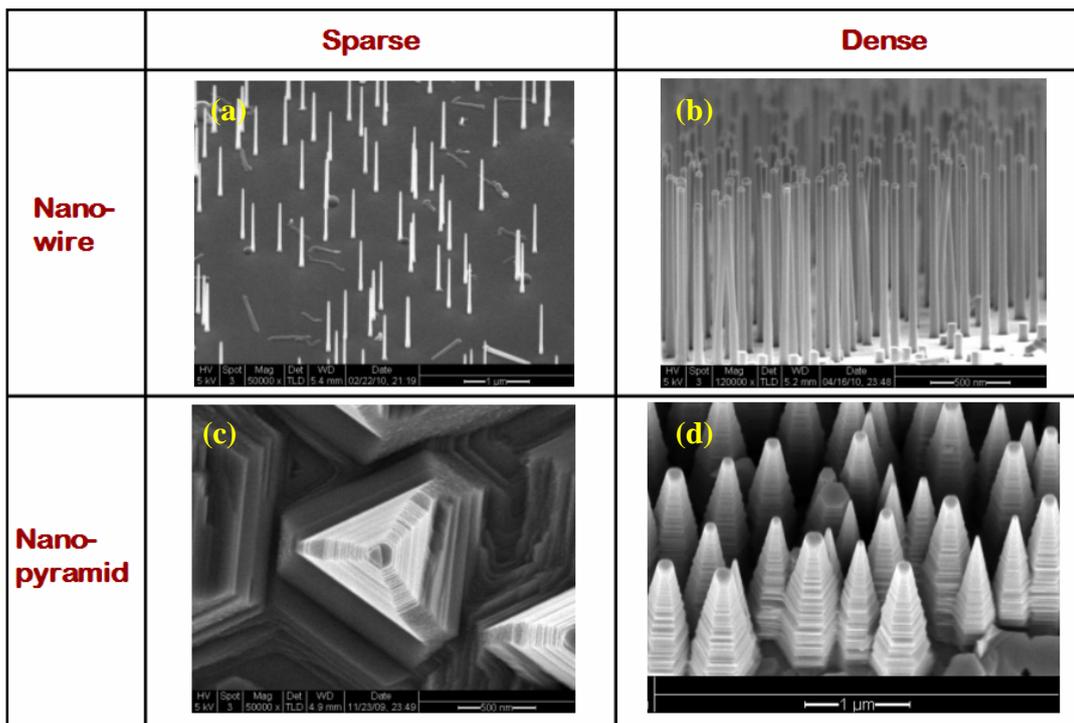


Figure 4.2.1.5 VLS growth of nanostructures of different shape and density. (a) Sparse nanowire. (b) Dense nanowire. (c) Sparse nanopyramid. (d) Dense nanopyramid.

4.2.2 Problems with Bottom-up Approach

Historically, we started with the “bottom-up” + “nanowire” approach., thanks to an unexpected discovery of single-crystal GaAs overgrowth on Ge nanowires. However, there are some intrinsic problems with the bottom-up nanowire approach.

a) Au catalyst removal and capillary force

For the Au catalyst VLS growth, the Au catalyst nanoparticles remain in the top tips of the nanowires. However, for most semiconductor devices, Au is a notorious deep-level recombination center and life-time killer for minority carriers, thus they must be completely removed before loading into either MBE or MOCVD growth chambers for device layer growth. Figure 4.2.2.1 illustrates the Au catalyst removal. (a) SEM of as-grown Ge nanowires with Au particles on the tip. (b) TEM bright field image of one as-grown Ge nanowire. (c) TEM bright field image of one Ge nanowire with Au catalyst removed [7].

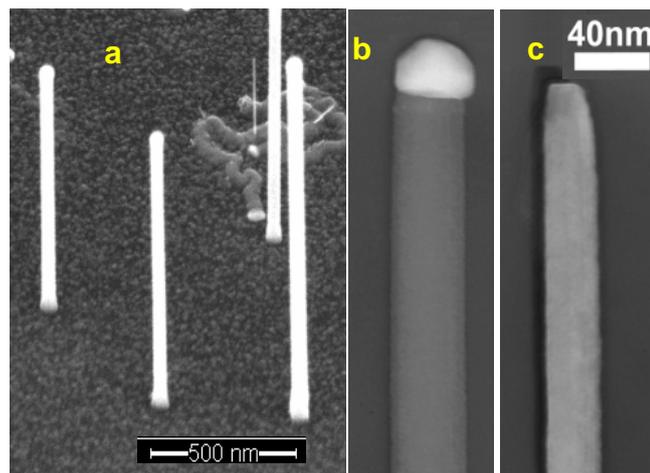


Figure 4.2.2.1 Au catalyst removal. (a) SEM of as-grown Ge nanowires with Au on the tips. (b) TEM bright field image of one as-grown Ge nanowire. (c) TEM bright field image of one Ge nanowire with

Au catalyst removed.

We successfully achieved Au removal using wet etching on the sparse Ge nanowire arrays. These samples are great for material study. However, their sparsity effects the overall efficiency of solar cells fabricated from these nanowires. To make a good filled/empty space ratio, we have grown a dense nanowire array such as Figure 4.2.1.5 (b). After a similar Au catalyst etching process on the sample with dense Ge nanowire arrays, the capillary force of the etchant becomes unfavorable and pulls the long and slim nanowires cause them to become entangled together (shown as Figure 4.2.2.2). The entanglement makes the conformal re-growth of GaAs on nanowire a mission of impossible.

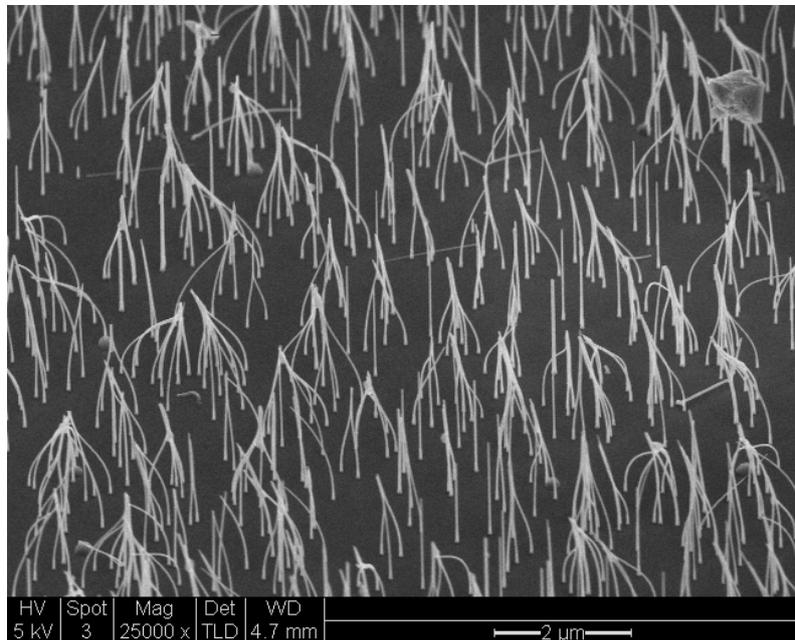


Figure 4.2.2.2. SEM image showing the effect of capillary forces from the Au wet etching solution which entangles the tall and slim nanowires during Au removal..

b) Density and Uniformity

Due to the random nature of the VLS growth process, it is impossible to control the uniformity at the macro scale. Figure 4.2.2.3 shows a SEM top view of a typical Ge nanowire array. The spacing between nanowires varies from a few nanometers to a few microns. This will add abruptness in the GaAs overgrowth, for instance, the regions with dense nanowires will have unevenness when coated with GaAs, while the regions with sparse nanowires will have too much GaAs directly coated on the Si substrate instead of the Ge nanowires. This randomness will certainly effect the overall solar cell efficiency, but even more importantly, it might cause shorting or high leakage current problems in the final solar cell devices.

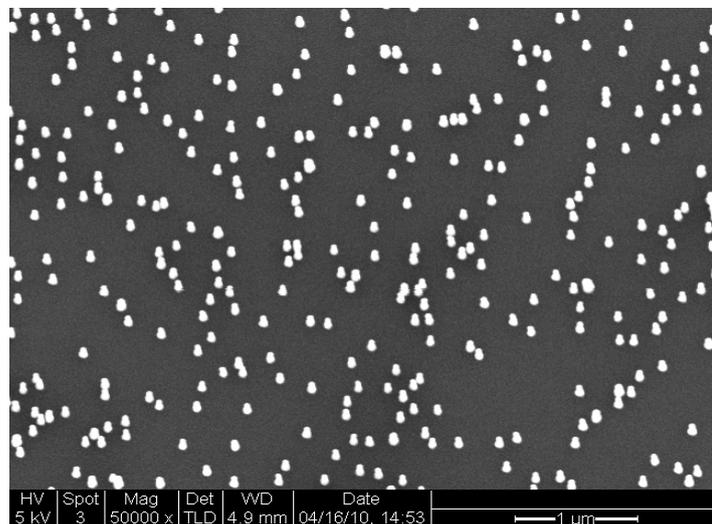


Figure 4.2.2.3 Uneven distribution of Ge nanowires due to the random assembly of the Au catalyst.. The spacing between nanowires varies from a few nanometers to a few microns.

4.3 Top-down Approach

To overcome the intrinsic problems of the bottom-up approach (Au catalysts, capillary force during Au etching, uneven distribution of Ge nanowires in wafer scale), a top-down approach was adapted to make reasonably good efficiency solar cell devices on a wafer scale level. Generally, lithography is used to fabricate ordered nanostructures from bulk material. [11]

Lithography and etching are common tools to make semiconductor integrated circuits, optoelectronics and MEMS (Micro-Electro-Mechanical-System) devices [11]. Electron-beam lithography combined with etching can define features down to sub-10 nm dimensions [12] but the cost is high and the throughput and speed are very low. Photolithography is a possible choice, but it is still too expensive for making low-cost solar cells [13]. In order to reduce the cost of solar cell fabrication, we adapted a “smart nano-lithography” method originally developed in Professor Yi Cui’s group [14].

Ching-mei Hsu, Yi Cui, et al in the paper [14] report a technique known as natural lithography [15][16], using chemically synthesized nanospheres as masks for patterning different dimensions and shapes of particles and pillars [17]. The advantage of this approach is that nanospheres can assemble into close-packed arrays. The spacing and diameter can then be tuned with nanoscale control by etching. [14]

Before Ching-mei Hsu’s work, spin coating was usually used to prepare single or multiple layers of nanospheres. While spin coating is quick and cost-effective [18][19], the resulting monolayer of nanospheres does not uniformly cover large surface areas, but

rather forms domains, even within the domains, the nanospheres are not close packed everywhere. Ching-mei Hsu and her co-workers in Yi Cui's group at Stanford exploited the Langmuir-Blodgett (LB) method [20][21][22] to assemble nano-particles as a mask for reactive ion etching (RIE) for fabricating nano-pillars with uniform coverage over an entire 4 inch wafer [14]. The demonstrated precise control over a wide range of diameters and spacings are very practical and cost-effective for our nanostructured, low cost and high efficiency III-V solar cells.

As in this paper, Figure 4.3.1 shows the general fabrication process for making the Si nanopillars. First, SiO₂ nanoparticles were synthesized in-house, were monodispersed into a close packed monolayer on a Si <100> wafer using the LB method as illustrated in Figure 4.3.1 (a), the monodispersed SiO₂ particles with diameters from 50 to 800 nm were produced by a modified Stöber synthesis process. [23]. Before LB assembly, SiO₂ particles were modified with aminopropyl methyl-diethoxysilane so as to terminate them with positively charged amine groups and prevent aggregation. Second, the diameter and spacing of the nano-particles were tuned by selective and isotropic RIE of SiO₂ as shown in Figure 4.3.1 (a). The etching is based on fluorine chemistry using a mixture of O₂ and CHF₃. This shrinking step also removed the native oxide from the Si substrate, facilitating further etching. Third, Si nano-pillars were formed by a Cl₂ based selective and anisotropic RIE of the Si substrate, as shown in Figure 4.3.1 (c). The diameter and spacing of the nano-pillars were determined by the initial nano-particle size and both SiO₂ and Si etching times. Finally, SiO₂ particles at the tips of pillars can be selectively

removed by etching with hydrofluoric acid (HF), as shown in Figure 4.3.1(d).

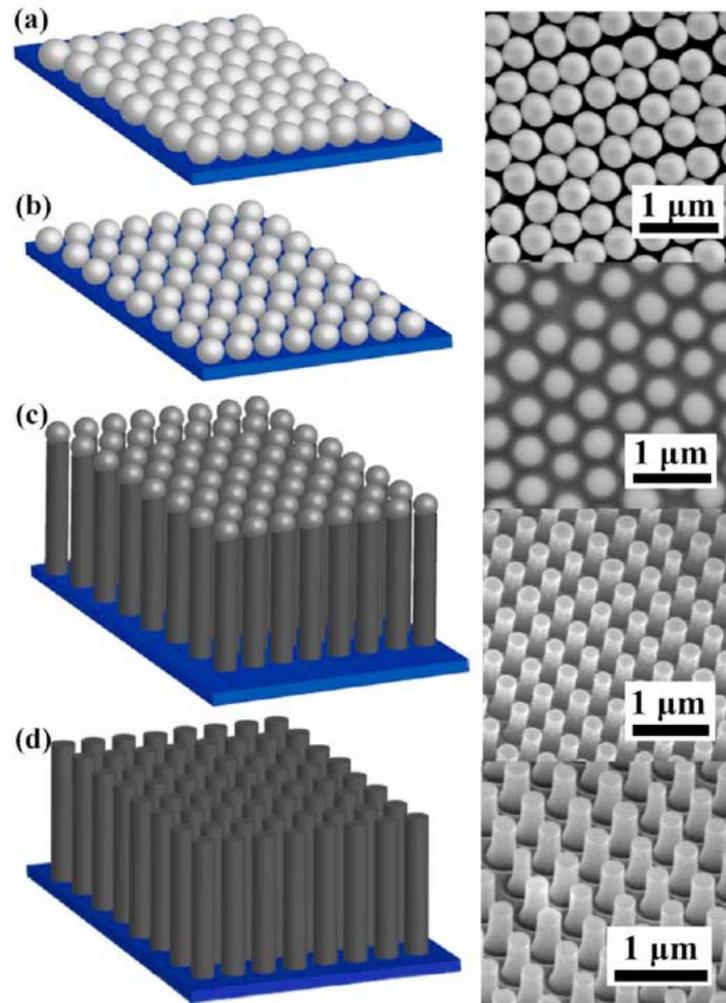


Figure 4.3.1 Ching-mei Hsu's paper [14] describes the fabrication process of Si nanopillar arrays. (a) Deposition of the silica nanoparticles by LB process [20]. (b) Shrinking of the mask by isotropic RIE of SiO₂. (c) Anisotropic etching of Si into pillars by RIE. (d) Removal of the residual mask by HF etching.

The technique developed by Ching-mei Hsu and co-worker in Professor Yi Cui's group is very practical and cost-effective for large-scale applications. However, most

work is on Si substrates. For this dissertation research of nanostructured III-V solar cells, we learned from Yi Cui's group about the nano-sphere coating, but developed our own recipes and technical know-how for Ge and GaAs substrates. Each step is described in the following section

4.3.1 Nano-sphere Mask

a) Langmuir-Blodgett Method

The **Langmuir-Blodgett Method** is known to be a reliable technique to prepare a monolayer of nanoparticles uniformly over a large area [20][21][24]. A Langmuir-Blodgett trough is a laboratory apparatus that is used to compress mono-layers of molecules on the surface of a given subphase (usually water) and measures surface phenomena due to this compression. It can also be used to deposit single or multiple monolayers on a solid substrate. [24]

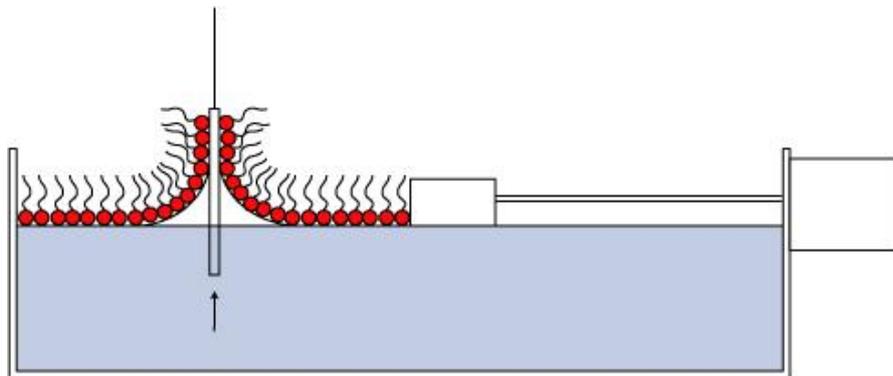


Figure 4.3.1.1: Monolayer transfer onto a substrate after film compression. The substrate is moving from bottom to top and is hydrophilically coated because the polar head groups adhere to the surface.

One important characteristic of this LB approach is that hexagonal, close-packed monolayers of nanoparticles can be produced on a wafer-scale within a short 60 min LB assembly and deposition [14]. Figure 4.3.1.2 shows a photograph of a 4 inch wafer covered by a monolayer of 200 nm diameter SiO_2 particles. Scanning electron microscope (SEM) images at four random locations far from each other show that a monolayer of particles covers the whole wafer. Although line and point defects exist in the nanoparticle packing, there is no area that is not covered by the nano-particles at a macro-scale.

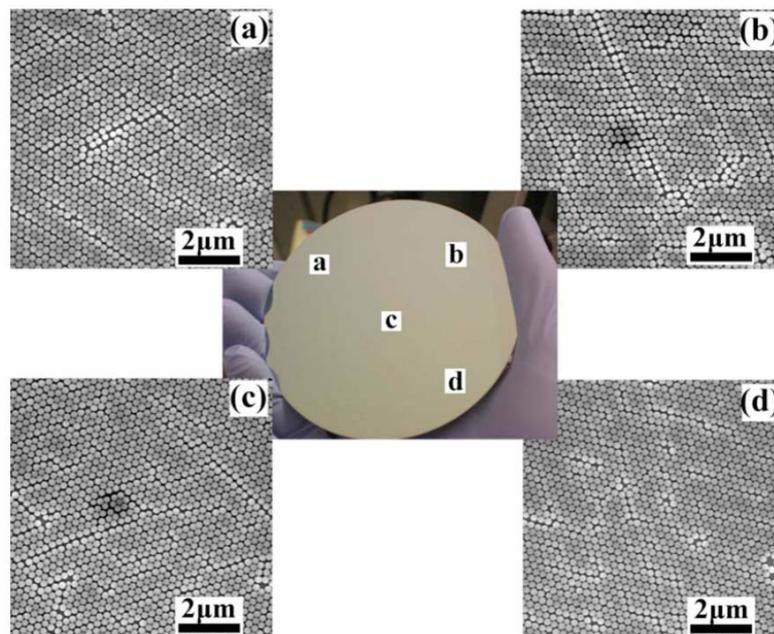


Figure 4.3.1.2 (a)–(d) are SEM images of randomly selected areas at great distances from each other on a 4 inch wafer with nanoparticles deposited by LB.[14]

b) Dip Coating

Dip coating is a popular way of creating thin films for research purposes. The substrate is immersed in the solution of the coating material at a constant speed and then is pulled up and dried. [25] [26]

Figure 4.3.1.3 shows a schematic of the dip-coating apparatus [26]. The trough is filled with an aqueous suspension of silica beads. A silicon wafer is dipped into the solution and then pulled up at a smooth and constant speed to become coated with a close-packed monolayer of silica beads.

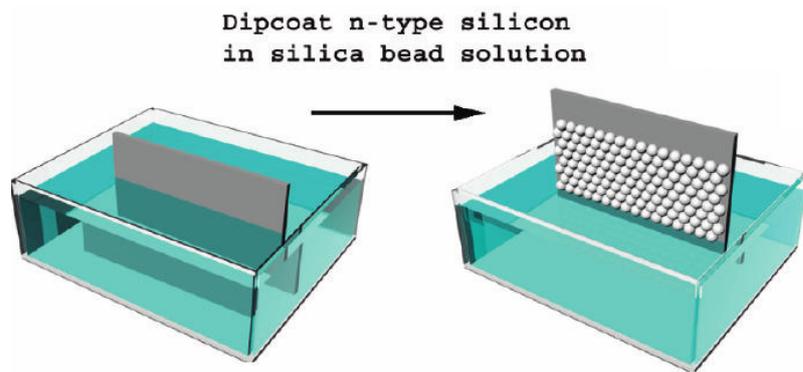


Figure 4.3.1.3 Schematic illustration of the dip-coating apparatus

With delicate control of the concentration, the pull-up speed and the humidity of the ambient on the closed box contenting the dip-coating apparatus, a large-scale monolayer film of nano-spheres can be coated on a Silicon wafer. Figure 4.3.1.4 shows SEM pictures of the close packed monolayer silica nano-spheres at different scales. These monolayer silica nano-spheres will become the natural etching mask for further processing steps: reactive ion etching.

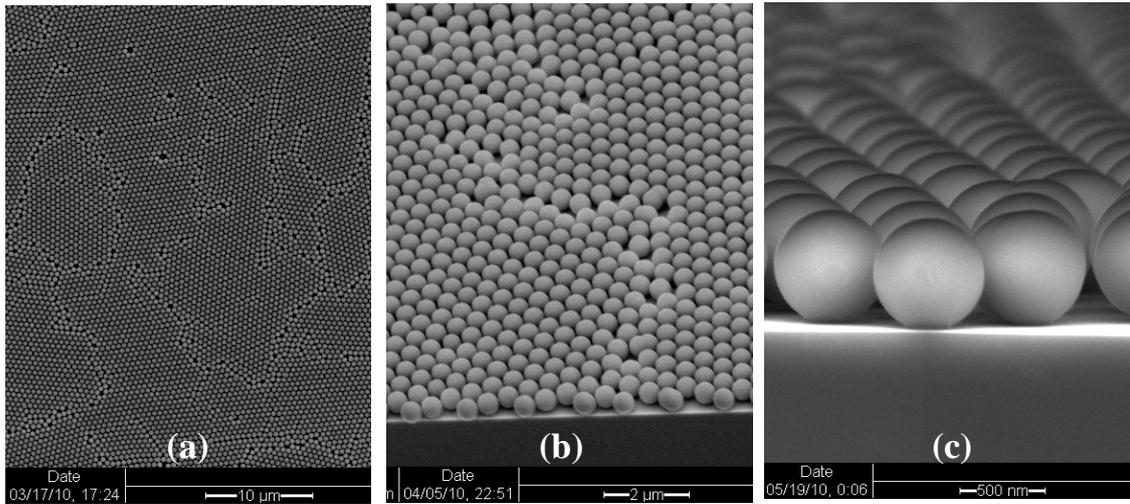


Figure 4.3.1.4 SEM images showing the close packed monolayer silica nano-spheres which serve as an etching mask. (a) (b) (c) shows different scales.

4.3.2 Reactive Ion Etching

Reactive ion etching (RIE) uses a chemically reactive plasma to remove material deposited on wafers. The plasma is generated under low pressure (vacuum) by an electromagnetic field. High-energy ions from the plasma attack the wafer surface and react with it. [27]

We adapted the nano-sphere “natural lithography” technique developed in [14] but replaced the silicon substrate by a germanium (Ge) substrate. We use the AMT etcher in Stanford Nanofabrication Facility [30], with standard recipes to etch SiO_2 and Si (similar etch effect on Ge). Parameters of this AMT etcher are listed in Table 4.3.2.

Table 4.3.2 Parameters of AMT etcher

Etcher	Primary Materials Etched	Standard Recipes	Gases available
AMT etcher	SiO ₂ , SiN, Si, PR	Oxide (prog #3), Via Etch (AMSL 0 layer, #4), Si Trench (#1)	O ₂ , CHF ₃ , SF ₆ , Ar, NF ₃

Figure 4.3.2.1 shows reactive ion etching of a Ge substrate for different time durations. One can find the uniformity and density are fundamentally improved compared to the bottom up VLS growth approach shown as Figure 4.2.1.5(a)

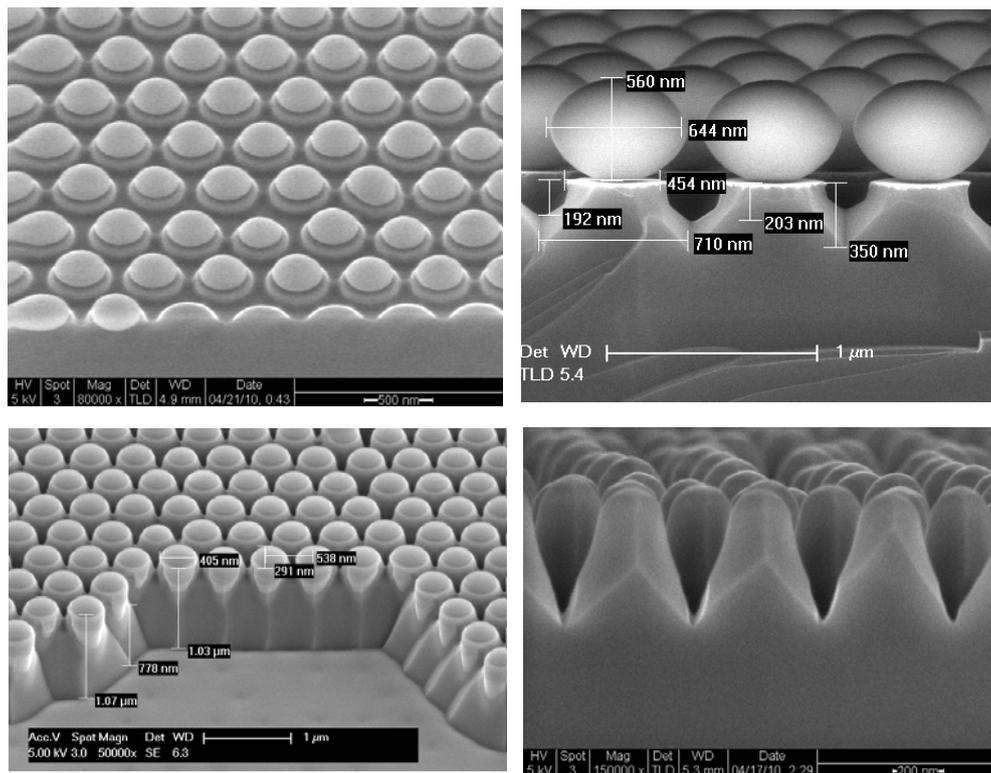


Figure 4.3.2.1 SEM images of a Ge substrate after reactive ion etching for different time duration.

Surprisingly, we found naturally forming nanopyramids during etching of the Ge substrate instead of nano-cones reported in [14][28]. Furthermore, different lattice orientations of the substrates give different shape of nano-pyramids. Figure 4.3.2.2 shows two types of nano-pyramids under SEM after the reactive ion etching with well-controlled parameters. For Ge (100), it forms pyramids with four bottom sides; while for Ge (111), pyramids are of three bottom sides. We will come back to these interesting phenomena in Chapter 5, Material Growth.

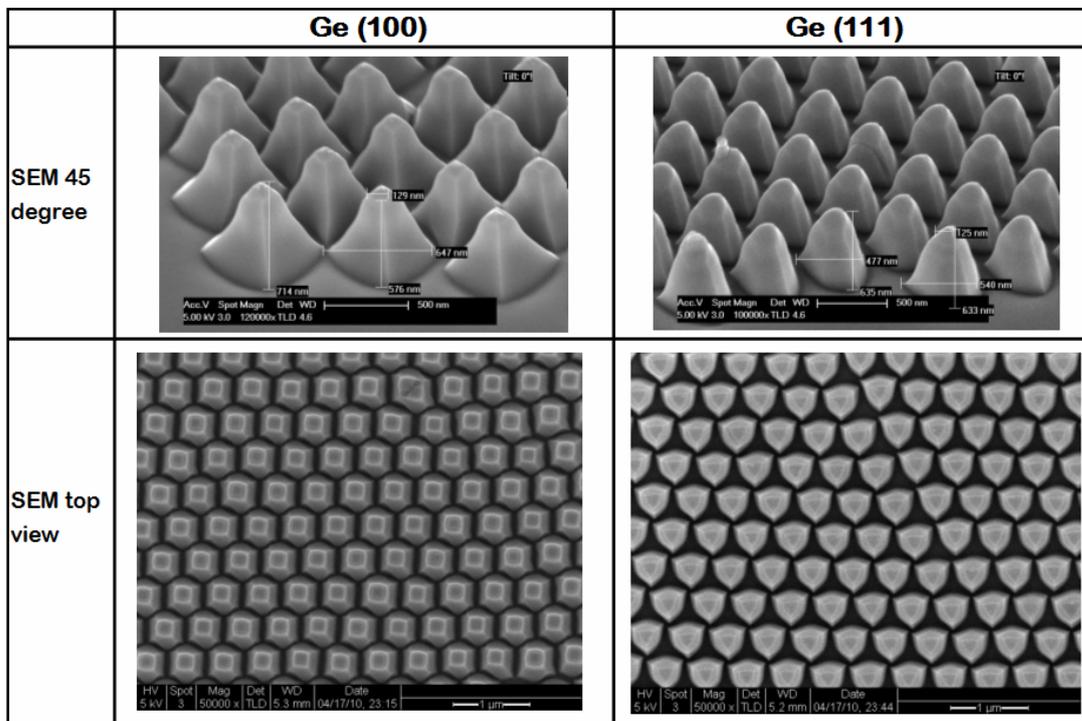


Figure 4.3.2.2 SEM images of Ge (100) and (111) surfaces after reactive ion etching using our recipes, illustrating the different types of nano-pyramids that are formed.

4.3.3 Wet Etching

In order to remove the residual chemicals after reactive ion etching and to smooth the surface of the templates, we added a step of wet etching in the final template preparation process. Figure 3.4.3.1 shows Ge (100) and Ge (111) nano templates after the wet etching.

We also developed robust etching recipes for preparing Si nano structured templates. Figure 4.3.3.2 shows a set of SEM pictures for Si nano templates as a sequence of RIE and wet etching.

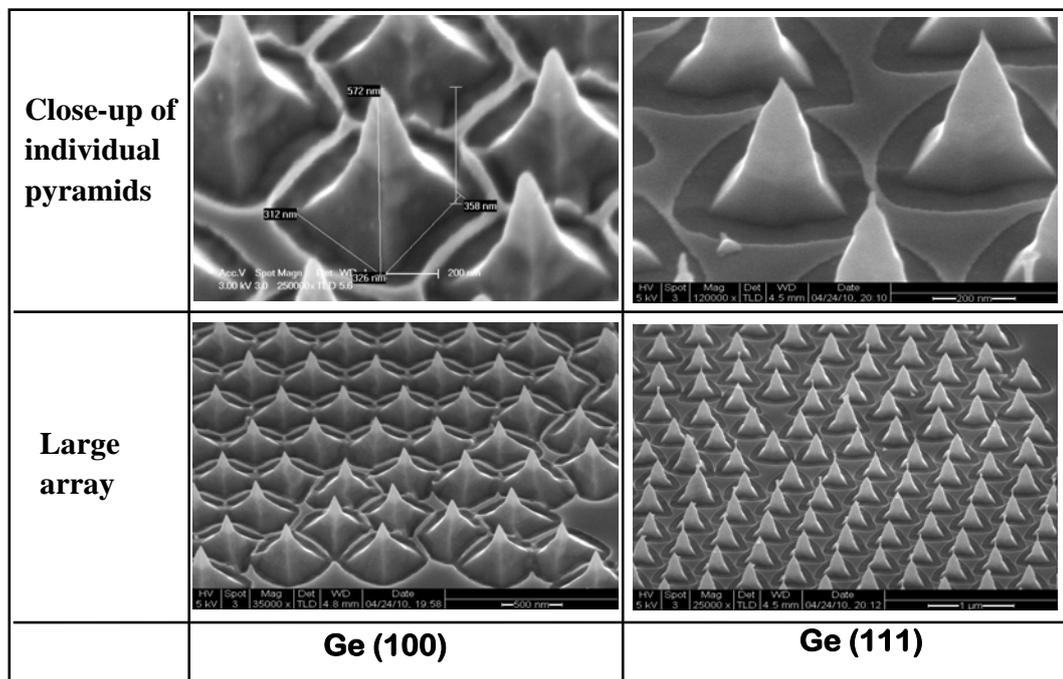


Figure 4.3.3.1. SEM images of Ge (100) and Ge (111) nanostructured templates after wet etching

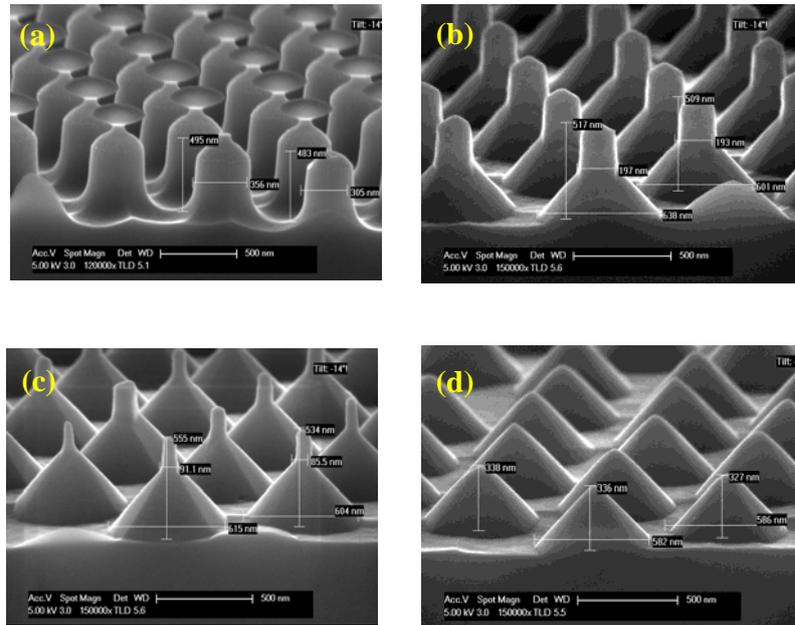


Figure 4.3.3.2 SEM images illustrating the process of Si nanostructured template preparation. (a) Si nano-pillars formed after RIE; (b) HF etching to remove residual nano-spheres and dry etching chemicals (c) H₂O:KOH:IPA wet etch; (d) Final nano-pyramids in the template.

4.4 Conclusion of Bottom-up vs. Top-down

Finally, using both bottom-up and top-down approaches to make nanowire/nanopillar and nanopyramid/nanocone structures, we compare these in Figure 4.4. The merits of these approaches are summarized in Table 4.4. For the bottom-up approach, it requires metal (Au or other) catalysts, it is hard to control uniformity and coverage and density, thus it's not that great to make solar cell device in wafer scale; while for top-down approach, it does not need any catalysts, it has precise control of uniformity, coverage, density and the shape of the nanostructures, thus it is more suitable to make a solar cell device in wafer scale, although it might require a few more process steps.

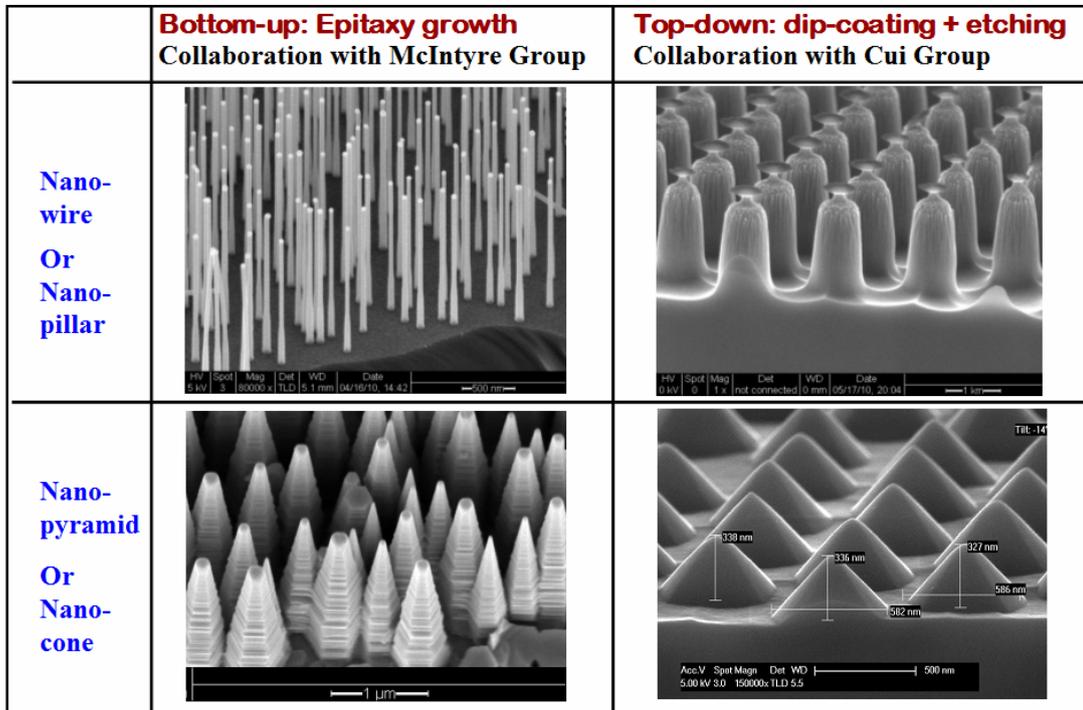


Figure 4.4 Comparison of bottom-up and top-down approaches to make nanowire/nanopillar and nanopyramid/Nanocone.

Table 4.4 Merits of Bottom-up v.s. Top-down

	Bottom-up	Top-Down
Catalysts?	Yes	No
Coverage	Hard to control	Better, wafer-scale
Uniformity	Hard to control	Better, wafer-scale
Process Steps	Less	More
Overall	Hard to make a device	Great to make a device

4.5 Summary

In this chapter, we reviewed the details of our nanostructured template preparation process and analyzed both bottom-up and top-down approaches as potential strategies to produce nanostructure substrates. For the bottom-up approach, VLS (Vapor-Liquid-Solid method) growth of nanowires was first adapted for our exploratory growth experiment and results in good quality of single crystal (details in Chapter 5). However, we also pointed out two intrinsic problems associated with the bottom-up approach.

Then we found the top-down approach is a better alternative. By adapting some innovative nano-sphere mask coating and natural lithography processes on semiconductors developed in Professor Yi Cui's group at Stanford, we fabricated various nanostructures with pitch, spacing, shape, aspect ratio and orientation of facets being well controlled.

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Chapter 5 Materials Growth

Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) or MOVPE, Metal-Organic Vapor Phase Epitaxy, also known as OMVPE, Organo-Metallic Vapor Phase Epitaxy) are the two most common material deposition tools for III-V materials growth. In this Ph.D. dissertation research, we used both MBE and MOVPE for materials growth for the nano-structured III-V solar cells: MBE for proof-of-concept research and prototyping, MOVPE for testing the feasibility of large-scale industrial manufacture.

5.1 MBE

Molecular beam epitaxy (MBE) was invented in the late 1960s at Bell Telephone Laboratories by J. R. Arthur and Alfred Y. Cho [1][2]. It is a powerful technique for epitaxial growth via the interaction of one or several molecular or atomic beams that occurs on a surface of a heated crystalline substrate [3][4]. It utilizes an ultrahigh-vacuum (UHV) ($\sim 10^{-10}$ torr) for epitaxial crystal growth for depositing films with very low impurity levels and abrupt interfaces on the atomic scale [5][6][7][8]. Atomic or molecular beams of various materials are created by evaporating sources which then

impinge on a heated single crystal substrate to form the films. Films of different materials and alloy compositions are synthesized by carefully regulating the temperature of each source material in an effusion cell and by opening and closing shutters covering the sources. [5]

The effusion cells are basically inert crucibles (generally composed of pyrolytic boron nitride, P-BN) heated by a resistive heater to a precisely controlled temperature. The temperature of the source determines the flux of atoms or molecules in the molecular beam and the fluxes in the beams and their incorporation rates into the film determine the composition of the grown material. Growth rates in MBE are generally very low, on the order of 1 μm per hour, which aids in producing material with low defect densities and superb interfacial properties.[5]

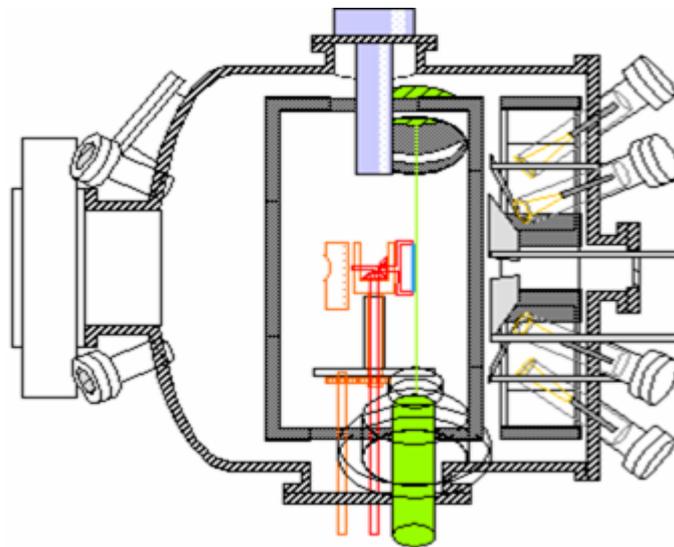


Figure 5.1 A schematic diagram of a MBE growth chamber [3]

A typical MBE system is shown schematically in Figure 5.1 [3]. The solid element

source materials are placed in effusion cells. When heated up to a certain temperature, the III and V materials evaporate from the cells to form a beam of atoms or molecules because of the extremely high vacuum level (10^{-9} - 10^{-10} Torr, ultra high vacuum, or UHV). The substrate is heated to the necessary temperature and continuously rotated to improve the growth homogeneity and uniformity. [3]

Figure 5.2 shows the mean free path for nitrogen molecules at 300K. As shown in the figure, a molecular beam is formed at the substrate surface only under the condition that the mean free path of the particles is larger than the geometrical size of the chamber. This will be fulfilled if the total pressure does not exceed 10^{-5} Torr [3]. Also, the condition for growing a sufficiently clean epilayer must be satisfied, e.g. requiring the monolayer deposition times of the beams, t_b and the background residual vapor t_{res} to satisfy the relationship $t_{res} < 10^{-5} t_b$. Thus, UHV is the essential environment for MBE [3].

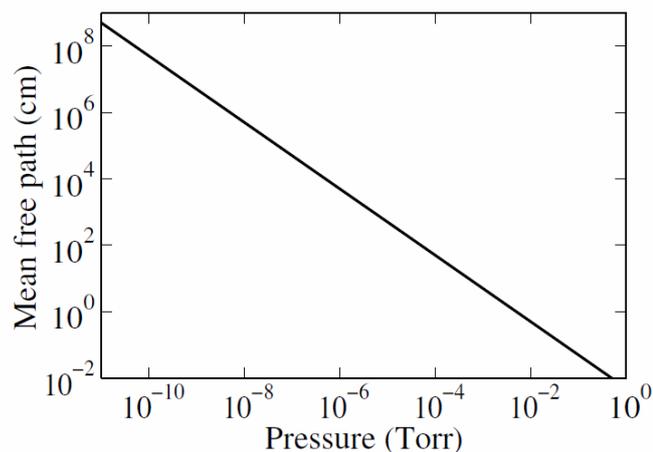


Figure 5.2 Mean free path for nitrogen molecules at 300K [3]

The UHV environment of the system is also ideal for many in-situ characterization tools, like the RHEED (Reflection High Energy Electron Diffraction)[9][10]. The oscillation of the RHEED signal exactly corresponds to the time needed to grow a monolayer of material and the diffraction pattern on the RHEED window gives a direct indication of the state of the surface, as can be seen in Figure 5.3.[11][12]

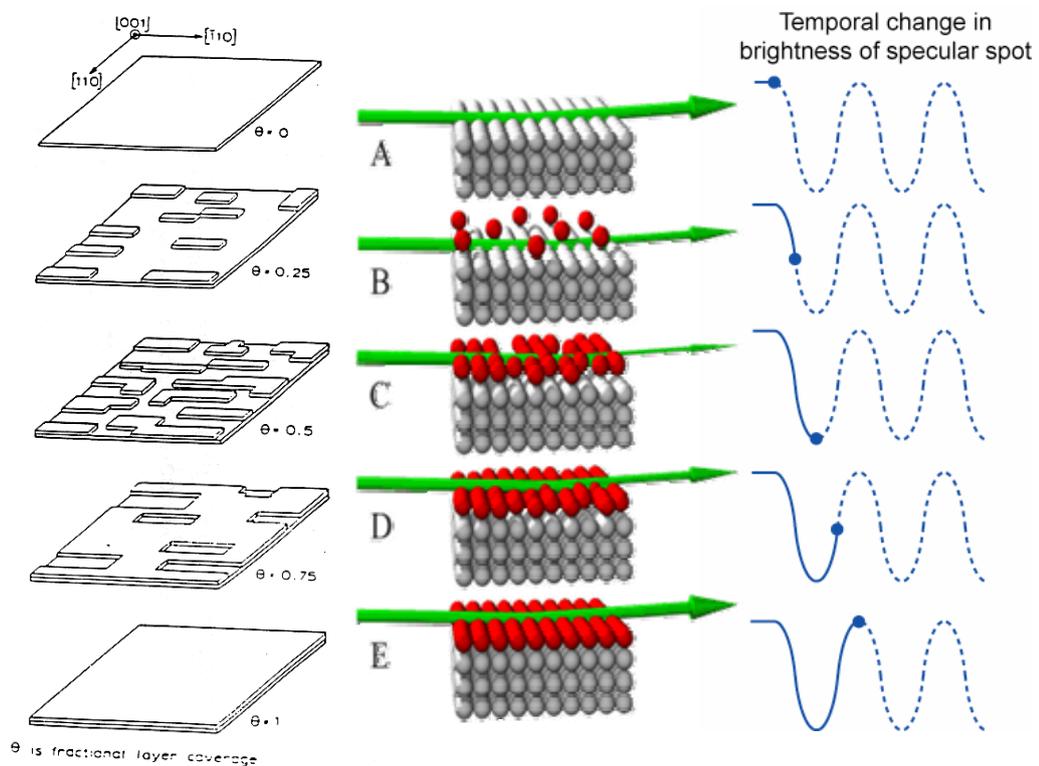


Figure 5.3 Epitaxial surface coverage and RHEED pattern and oscillation corresponding to layer by layer atomic deposition [11][12]

5.2 Surface Kinetics on 2-D Substrate

For III-V epitaxial growth, a lattice matched single-crystal III-V substrate is a necessity to provide as template or seed crystal for subsequent growth [3][5]. There is considerable knowledge available concerning the MBE growth of gallium arsenide,

including Larkins and Harris, 1994 [8], Tsao, 1993 [7], and Herman and Sitter, 1996 [6]. For MBE growth with precise control of atomic layers, the surface kinetics is very important. Figure 5.2.1 shows the surface kinetics for GaAs growth on a 2D (planar) substrate wafer [12].

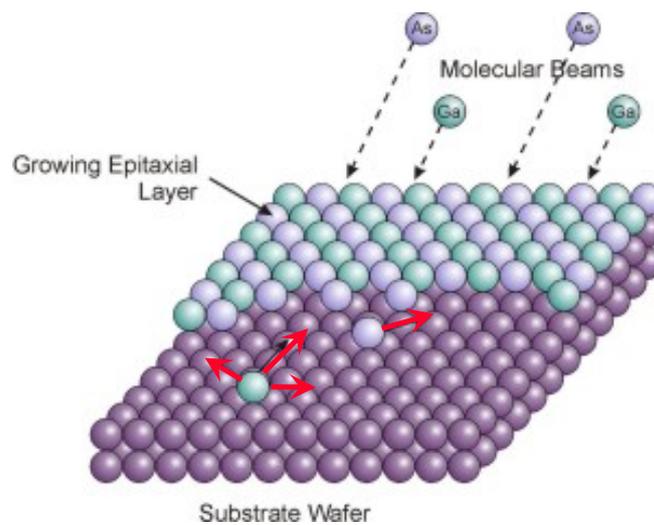


Figure 5.2.1 Surface Kinetics of GaAs grown on a planar substrate [12]

MBE is particularly good for the growth of III-V materials, due to the fact that the growth rate is totally determined by the group III fluxes, provided suitable growth conditions are provided. In other words, the arsenic only incorporates into the film if there is a group III species on the surface with which it can bond. As a result, the AS flux does not require precise control and typically an As flux many times greater than the Ga flux is used, and the resulting film will be highly stoichiometric GaAs. The arsenic incorporation can be improved through the utilization of a cracking cell, which splits the arsenic tetramer, As_4 , into 2 As_2 dimers. These dimers have a higher sticking coefficient than the tetrameric species and therefore prevent the formation of As vacancies or GaAs

antisite defects. The substrate temperature during the growth of GaAs films is roughly 550-650°C [5][6][7][8]

When Ga atoms arrive on the surface of the substrate wafer, they will diffuse around to find the local minimal energy states. The diffusion length is of the order of 100-200 nanometers [13].

5.3 Surface Kinetics on 3-D Substrates

Compared to 2-D (planar) substrates, the surface kinetics on 3-D nanostructured substrates might be substantially different. First, because of the sharp radius curvature in the nanostructure (nanowires and nano-pyramids), the diffusion length of atoms on the tip of the nanostructure might be different from the 2-D planar case. [14]

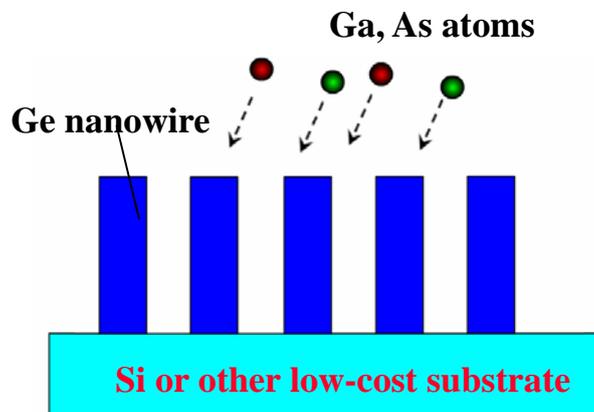


Fig. 5.3.1 Surface Kinetics for MBE growth on a 3D nanostructured template

Second, for this type of 3-D nanostructure growth, in-situ RHEED monitoring is not available in state-of-the-art MBE system. A try-and-error method is deployed here to iterate many times until it converges to the right growth condition. Figure 5.3.2 shows

various growth condition results in all kinds of shapes of GaAs overgrown on Ge nanowires. Fortunately, after fine-tuning the growth temperature, III-V flux ratio and growth rate, etc., we observed high-quality GaAs crystalline material grown on Ge nanowires. [14]

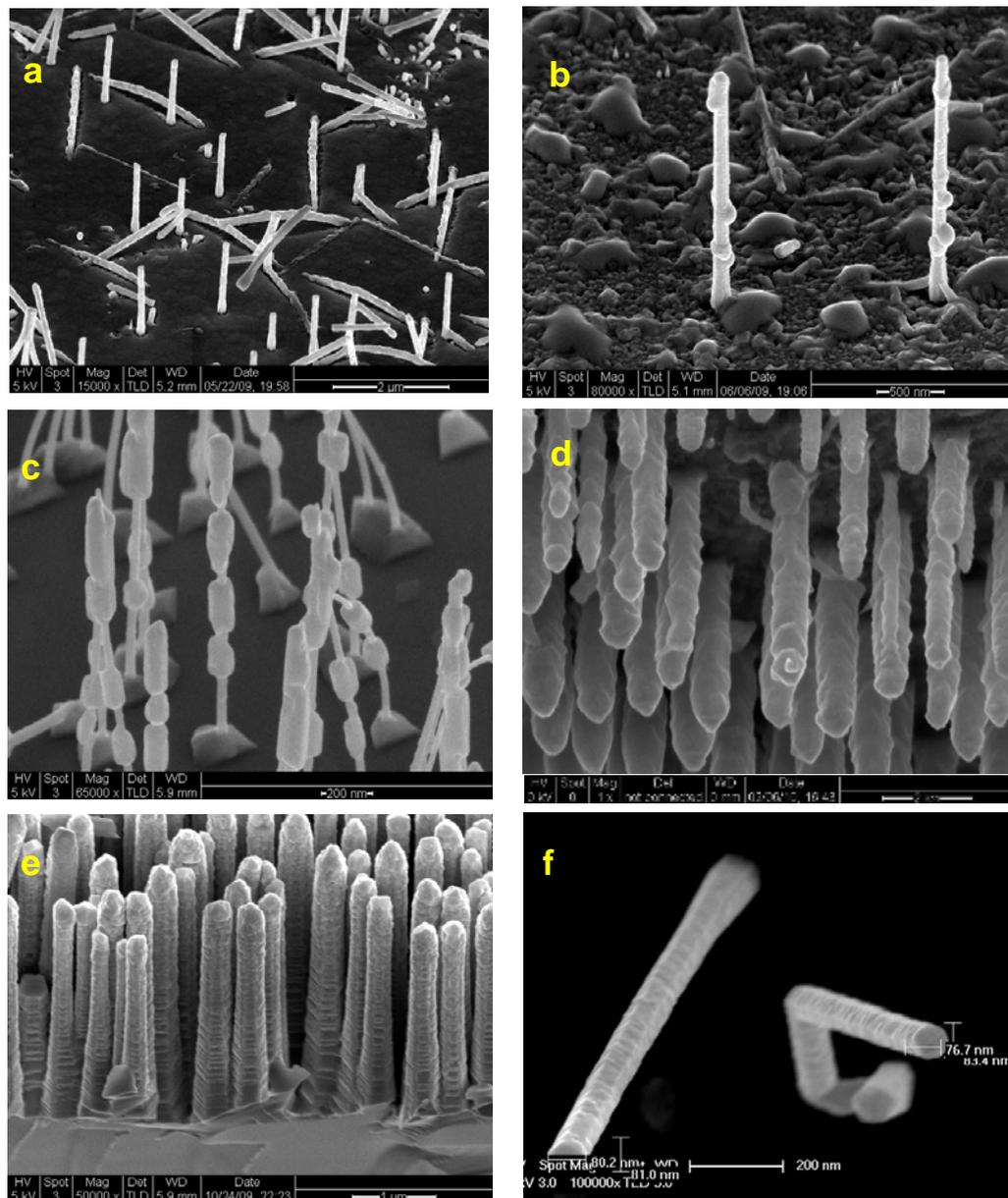


Figure 5.3.2 Types of GaAs/Ge nanostructures observed under various growth conditions. (a)

Nanowires are buried under GaAs “blizzard”; (b) Ga flux is over supplied and nanowires have Ga droplets; (c) Surface clean problems cause the discontinuity of overgrown GaAs on nanowire, forming “ice cream bars”-kind-of shape; (d) GaAs is conformally coated on Ge nanowires, forming “icicle”-kind-of shape. (e) GaAs overgrown on dense Ge nanowire arrays. (f) Good quality GaAs crystal on Ge nanowires by optimizing temperature, flux and growth rate etc.

5.4 MBE Growth of GaAs on 3D Nano-Structure

With trial-and-error experiment and final tuning, we have achieved single-crystal GaAs (and AlGaAs) on Ge nanowires by MBE system in our research group at Stanford University. We grow Ge nanowires on Si substrates via VLS method (Figure 5.4 (a)) and remove the gold catalysts (Figure 5.4 (b)), see details in Chapter 4, Nanostructured Template Preparation, and then epitaxially grow GaAs core-shell structure on the Ge nanowires (Figure 5.4 (c)). Figure 5.4 (d),(e),(f),(g) show clear evidences of single crystal GaAs/Ge core-shell structure. [15]

The Ge nanowire template (Figure 5.4 (a)) is first dipped in gold removal etchant and cleaned in 1:50 HF and DI water, and then loaded in to a Veeco Gen II MBE system with solid Ga source and crackers for As. The sample is first baked at 350°C to remove all the water vapor and then loaded into growth chamber where the base pressure is at 10^{-10} Torr range. Ge oxide is blown off around 500°C (thermocouple reading) for 5 minutes. After

that, GaAs is grown at $0.3\mu\text{m}/\text{hour}$ with As overpressure around 400°C . The result is shown in Figure 5.4(c)(d)(e). The perfect Ge nanowire (111) crystal and sharp radius curvature enhance surface mobility and thus allow us to achieve a good single-crystal GaAs shell coated outside Ge nanowire. Clear single-crystal hexagonal GaAs (shell) / Ge (core) nanowire (or nanopillar) is obtained.

Figure 5.4 summarizes the clear evidence of this single-crystal GaAs/Ge nanostructure. (a) is as-grown Ge nanowire template via VLS prepared in Chapter 4. (b) is Ge nanowires after Au removal, there are no contrast difference on the tips and the tips are sharper comparing to (a) because of the effective wet etching removed off Au catalysts. (c) is SEM 45 degree view image of the overgrown GaAs (shell) on Ge (core) nanowire by MBE. (d) is SEM top view image of the GaAs core-shell nanostructure, showing a beautiful hexagonal shape. (e) is TEM bright field image of the nanowire tip with clear facets. This feature will be utilized in the simulation session because of the facets. (f) is TEM high resolution image, showing a single-crystal lattice arrangement. (g) is TEM SAED (Selected Area Electron Diffraction), a direct evidence that this GaAs/Ge core shell structure is single-crystal.

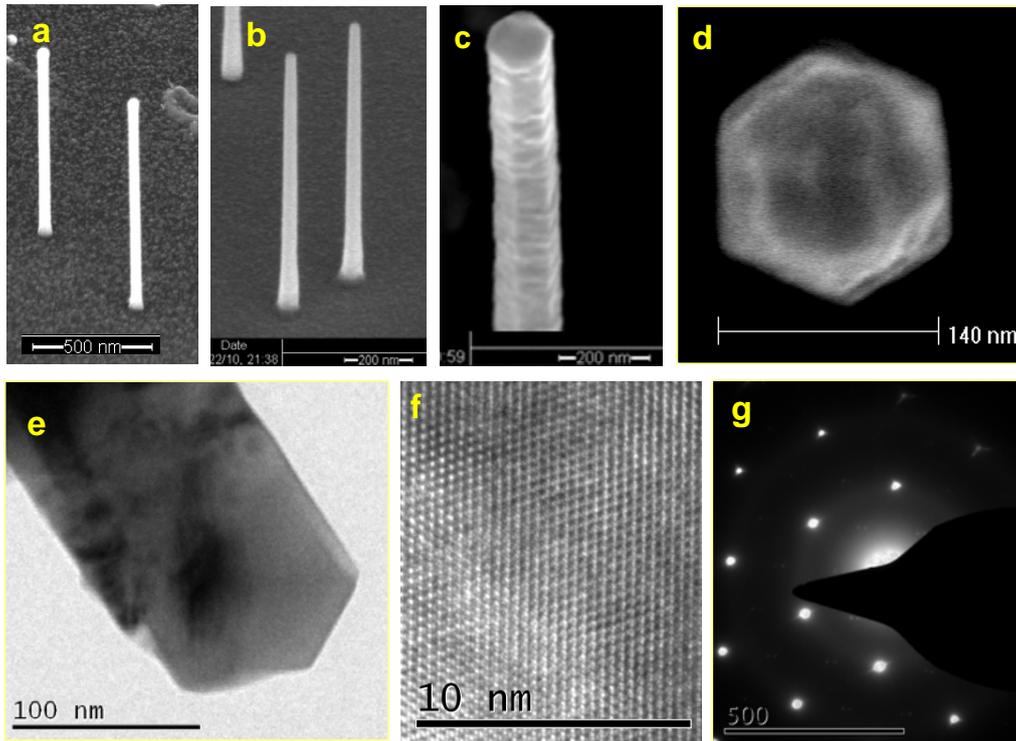


Figure 5.4 SEM images of MBE grown single-crystal GaAs on Ge nanowires. (a) As-grown Ge nanowire array via VLS method. (b) Ge nanowire after Au removal. (c) Overgrown GaAs (shell) on Ge (core) nanowire by MBE. (d) SEM top view of the GaAs core-shell nanostructure. (e) TEM bright field image of the nanowire tip with clear facets. (f) TEM high resolution image. (g) TEM SAED (Selected Area Electron Diffraction).

5.5 MBE Growth Rate for Nanostructures

In MBE growth, it is critical to know the growth rate on a highly non-planar structure. We built a mathematic model and derive the MBE growth rate for nanowires and nano-pyramids sidewall. [16]

Nanowire

We derive the ratio of growth rate on the nanowire side wall r_s vs. the growth rate

on the bottom planar substrate r_b , which is:

$$\frac{r_s}{r_b} = \frac{\tan \Phi}{\pi} \quad (\text{Equation 5.5.1})$$

where Φ is the angle between the Ga flux and the axis of nanowire [16].

We measured the thickness on the SEM pictures to verify that this formula is consistent with the experiment result.

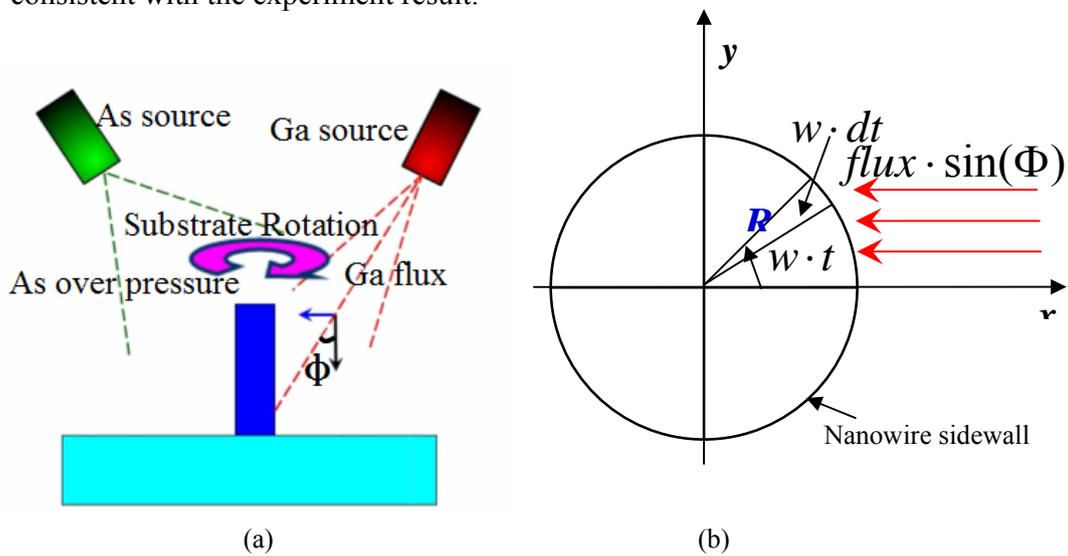


Figure 5.5.1 Derivation of GaAs growth rate on Ge nanowire sidewall. (a) Schematic of GaAs overgrown on 3D nanostructured template (nanowire) (b) the physical model of rotation of the nanowire (with substrate) and the Ga flux. [16]

Generalization in Nanocone / Nanopyramid

In order to generalize the formula so it also apply to nanocone or nanopyramid case, we derive the ratio of growth rate of nanocone side wall r_s over the growth rate of the bottom substrate r_b , which is:

$$\frac{r_s}{r_b} = \frac{(\sin \Phi \cdot \cos \theta + \pi \cdot \cos \Phi \cdot \sin \theta)}{\pi \cdot \cos \Phi} \quad (\text{Equation 5.5.2})$$

where Φ is the angle between the Ga flux and the axis of nanowire, θ is the cone angle as indicated blow.

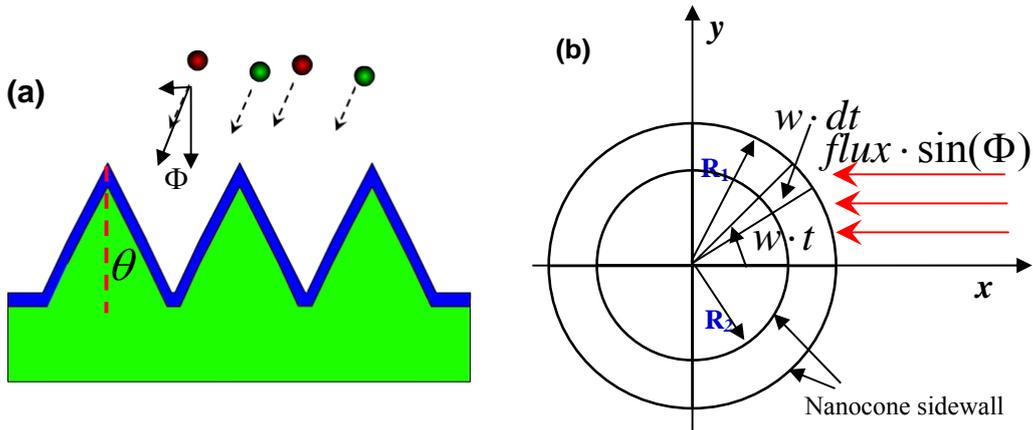


Figure 5.5.2 Derivation of GaAs growth rate on Ge nanocone/nanopyramid sidewall. (a) a schematic of GaAs overgrown on 3D nanostructured template (nanowire or nanopyramid), side view. (b) The physical model of rotation of the nano-cone with substrate and the flux of Ga. [17]

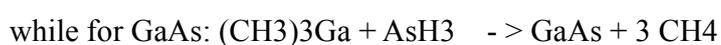
To test the formula with extreme scenarios, we set $\theta = 0$ degree, which is corresponding to nanowire structure, the Equation 5.5.2 becomes the same as Equation 5.5.1. We set $\theta = 90$ degree, which is corresponding to planar structure. $r_s/r_b = 1$. We measured the thickness on the SEM pictures and verified that this formula is consistent with the experiment result.

5.6 MOVPE

Metalorganic vapor phase epitaxy (MOVPE) was initially called Metal-Organic Chemical Vapor Deposition (MOCVD), but came to be known as MOVPE because the

resulting material today is single crystalline. It is also known as organometallic vapor phase epitaxy (OMVPE). MOVPE is a chemical vapor method for growth of epitaxial materials, especially compound semiconductors from the surface reaction of organic compounds or metalorganics and metal hydrides containing the required chemical elements. [18] For example, indium phosphide can be grown in a reactor on a substrate by introducing trimethylindium ((CH₃)₃In) and phosphine (PH₃). Formation of the epitaxial layer occurs by pyrolysis of the constituent chemicals at the substrate surface. In contrast to molecular beam epitaxy (MBE) the growth of crystals is via a chemical reaction and not physical deposition. This takes place not in a vacuum, but from the gas phase at moderate pressures (2 to 100 kPa). As such, this technique is preferred for the formation of epitaxial materials for devices grown near thermodynamic equilibrium, and it has become a major process in the manufacture of optoelectronic devices. [18] Comparing to MBE, another feature of MOVPE is its industrial scale manufacturing and automated mass production capabilities where precise epitaxial layer thickness, doping control and interfaces are not required.[19][20]

Figure 5.6.1 shows the MOVPE growth kinetics and actual photo of a MOVPE system. (a) shows the MOVPE growth reaction for InP and GaAs. (b) and (c) are actual photographs of the gas pipelines /valves and MOVPE growth system.



Other III-V, II-VI, IV, IV-V-VI compound semiconductor materials can be grown in

MOVPE systems as well with the appropriate chemical precursors, see the table below.[18]

Table 5.6.1 Semiconductors grown by MOVPE [18]

III-V	II-VI	IV	IV-V-VI
GaAs, AlGaAs, AlGaInP, AlGaIn, AlGaP, GaAsP, GaN, GaP, InAlAs, InAlP, InSb, InGaN, GaInAlAs, GaInAlN, GaInAsN, GaInAsP, GaInAs, GaInP, InN, InP	Zinc selenide (ZnSe) HgCdTe ZnO Zinc sulfide (ZnS)	Si, Ge Strained silicon	GeSbTe

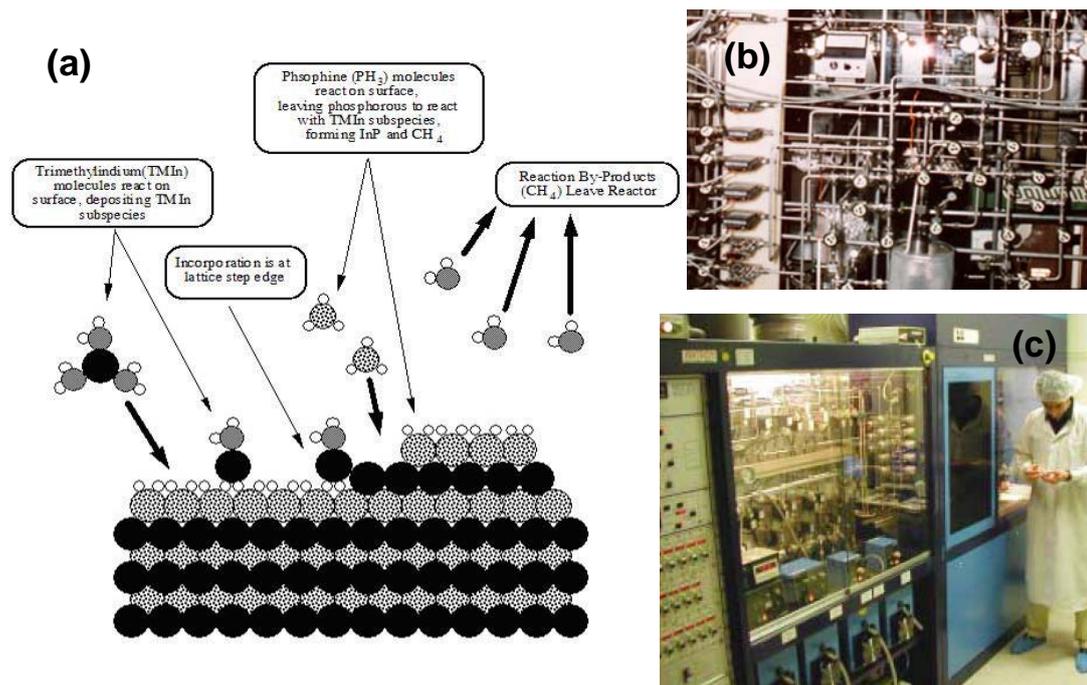


Figure 5.6.1 MOVPE system. (a) Schematic of MOVPE growth kinetics. (b) A photograph of gas pipelines and valves inside a MOVPE system. (c) A photograph of a MOVPE growth system with a technician shows the actual scale.

Based on our extensive experience in MBE growth of GaAs on Ge nanostructures, we quickly achieved single crystal core-shell GaAs growth on Ge nanowires by MOVPE. See table below for the MOVPE recipe.

Table 5.6.2 growth recipe for GaAs on Ge nanowire

<i>Run #.</i>	Material to growth	Pre-growth	growth temp	thickness (nm)	time (s)	pressure (torr)	AsH ₃ (As) (sccm)	TMG(Ga) (sccm)
2649	GaAs on NW	700 Annealing	650	200	500	50	60	23

The result of MOVPE growth of GaAs on Ge nanowires is summarized in Figure 5.6.2. of SEM pictures. (a) is the as-grown Ge nanowire array template prepared in Chapter 4. (b) is Ge nanowire array after Au removal. (c) is MOVPE growth of single-crystal GaAs on Ge nanowire (SEM 45 degree image). (d) is SEM top view of GaAs/Ge core-shell nanowire structure. (e) is the GaAs/Ge nanowire array in micron scale, insert is a close-up picture shows the GaAs/Ge core-shell structure in 500nm scale bar. (f) is the SEM top view of the GaAs/Ge core-shell structure array. Insert is a close-up picture shows the hexagonal shapes and regular facet geometry. The hexagonal facets in (c)(d)(e)(f) are clear evidence of single crystalline material.

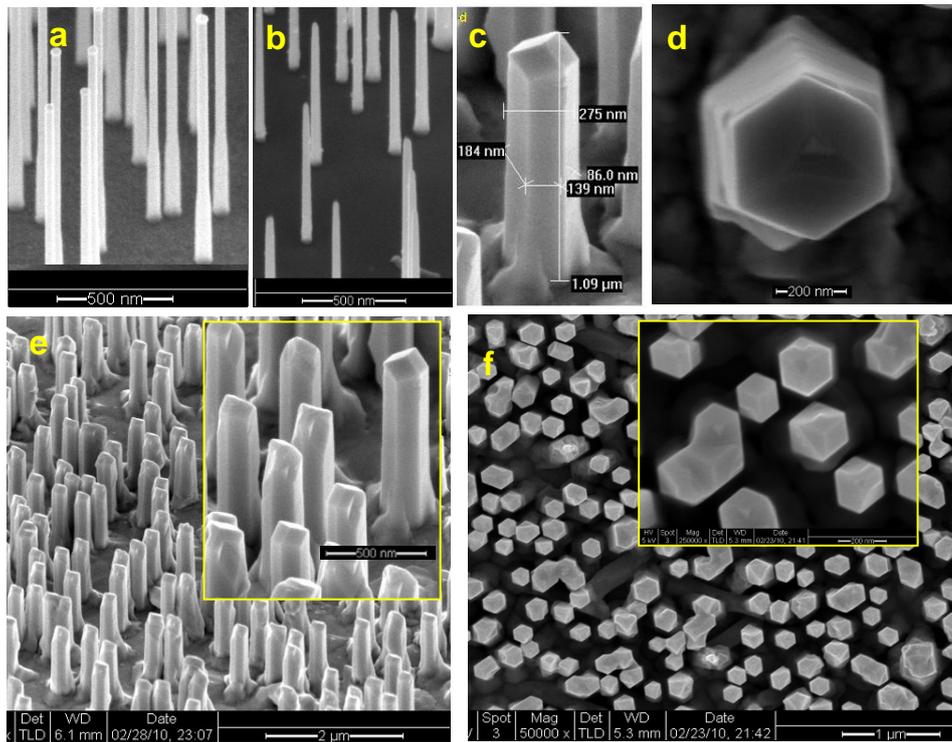


Figure 5.6.2 MOVPE growth of GaAs on Ge nanowires. (a) As-grown Ge nanowire array template. (b) Ge nanowire array after Au removal. (c) SEM 45 degree view of single-crystal GaAs on Ge nanowire after MOVPE growth. (d) SEM top view of GaAs/Ge core-shell nanowire. (e) GaAs/Ge nanowire array in micron scale, insert is GaAs/Ge core-shell structure in 500nm scale bar. (f) SEM top view of the GaAs/Ge core-shell structure array. Insert shows the hexagonal shapes and regular facet geometry in 200nm scale bar.

5.7 Anti-phase Domains in MBE vs. MOVPE

Anti-phase domains (APD) are the regions where the atomic arrangements are opposite to that of perfect a lattice system. [21]. This is very commonly seen in planar growth of GaAs on Ge substrates because GaAs is a polar material while Ge is non-polar material. Figure 5.7 (a) shows APDs in GaAs grown on a planar Ge wafer. The domains are on micron scale. (b) and (c) show APDs in Ge/GaAs core shell structures grown by

MBE under different run conditions. It is clear that the APDs are largely reduced compared to the planar structure. (d) shows GaAs/Ge core-shell nanowires grown by MOVCD with carefully adjusted conditions. The APDs are dramatically reduced.

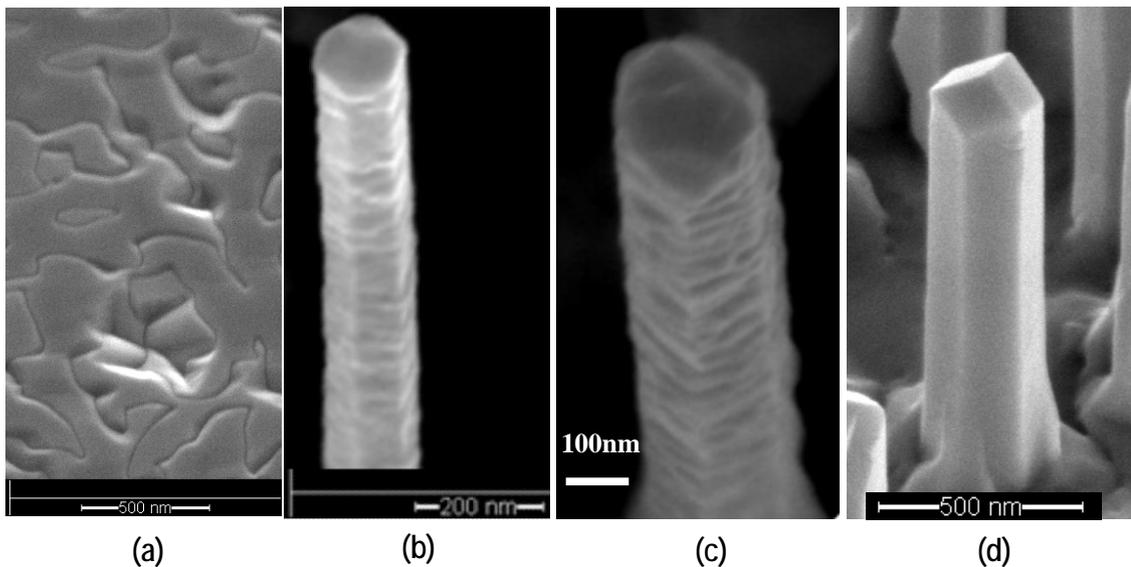


Figure 5.7 (a) Anti-phase Domains (APD) in planar Ge/GaAs structure. (b)(c) Significantly reduced APDs in Ge/GaAs core shell structure, grown by MBE under different growth conditions; (d) dramatically reduced APD in Ge/GaAs core shell structure, grown by MOVPE.

5.8 Two-step Growth on Nano-pyramids

We achieved good quality GaAs overgrown on Ge nanowires by both MBE and MOVPE following trial-and-error iterations. However, for nanocone and nanopyramid structures, more complicated surface conditions make GaAs overgrowth far less straightforward. Nevertheless, the first several runs of low and high temperature growth built up a foundation for future diagnoses. Figure 5.8.1 (a) shows the Ge nanopyramid template just before MOVPE growth; (b) (c) (d) are after MOVPE growth. One dilemma

we observed is shown in (b) which at low growth temperature provides good conformal coating, but poor crystal quality; while (c) and (d) illustrate higher crystalline quality at a higher growth temperature, but much poorer conformal coating.

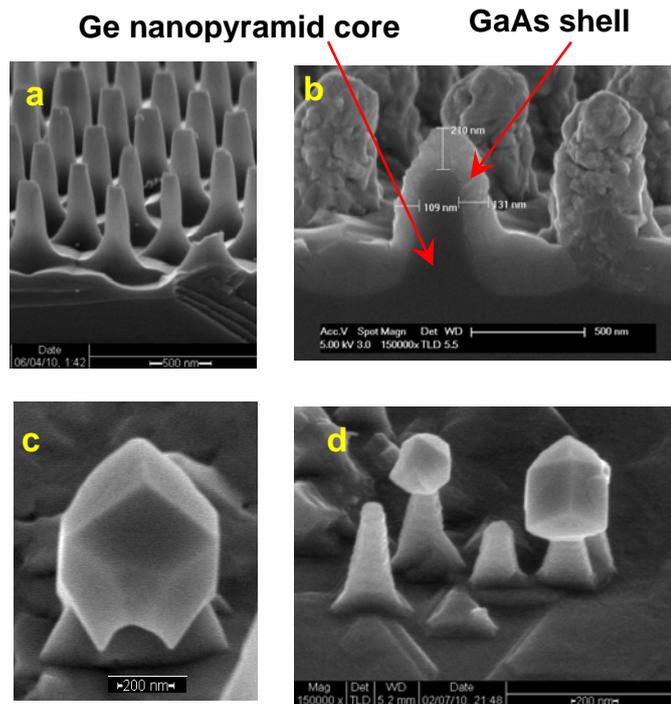


Figure 5.8.1 SEM images of (a) Ge nanostructured template before MOVPE growth. (b) (c) (d) After MOVPE overgrowth. (b) Low growth temperature: Good conformal coating, but bad crystalline quality (c), (d) High growth temperature: Good crystalline quality, but poor conformal coating.

To solve this dilemma, we innovatively developed a “two-step growth” strategy which was very successful. The “two-step growth” strategy combines both high temperature and low temperature growth by carefully adjusting the growth condition for each step: we start with lower temperature to obtain a conformal coating in the first thin shell structure, providing a suitable surface condition for subsequent epitaxial growth and

then we increase temperature to grow a thicker layer to obtain higher quality of single crystal material where the junctions can solar cells will be formed. Table 5.8 gives the detailed “two-step growth” recipe for growing GaAs on Ge nanopyramid by MOVPE. Figure 5.8.2 shows our first conformal single-crystal GaAs/Ge core-shell nanopyramid structure by MOVPE! Figure 5.8.2 (a) shows a SEM of the cross section of a GaAs/Ge core-shell pyramid. (b) shows a SEM 14 degree view of the core-shell pyramid array. Notice how both conformality and single-crystallinity are achieved in Figure 5.8.2 compared to the “one or the other” feature in Figure 5.8.1.

Table 5.8 “Two-step growth” recipe for GaAs on Ge nanopyramid

Run #.	Material	Pre-growth	growth temp	thickness (nm)	time (s)	pressure (torr)	AsH3(As) (sccm)	TMG(Ga) (sccm)
2661	GaAs	700	550	50	200	50	60	23
		Annealing	650	150	300	50	60	23

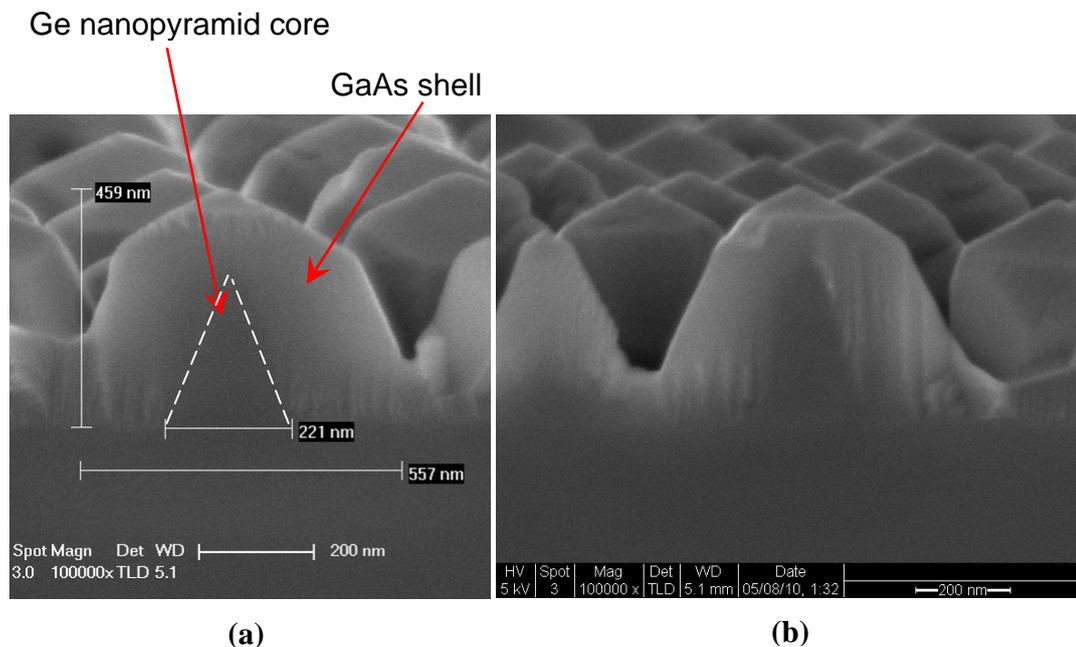


Figure 5.8.2. First conformal single-crystal Ge/GaAs core-shell nanopyramid by MOVPE. (a) SEM of

cross section of a core-shell pyramid. (b) SEM 14 degree view of the core-shell pyramid array. (c) SEM 90 degree view of the pyramids array from [100] (d) SEM 45 degree view of the pyramids array from [110].

Once we became more sophisticated in MOVPE growth and developed the “two-step” recipes, we found some interesting phenomena. Figure 5.8.3 shows a SEM top view of nanopyramid structures after MOVPE growth. The templates are: (a) and (b) Ge (111), (c) Ge (100), (d) GaAs (100). Surprisingly, we found the pyramids are of different geometry! For (a), the pyramid has three bottom edges, while for (b) it has six, (c) and (d) it has four! Even more interestingly, in (d), the growth of pyramid is anisotropic- the top views are rectangles instead of squares, e.g. the length of x and y is different!

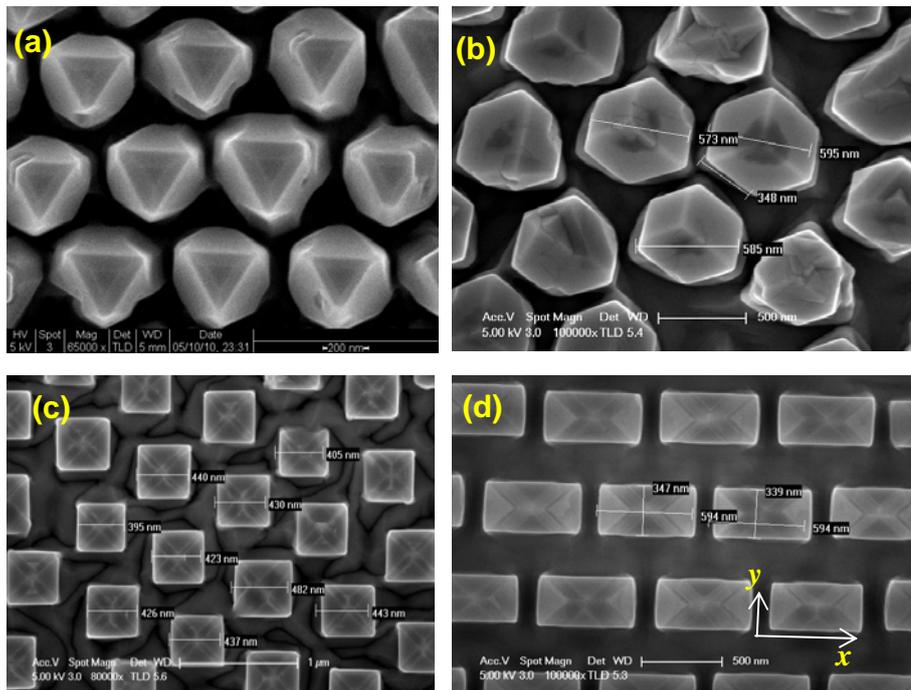


Figure 5.8.3 SEM top view of nanopyramid structure after MOVPE (a) GaAs on Ge (111), (b) GaAs on Ge (111), (c) GaAs on Ge (100), (d) GaAs on GaAs (100).

5.9 Anisotropic Growth of GaAs on Nano-templates

We studied this anisotropic phenomenon of MOVPE growth of GaAs on nanostructured templates [22]. By taking SEM pictures with different sample orientations, all the facets can be identified as shown in Figure 5.9.1. There are a total of twelve facets on each nano-pyramid (Figure 5.9.1.(b)). By symmetry, an identification of only five of these facets (taken from a quarter corner of the pyramid) is sufficient for complete identification of all facets. Once we observe the SEM images and angles where the facet is perpendicular to the plane of view, the facet to be identified forms a line. By measuring the angle between this line and the substrate, the facet can be verified. For example, in Figure 5.9.1 (c), via SEM, we see the structure from the [100] direction, the (110) facet is perpendicular to the plane of view and forms a line. The angle between this line and the substrate is measured to be 45 degrees, which is a verification of a (110) facet. [22]

Figure 5.9.1 summarizes the SEM views from different angles to reveal these anisotropic geometries. (a) shows a GaAs (100) nanostructured template before MOVPE growth. (b) shows a SEM top-view of GaAs nanopyramid structure after MOVPE growth, facet A, B, C are identified as A(111) B (101) C(111) and directions (111), (110), (011), (111),(110) are indicated as well. (c) shows a SEM from [100], facets of A, B, C and direction of (011) are identified according to (a). (d) (e) (f) (g) (h) are SEM from [011], [111], [110], [110], [110], [111], respectively.

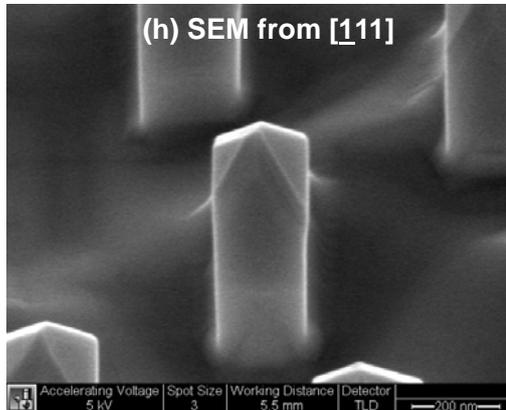
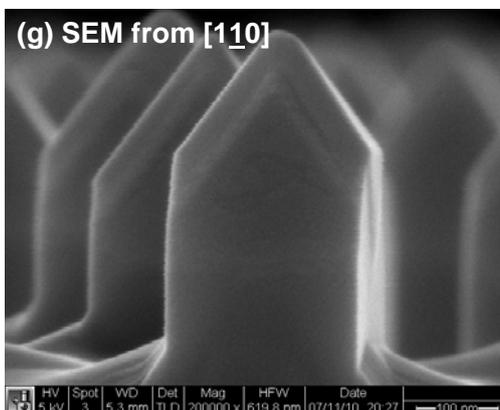
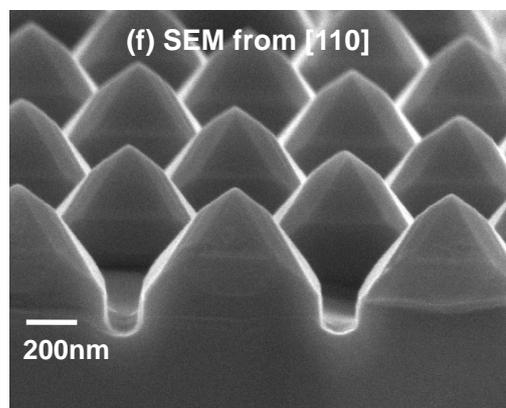
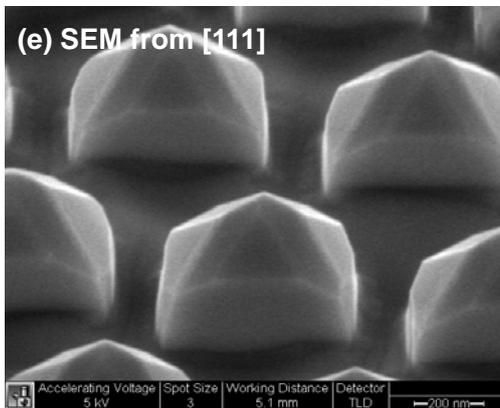
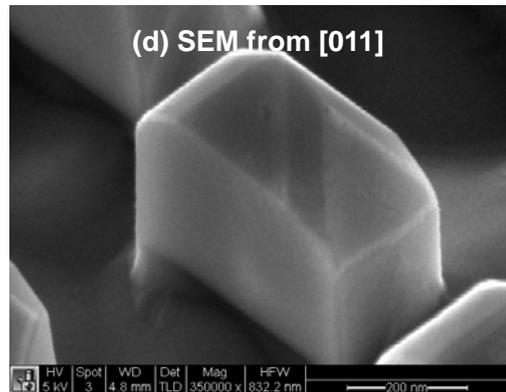
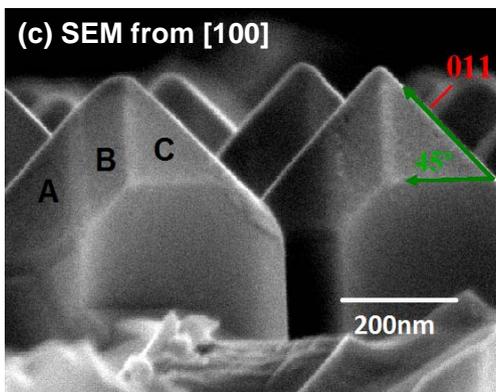
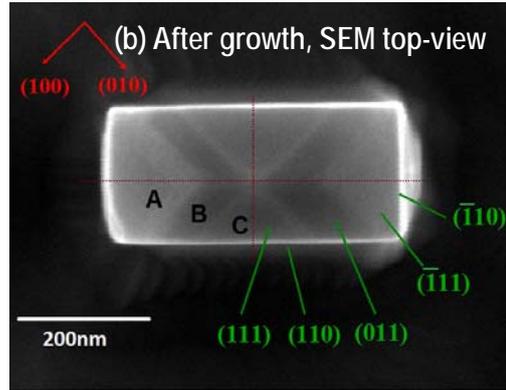
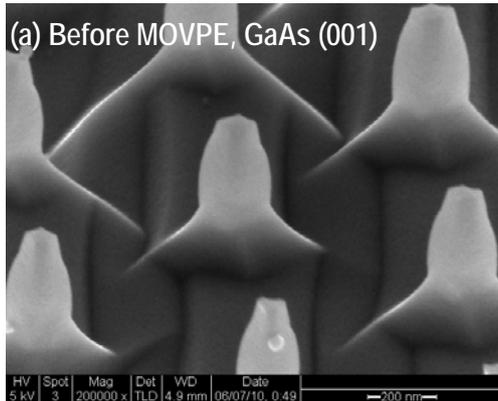


Figure 5.9.1 SEM views from different angles to reveal these anisotropic geometries. (a) GaAs (100) nanostructured template before MOVPE growth. (b) SEM top-view of GaAs nanopyramid structure after MOVPE growth, facets A($\bar{1}\bar{1}$) B (101) C(111) and directions (111), (110), (011), ($\bar{1}\bar{1}$), ($\bar{1}\bar{1}$) are identified. (c) SEM from [100], facets of A, B, C and direction of (011) are marked. (d) SEM from [011], (e) SEM from [111], (f) SEM from [110], (g) SEM from [$\bar{1}\bar{1}$ 0], (h) SEM from [$\bar{1}\bar{1}$ 1].

The rectangular shape from the top view reveals the lateral anisotropy at the two sidewalls (along [110] and [$\bar{1}\bar{1}$ 0] directions), in other words, the growth rates at these two sidewalls are different [22]. According to Hiromitsu Asai in his paper published in the Journal of Crystal Growth (1987) [23], this anisotropy stems from different Ga and As atomic arrangements and different numbers of As dangling bonds at [110] and [$\bar{1}\bar{1}$ 0] growth step sites [23]. Each Ga atom at the [110] growth step is bonded to two As atoms with three bonds in total, while at the [$\bar{1}\bar{1}$ 0] step, each Ga is bonded to two As with one bond to each. Therefore, under high AsH₃ pressure (more than 6 times of TMG pressure) and low temperature, Ga atoms are more easily bonded to the growth step at [110] and the crystal is growing faster in the [110] direction. However, if under low AsH₃ pressure (in our case) and high temperature, an As atom at a [110] growth step is more easily desorbed because it is bonded to a Ga atom with only one bond. In this case, the lateral growth rate along [110] is slower than it is along [$\bar{1}\bar{1}$ 0]. [23] Therefore, the final shapes of single crystal GaAs core-shell structure can be engineered by adjusting the AsH₃ pressure, TMG and AsH₃ flux ratio and growth temperature. [22]

5.10 Nano Art

Nano Art is “a new art discipline at the art-science-technology intersections. It features nano-landscapes (molecular and atomic landscapes which are natural structures of matter at the molecular and atomic scale) and nano-sculptures (structures created by scientists and artists by manipulating matter at the molecular and atomic scale using chemical and physical processes). These structures are visualized with research tools like SEM (scanning electron microscopes) and AFM (atomic force microscopes) and their scientific images are captured and further processed by using different artistic techniques to convert them into artworks showcased for large audiences.”[24]

We delightfully found numerous examples of nano-art in this Ph.D. dissertation project. To demonstrate the happy marriage of science and beauty, Figure 5.10.1 presents SEM pictures of our solar cell devices and certain steps in our nano-fabrication compared to real world architecture in macro-scale; Figure 5.10.2 (a) shows “nano sushi”- an inspiring SEM picture occurring in “natural lithography”, (b) shows a “nano candle”- a broken tapered nanowire on the background nanowire array of a SEM top-view picture.

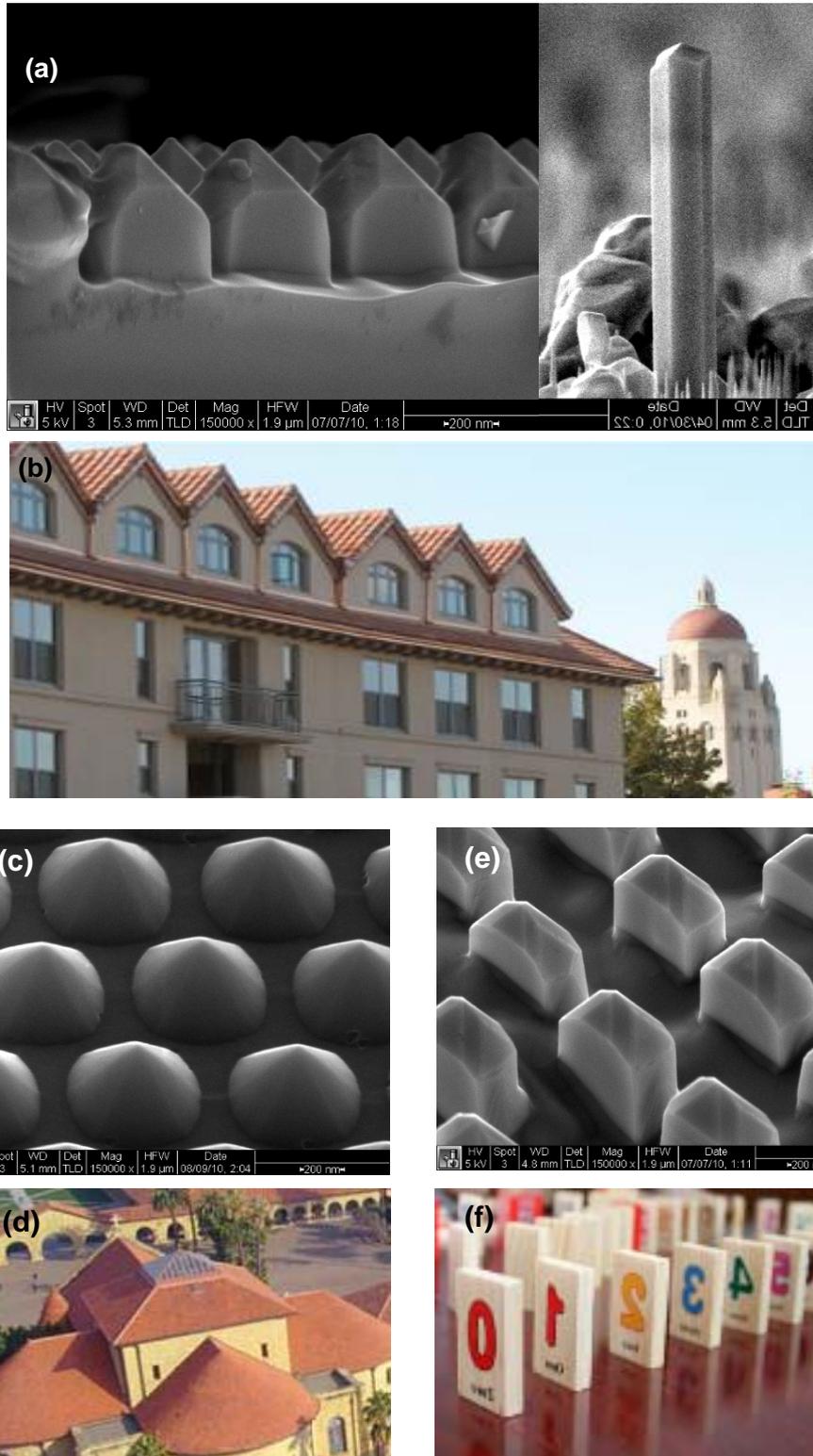


Figure 5.10.1 Nano-art: nanostructures and real world architecture. (a) GaAs nanopillars and one

standing-alone nanowire. (b) Munger graduate student housing and Hoover Tower at Stanford University [25]. (c) Nanocone of Silicon wafer after “natural lithography” and wet etching (in Chapter 4). (d) The roof of Stanford Memorial Church [26]. (e) Anisotropic MOVPE growth of GaAs on GaAs (100) nanostructured template. (f) A toy Domino set.

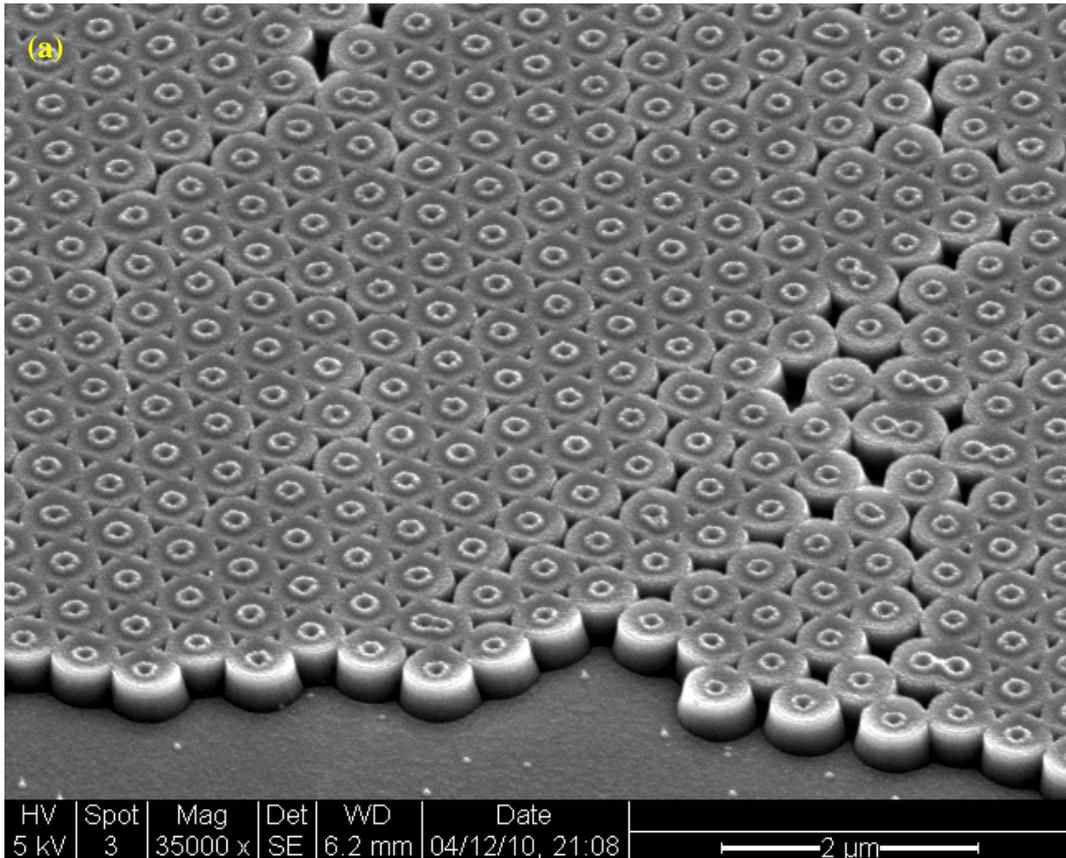


Figure 5.10.1 Nano-art: “nano sushi”- an inspiring SEM picture during “natural lithography”

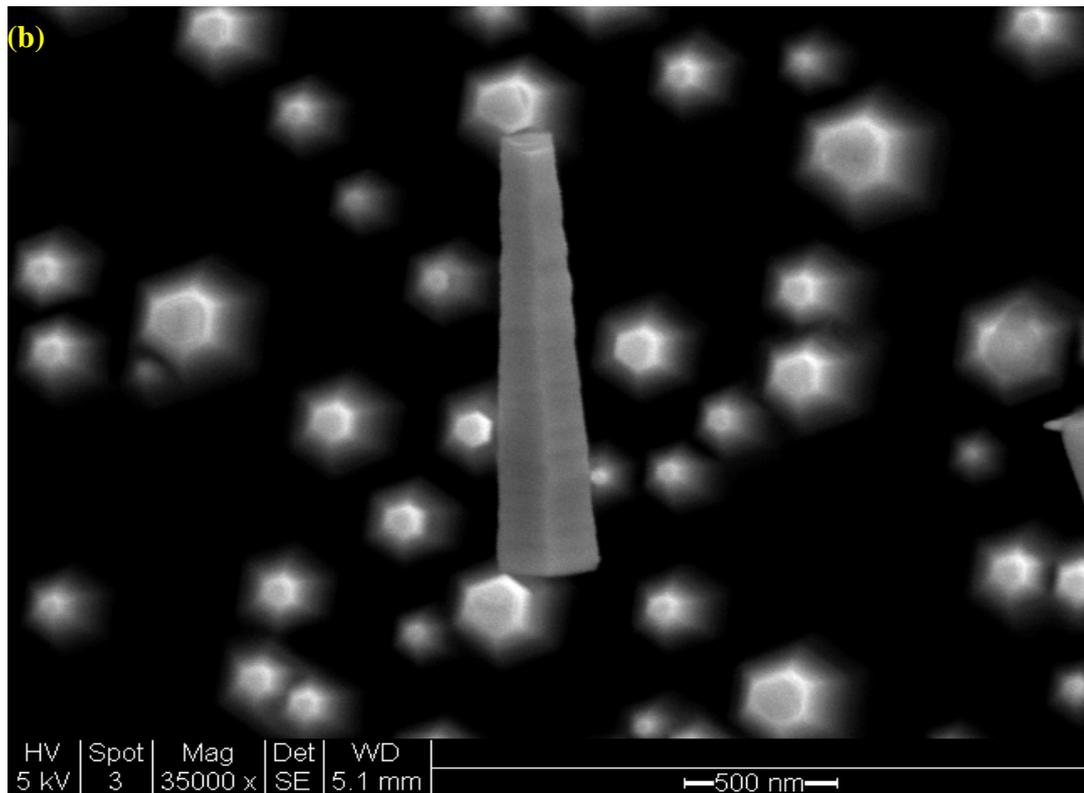


Figure 5.10.2 “Nano candle”- a broken tapered nanowire on the background nanowire array of SEM top-view picture.

5.11 Conclusion of MBE vs. MOVPE

The comparison of MBE and MOVPE for this particular dissertation research is summarized as Table 5.11 below.

Table 5.11 Comparison table of MBE and MOVPE

	MBE	MOVPE
Single Crystal?	Yes	Yes
Material Quality	Good	Great
Anti-Phase Domain or defects under SEM	Still observable	Dramatically reduced
Maintenance	Used to be "Mostly Broken Equipment"	Regular routine
Cost	Used to be expensive	Reasonable
Overall	Good for research and prototyping, rapid development in III-V solar cell era	Good for large-scale industrial manufacture

5.12 Summary

This chapter highlights the materials growth for nanostructured III-V solar cells. We first overviewed the fundamentals of MBE and MOVPE and presented the growth results of single-crystal GaAs on 3-D nanostructures, including nanowires and nano-pyramids. For the first time, we derived equations for the growth rate for nanowire structures and generalized these to nano-cone or nano-pyramid structures grown by MBE.

In this dissertation research project, MBE is an excellent tool for research and prototyping a proof-of-concept device, while MOVPE is currently more widely used in industry for mass production. We have developed mature recipe for single-crystal GaAs overgrowth on nanowire with both MBE and MOVPE, and innovatively developed a

“two-step growth” process for growing GaAs on Ge nanopramids and GaAs nano-pillars by MOVPE. We succeeded in demonstrating this strategy by verifying by both good conformality and good single-crystalline quality nanostructures.

We also studied the phenomena of anisotropic growth of GaAs on GaAs (100) nano-templates and found a reasonable explanation for it.

This chapter lays a solid foundation for device fabrication described in chapter 6.

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Chapter 6 Device Fabrication and I-V Characterization

6.0 Overview

After materials growth, the final step is to fabricate devices and measure their I-V characteristics. We fabricated the solar cells in the Stanford Nanofabrication Facility (SNF). Both ITO (Tin-doped Indium Oxide), finger metal contacts and Cu nanowire transparent contacts have been investigated for making the electrodes to collect photocurrent in nanostructured solar cells. We overcame the current shorting and shunting problems which always exist in nanostructured solar cells. A final I-V characteristic showed that solar-electric conversion efficiency of the nanostructured solar cell is improved over the planar solar cell grown under the same conditions and same thickness of optical absorbing layer.

6.1 ITO and Metal Pad

Indium tin oxide (ITO, or tin-doped indium oxide) is one of the most widely used transparent conducting oxides for solar cell contacts. ITO is a solid solution of indium (III) oxide (In_2O_3) and tin (IV) oxide (SnO_2), typically 90% In_2O_3 , 10% SnO_2 by weight. [1]

ITO has two attractive properties: high electrical conductivity and good optical transparency. A compromise has to be reached during its film deposition, a high concentration of charge carriers will increase the conductivity of the material, but

decrease its optical transparency [1].

Thin films of ITO are most commonly deposited on surfaces by electron beam evaporation, physical vapor deposition, or a range of sputter deposition techniques. We used an AJA sputtering system to deposit conformal ITO layers on the Ge/GaAs nano pillars. Figure 6.1.1 (a)(b) present clear SEM pictures showing the conformality and uniformity of ITO deposited on GaAs/Ge nanopillars. (a) shows a SEM top view to the dense array, insert is an individual GaAs/Ge nanopillar covered by ITO. (b) shows a SEM 45 degree view of the same nanopillar array, insert is an individual GaAs/Ge nanopillar covered by ITO.

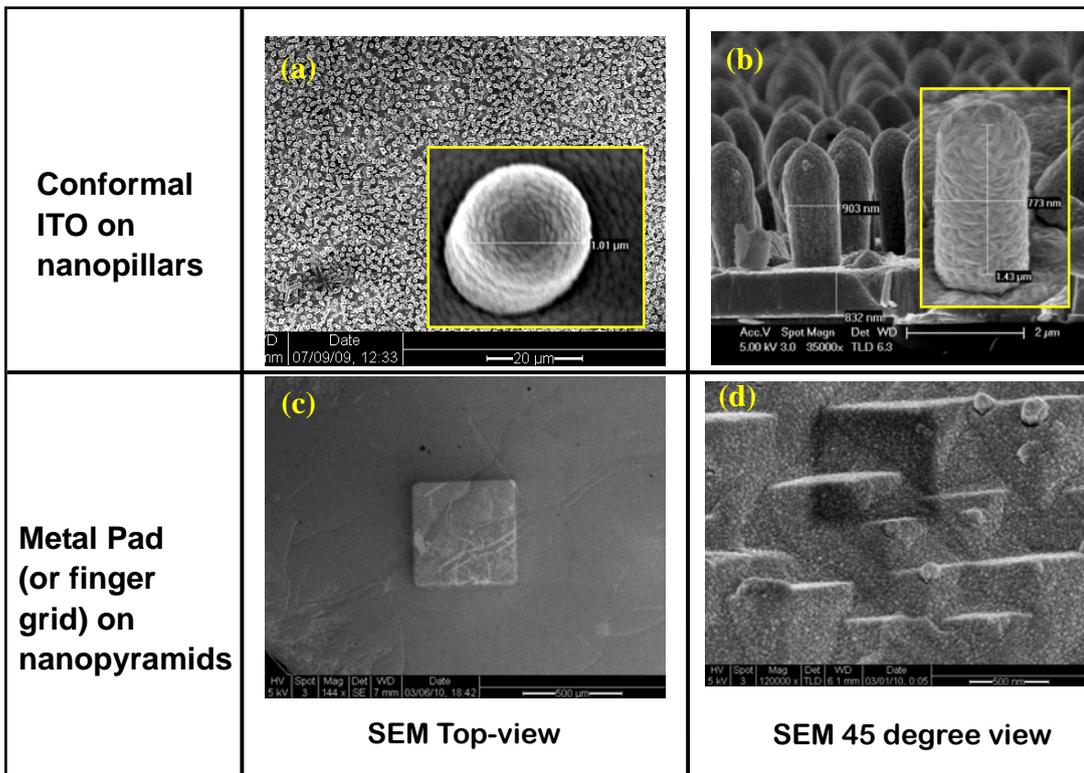


Figure 6.1.1 Conformal ITO deposition on GaAs/Ge nanopillars and metal pad deposition on GaAs nanopyramids.

In order to have a comparison, we also deposited metal pads on the nanopyramid structure. The idea of metal pads is derived from the traditional “metal finger” contact patterns used on solar cells illustrated in Figure 6.1.2 [2][3]. A metal pad might provide better protection of the cells when probed by the sharp needles of the probe station.

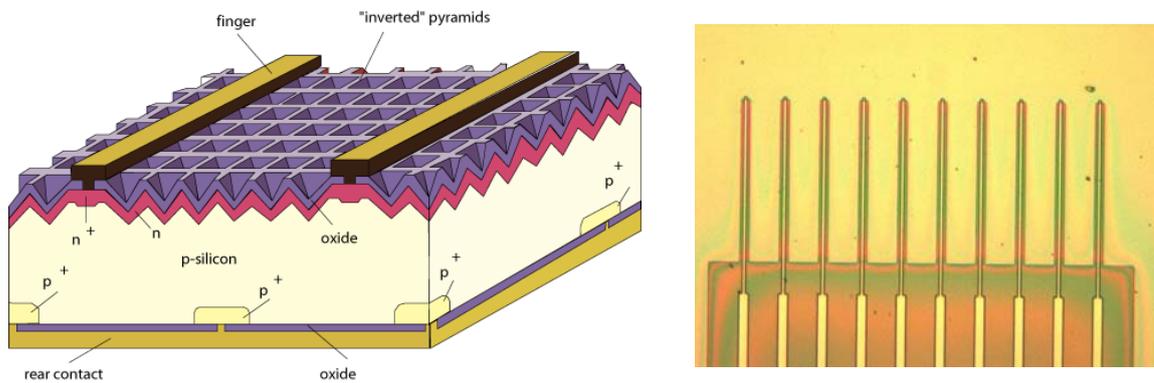


Figure 6.1.1 Metal finger contact. (a) Schematic of the “metal finger” contact for a Si solar cell [2]. (b) A photograph of finger metal mask for lithography [3]

6.2. Leakage/Shorting Problems in Nanowire Solar Cell Devices

For most nanowire solar cells, the I-V curves often exhibit shorting or severe leakage problems. Figure 6.2 shows the measurement results of our first several rounds of solar cell devices. (a) shows the I-V curve of a GaAs/Ge core-shell nanowire solar cell. The large leakage current completely quenches the photovoltaic effect. (b) shows the I-V curve of a GaAs/Ge core-shell nanopyramid solar cell. Over most of the range of voltage sweep, the I-V curve looks like a resistor, because the device is shorted.

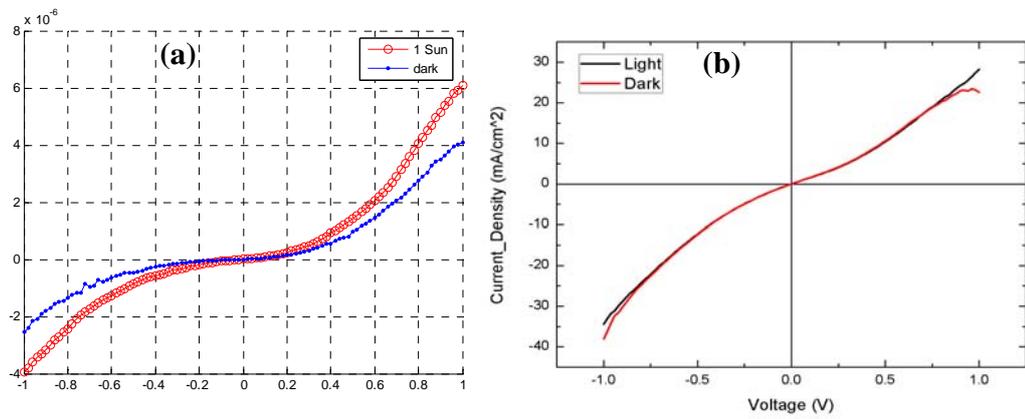


Figure 6.2 Leakage/shorting problems in nanowire solar cell device (a) leakage problems (b) shorting problems.

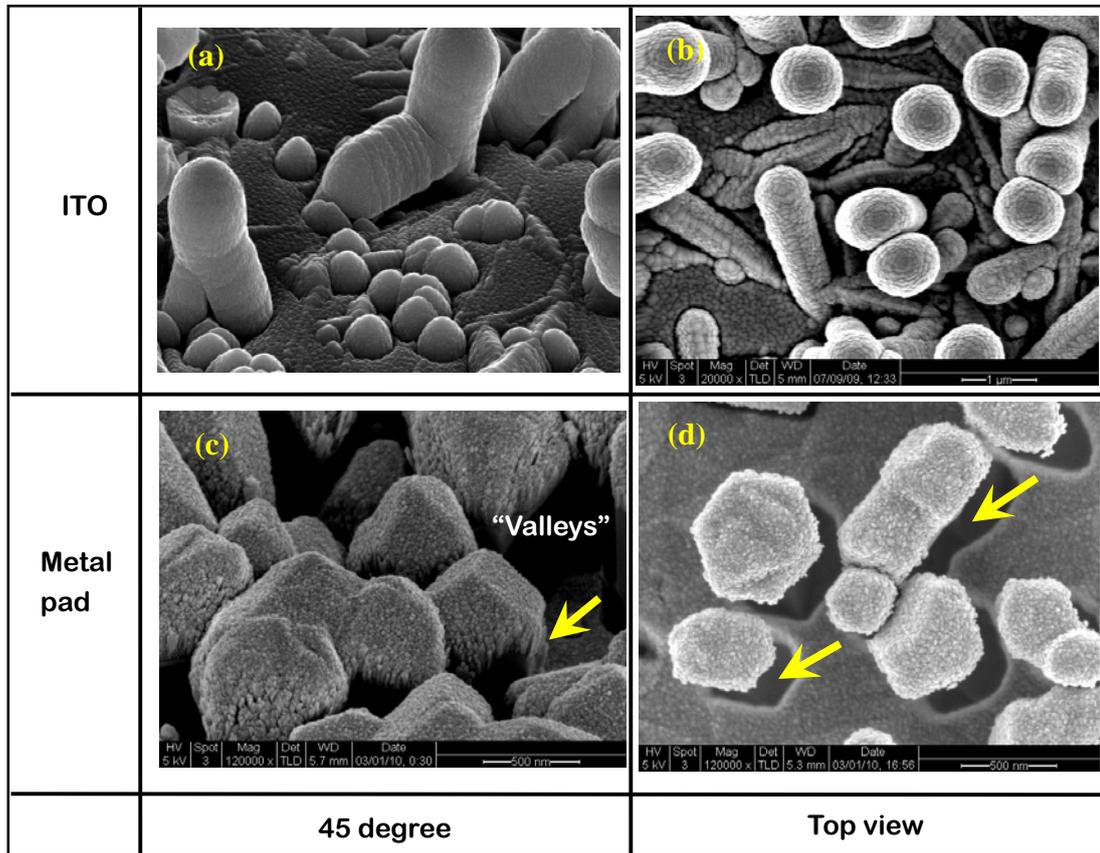


Figure 6.2. Problems with ITO and metal pad deposition

To diagnose this problem, we took more SEM pictures of the solar cells after the

contact/electrode deposition. The reason for the leakage/shorting problems is that part of the deposited contact reaches the bottom of the substrate, so the current does not pass through the path we designed for the solar cell.

For some corner cases, e.g. because of the non-uniformity of nanostructures and deposition variation, the metal or ITO might directly reach substrate with poor epitaxial growth. Figure 6.2 (a) and (b) show this bad coverage of ITO in the nano template with rough surfaces. (c) and (d) show poor coverage of metal contacts in the “valleys” of the nanopyramid template: in (c), metal reaches the substrate (indicated by the yellow arrow), in (d) there are some shadows (indicated by the yellow arrows) aside from the big pyramids.

6.3 Final Device Fabrication

To overcome the leakage/shorting problem, we need to separate the metal contact from the “valleys” of nanopyramid template. As illustrated in Figure 6.3.1, we found the missing link: using PMMA (methyl methacrylate) [4][5][6] as the insulation layer (indicated by red arrow) to prevent metal directly contacting the “valley” and the bottom of the substrates.

Poly (methyl methacrylate) (PMMA) is a transparent thermoplastic, often used as a light or shatter-resistant alternative to glass [4]. It is sometimes called acrylic glass. Chemically, it is a synthetic polymer of methyl methacrylate. The material was developed in 1928 in various laboratories [4][5][6]. The reason we choose PMMA is because its

excellent property of electrical insulation and optical transparency, and liquid enough to be spun-on and provide coverage of the nanostructured template. In addition, PMMA can be etched by being exposed to UV Ozone [5][6], which is well suited when we need to “peel of” PMMA on the tips nanostructure to expose them for metal contacting.

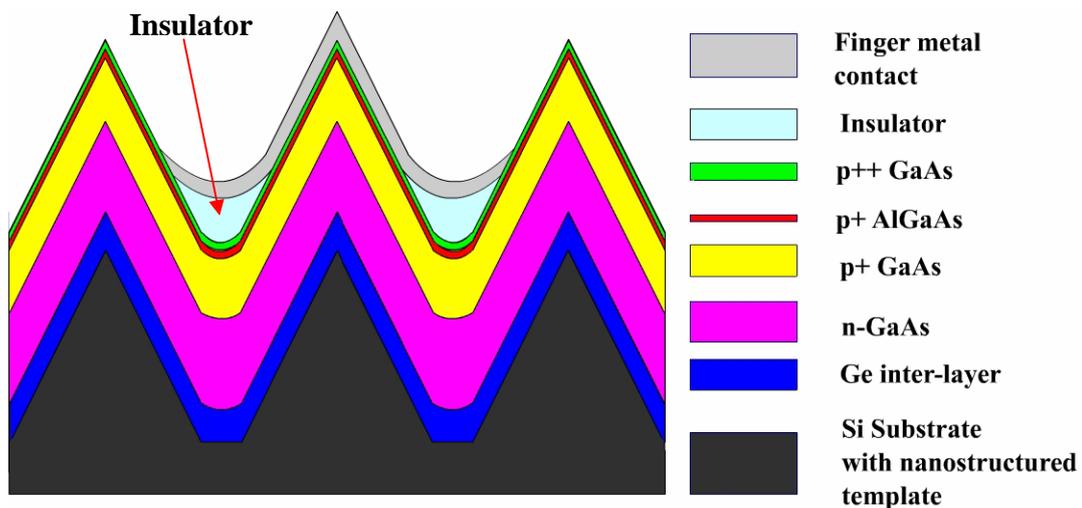


Figure 6.3.1 More realistic device design, modified from chapter 3: inserting an insulating layer between the metal contact and valleys of the pyramid arrays to prevent shorts.

Figure 6.3.3 shows the effectiveness of the PMMA treatment and metal contact deposition. (a) After PMMA treatment, the “valleys” and bottom of the nanopyramid array are fully and uniformly covered by PMMA. (b) Following step (a), the metal deposition gives the final device very uniform metal coverage. There is no metal directly contacting the bottom of the valleys.

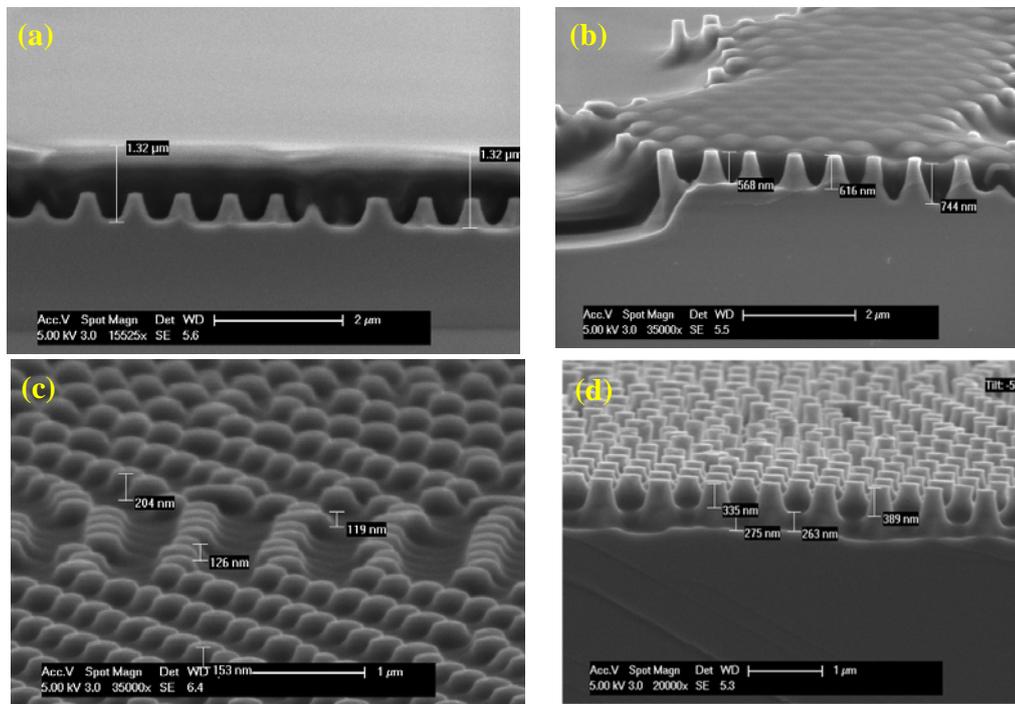


Figure 6.3.2 Process of inserting PMMA to prevent short circuiting the junction. (a) Spun-on PMMA to cover the nanostructures; (b) UV-Ozone treatment to expose the tip; (c) More UV-Ozone exposure; (d) Tips are ready for electrode contact.

We defined the process of inserting the PMMA layer as PMMA treatment. Figure 6.3.2 shows the SEM result of PMMA treatment after GaAs overgrowth and final metal deposition. (a) shows the spun-on 1.3 μm PMMA to cover the nanostructures; (b) shows the nanostructured array after UV-Ozone treatment to expose the tips; (c) shows the SEM of the nanostructured devices after more UV-Ozone exposure; (d) shows the tips after the optimum exposure, which are ready for metal/ITO contact.

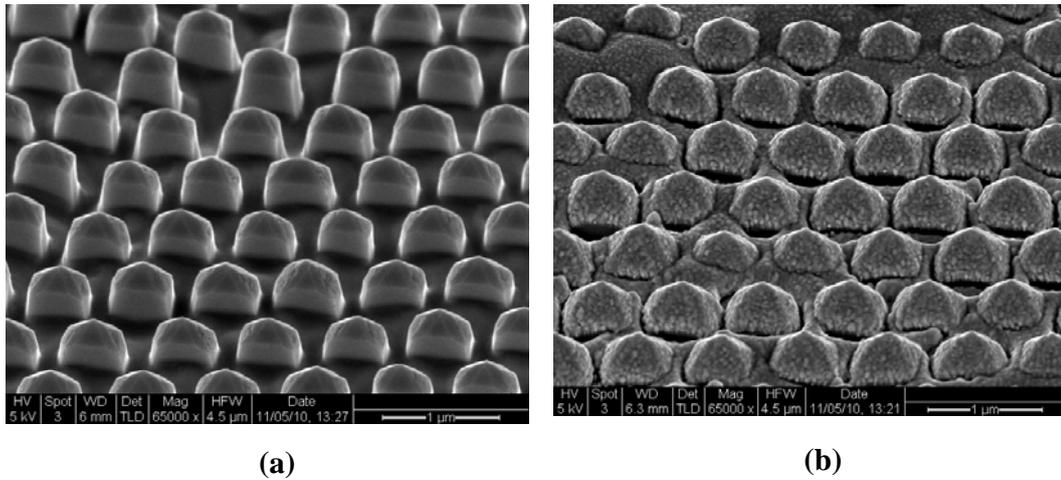


Figure 6.3.3 SEM images showing the effectiveness of the PMMA treatment and metal contact deposition. (a) After PMMA treatment. (b) After metal deposition.

We have accomplished all process steps and prototyped a working nanostructured III-V solar cell device that overcomes the leakage/short problems. Figure 6.3.4 shows the final nanostructured device structure and the planar structure control sample in the same MOVPE run (exactly same growth condition). To prove the concept, we designed a simple (**not optimized**) single GaAs P-N junction with an AlGaAs window layer to confine the minority carriers.

Figure 6.3.4 shows the schematic structure of the final device and control sample. (a) shows a nanostructured GaAs solar cell. (b) shows a planar GaAs as control sample. (c) shows the band diagram of the planar solar cell or along a normal direction to the slope of nanopyramid solar cell. The depletion region is about 80nm, the whole P-N junction is 200nm. The doping could be reduced to increase the depletion region in an optimized structure.

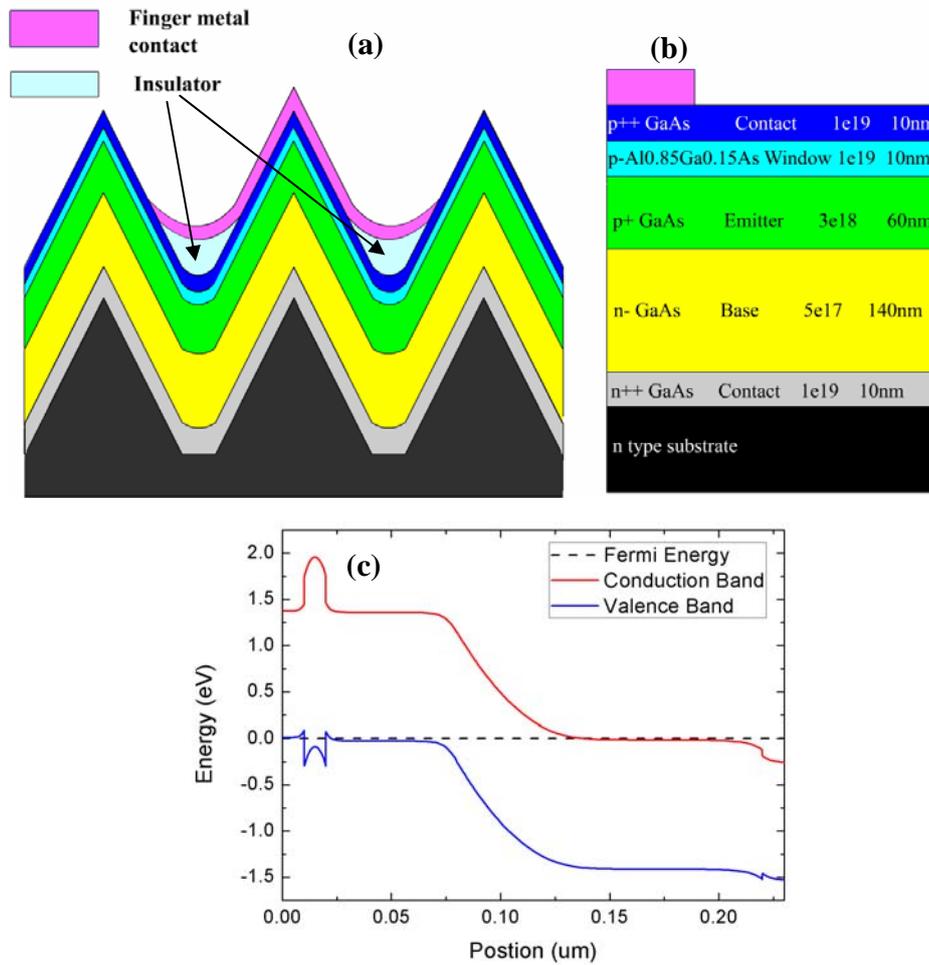


Figure 6.3.4 Schematic structure of the final device and control sample. (a) Nanostructured GaAs solar cell; (b) Planar GaAs solar cell as control sample. (c). Band diagram of the planar solar cell or along the normal direction to the slope of nanopyramid solar cell.

6.4. I-V Characterization

In order to verify that the MOVPE material growth is reasonably good for the first step, we measured the I-V characteristic of the planar control sample using a one sun solar simulator. Figure 6.4.1 shows the result of the I-V characteristic of the planar control sample. (a) shows a linear scale, (b) shows a log scale, (c) is a zoom-in of voltage

from -0.1 to 0.6V. (d) shows the calculated results for this solar cell.

From -1.0 V to 1.0 V, the planar control sample's I-V curve qualifies as a good p-n diode behavior; however the short circuit current is small due to the very thin optical absorption layer. This demonstrates the high quality of the MOVPE material and that the doping levels are well controlled.

We noted that the efficiency of the planar control sample is low, this is because we only grow a **200 nm** absorbing layer, not thick enough to absorb much of the passing light.

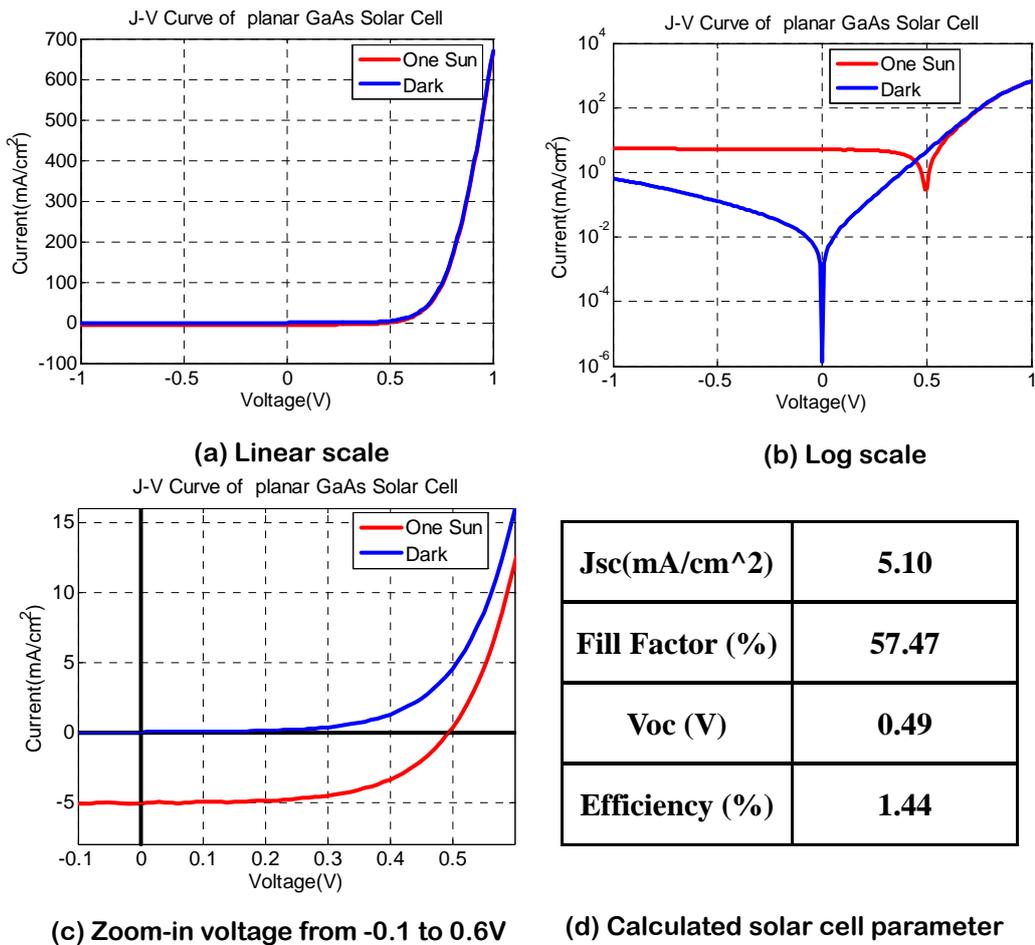


Figure 6.4.1 I-V curve of the control sample. (a) Linear scale, (b) Log scale, (c) Zoom-in voltage

swept from -0.1V to 0.6V (d) Calculated solar cell parameters

In order to compare the nanostructured GaAs solar cell to the planar control sample, Figure 6.4.2 shows the I-V curve of nano-structured sample. (a) is on a linear scale, (b) is on a log scale (c) is a zoom-in voltage sweep from -0.1V to 0.5V, (d) shows the calculated solar cell parameters.

We noted that for the I-V curve of the nanostructured sample under no illumination, the dark current is about 100 times of that of the planar counterpart. And V_{oc} and Fill Factor decrease a lot comparing to the planar counterpart.

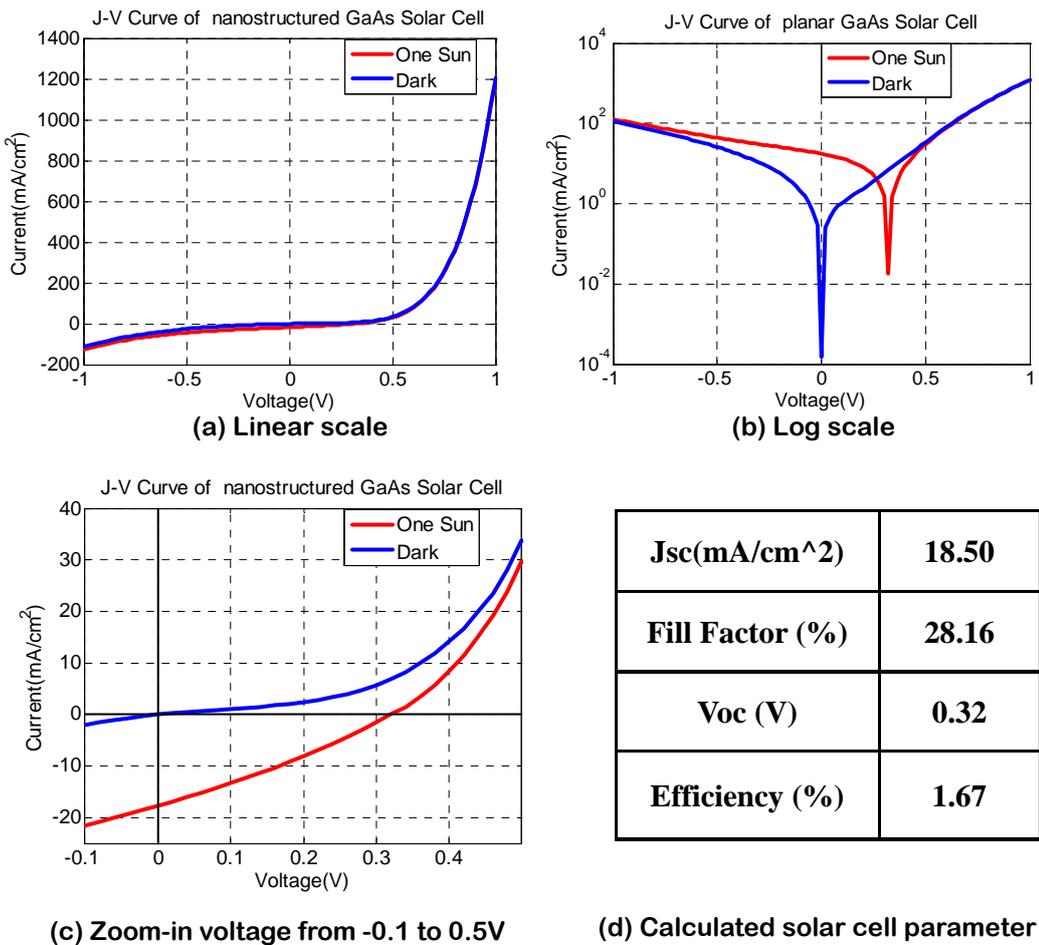


Figure 6.4.2 I-V curve of nano-structured GaAs solar cell sample. (a) Linear scale. (b) Log scale. (c)

Zoom-in voltage from -0.1V to 0.5V. (d) Calculated solar cell parameters.

Above all the shortcomings, there is one feature that outstandingly surpasses the planar counterpart: the short circuit current density is improved by 2X over the planar cell. This is because of the light trapping and absorption enhancement of this unique nanostructure. Thus, the overall efficiency is actually improved by roughly 15%. Note that it is difficult to measure the actual area of active nanostructure solar cell region, with a potential for an estimated error of 40%. Nevertheless, the nanostructured solar cell demonstrates an overall efficiency that is better than or equivalent to that of the planar solar cell grown under same conditions and with an equally thick optical absorbing layer.

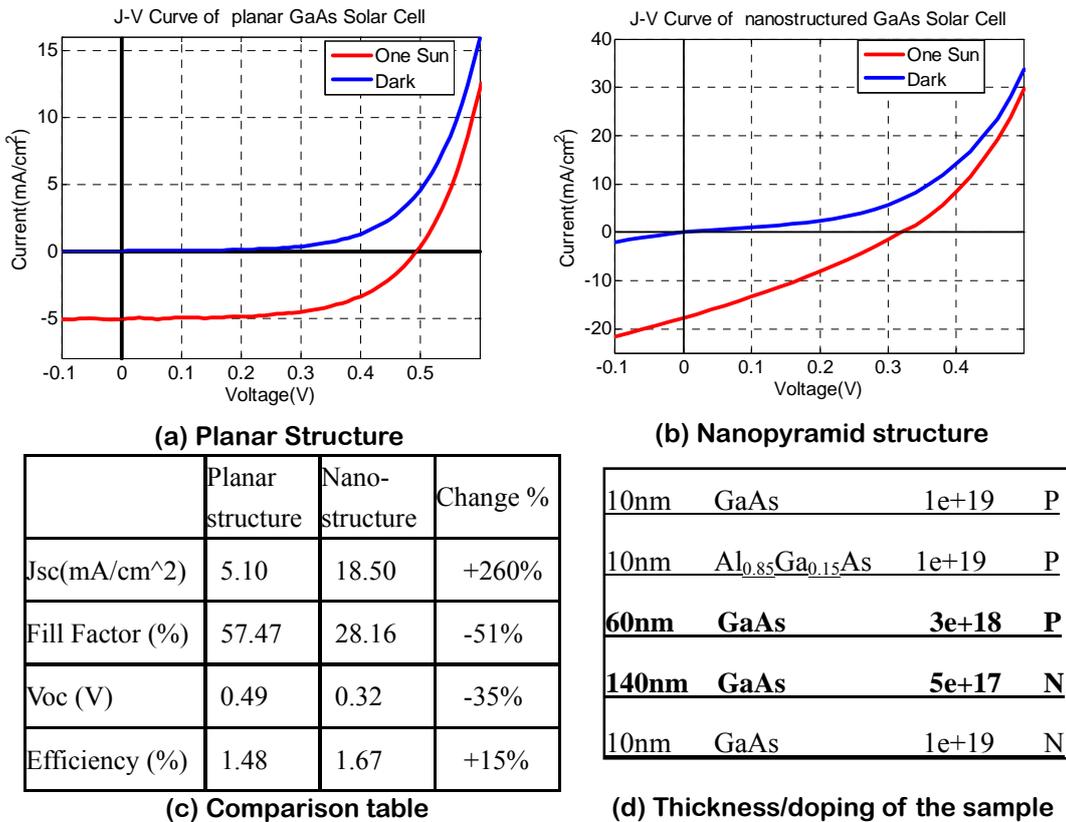


Figure 6.4.3 Comparison of the planar structure and nano-structure with the same thickness of

absorption layer (200nm). (a) (b) are I-V curves of the planar control sample and the nanostructured solar cell sample with similar voltage sweeping range. (c) Comparison table of planar structure and nanostructure. (d) Thickness/doping profiles of the planar control sample which is also conformally coated on the nanostructure.

Revisiting the nanostructure angle independent simulation, over one day (24 hours)[7], the energy harvested by the nanopyramid solar cell is **1.4 X** greater than that of its planar counterpart!

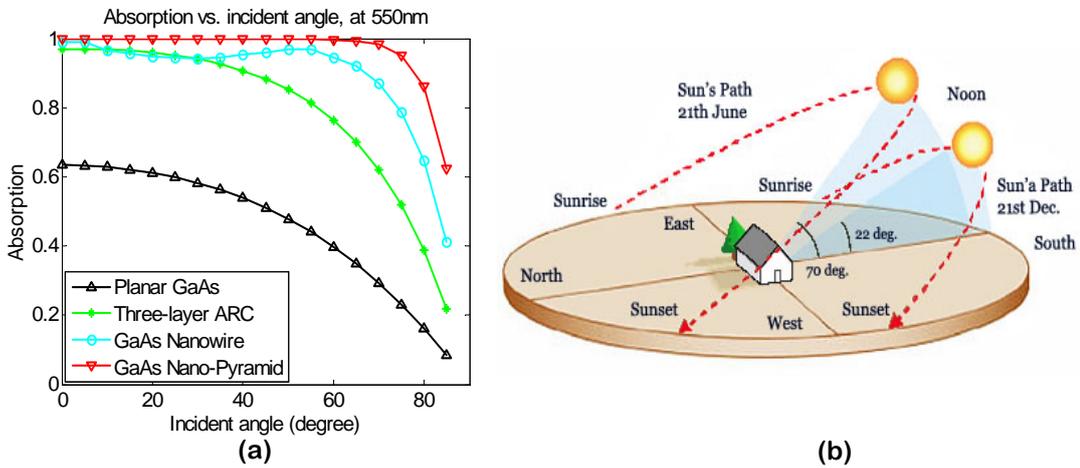


Figure 6.4.3 In 24 hours, a nanostructured solar cell's overall improvement over the planar control sample. (a) Simulation and comparison of absorption of planar and different nanostructure solar cells. (b) Schematic of integrating 180 degree angle to get overall harvested energy. [7]

6.5. Comparison to Relevant Literature

Czaban, LaPierre, et al, reported in "GaAs Core-Shell Nanowires for Photovoltaic Applications" in Nano Lett.(2009) a nanostructured GaAs solar cell with an efficiency of 0.36% and V_{oc} of 0.20V. Compared to this work, we improve V_{oc} from 0.20V to 0.32V (a 60% increase) and efficiency from 0.83% to 1.67% (a 105% increase!)

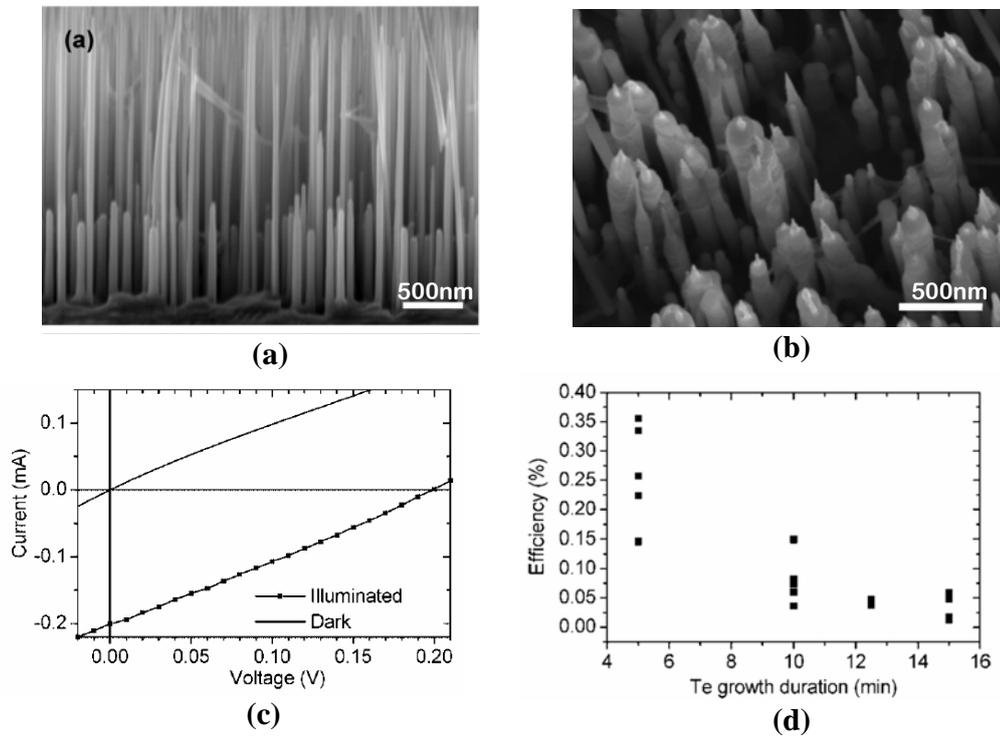


Figure 6.5 GaAs core-shell nanowire solar cell reported in [8]. (a) Cross-sectional SEM images of GaAs nanowire array, scale bar indicates 500 nm. (b) Tilted SEM images of GaAs nanowire solar cell device, Tips of nanowires after HF etching of oxide; scale bar indicates 500 nm. (c) I-V curve of the sample in dark and illuminated conditions. (d) Energy conversion efficiencies of photovoltaic devices for different Te-doped growth durations.[8]

6.6. Projected Improvement

As proof-of-concept, this first-ever working nano-pyramid solar cell has much room to improve its efficiency.

To deeper understand the factors that effect a solar cell's efficiency, we draw the equivalent circuit for a solar cell under illumination and load as shown as Figure 6.6.1 (a). There are two major parasitic resistances that effect the overall performance of solar cells:

shunt resistance and series resistance [9][10]. Figure 6.6.1 (b) shows an ideal solar cell's I-V curve and one with too small shunt resistance, the other one with too high series resistance [11]. Figure 6.6.1(c) shows how series resistance effects solar cell efficiency and fill factor. By increasing series resistance, the solar cell moves away from the maximum power point, both short circuit current and fill factor decrease [9]. Figure 6.6.1(d) shows how shunt resistance effects solar cell efficiency and fill factor. By increasing shunt resistance, the solar cell moves towards the maximum power point, both open circuit voltage and fill factor increase. [10]

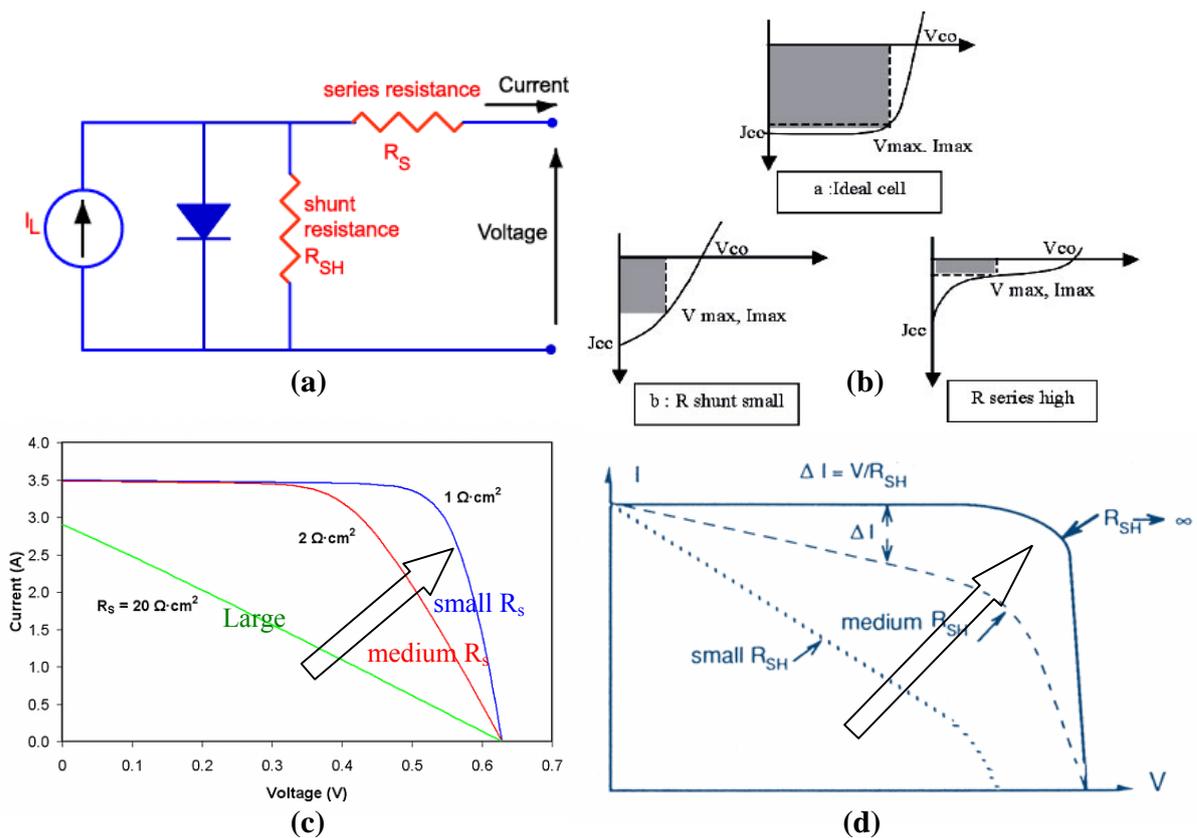


Figure 6.6 Parasitic resistances: shunt resistance and series resistance (a) equivalent circuit of solar cell device under load. (c) The effect of series resistance on a solar cell's output voltage and current.

By decreasing series resistance, the solar cell moves toward the maximum power point. [9]. (d) The effect of shunt resistance on the fill factor of a solar cell. By increasing shunt resistance, the solar cell moves toward the maximum power point. [10]

According to this analysis, we need to decrease series resistance and increase shunt resistance. One possible approach is using a nanowire transparent mesh contact to decrease the series resistance (better contact on the tips of nanopylramids, lower sheet resistance), and increase the shunt resistance (avoid contacting on the valleys or bottoms of nanopylramid template) and more efficiently collect current from nanopylramid surfaces.

6.7 Nanowire mesh transparent contact

Solution-processed transparent electrodes consisting of random meshes of metal nanowires are proposed as a cost-effective alternative for transparent conductive electrodes for thin-film solar cells, light-emitting diodes, and many display technologies being developed in Professor Peter Peumans group at Stanford University [12]. Unlike doped metal oxides, such as ITO with limited optical transparency and high sheet resistance, nanowire transparent electrodes have tunable transparency and sheet resistance based on the density and diameters of the nanowires. Furthermore, conventional doped metal oxides are costly and are prone to cracking when deposited on flexible substrates and they require a high-temperature annealing step for the best

performance [12], while nanowire transparent electrodes are cheaper and better suited to the thin-film, nanostructured III-V solar cell described in this dissertation.

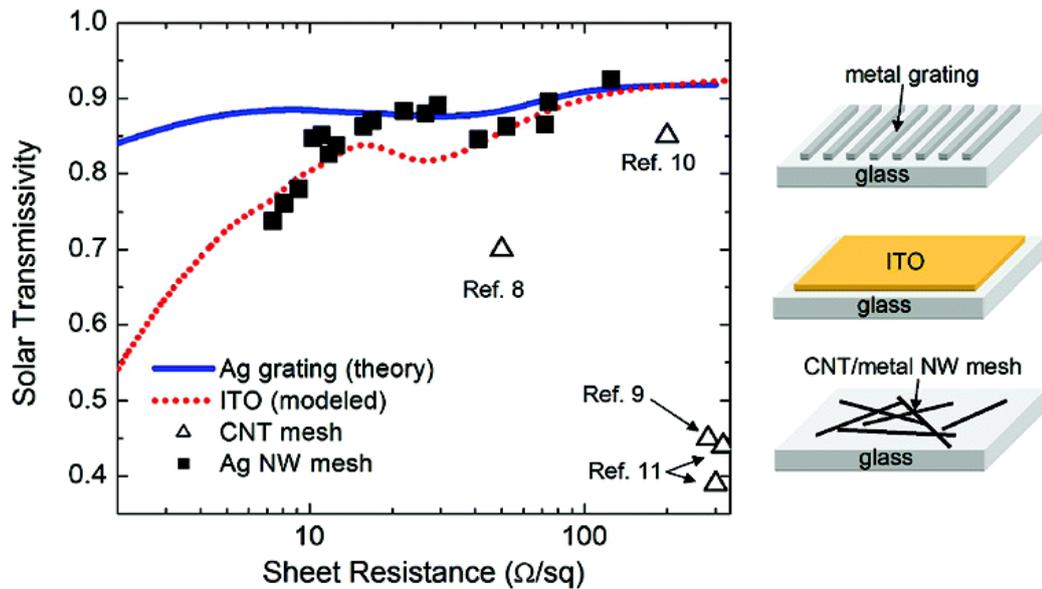


Figure 6.7.1 Solar transmissivity vs. sheet resistance for Ag gratings, ITO, CNT meshes and Ag nanowire meshes deposited on a glass substrate [12]. “The data for the Ag gratings were obtained by finite element modeling. The grating period is 400 nm, the Ag line width is 40 nm, and its thickness is varied. The data for ITO are computed based on optical constants for e-beam deposited ITO acquired using spectroscopic ellipsometry. The data for CNT meshes were obtained from the literature, and the Ag nanowire mesh data were obtained experimentally. T_{Solar} is calculated by integrating the product of the spectrally resolved transmittance with the spectrally resolved AM1.5 photon flux over the wavelength range $\lambda = 400\text{-}800\text{ nm}$.” [12]

J.Y. Lee, S.T. Connor, Y. Cui and P. Peumans, et al [12] demonstrated an optical transparency equivalent to or better than that of metal-oxide thin films for the same sheet resistance. Organic solar cells deposited on these electrodes show performance

equivalent to that of devices based on a conventional metal-oxide transparent electrodes.

[12]

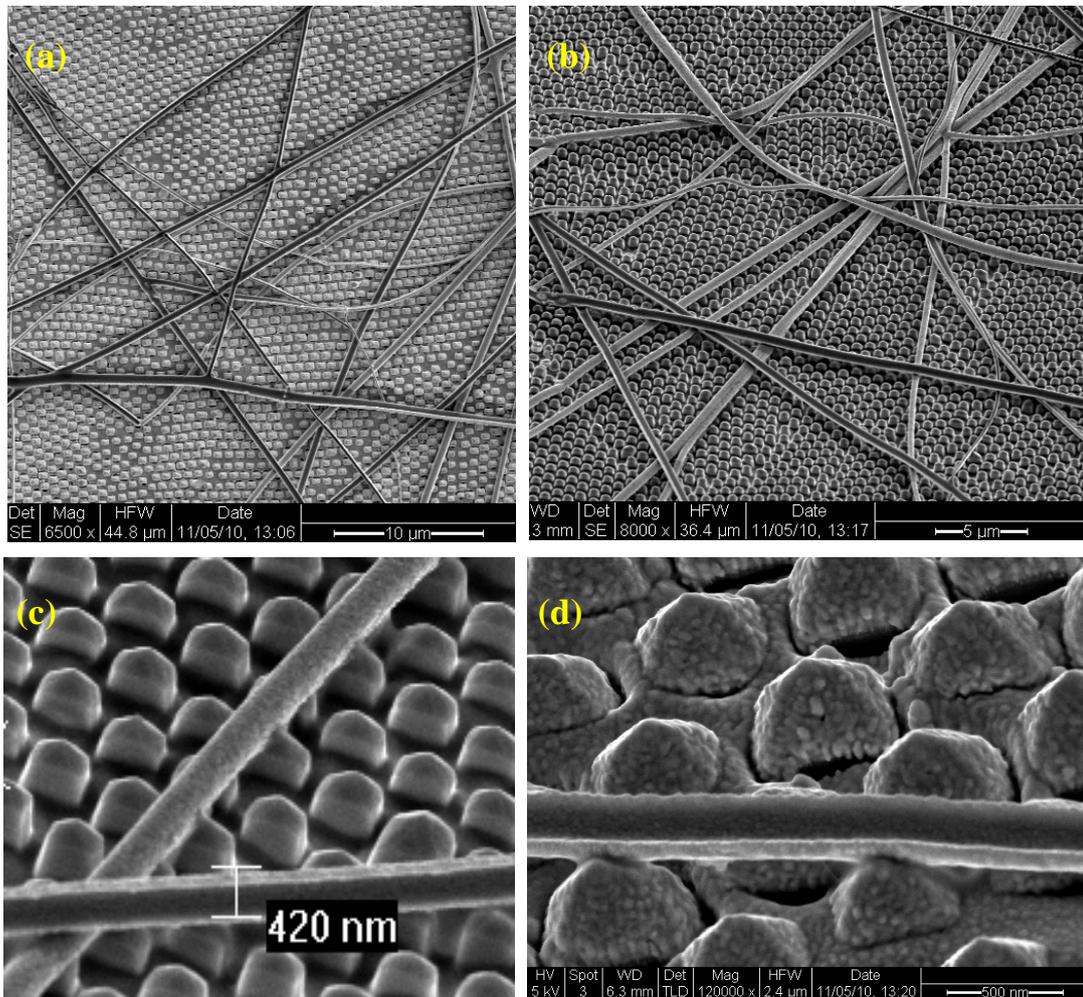


Figure 6.7 Nanowire mesh transparent contact on nanostructured III-V solar cell. (a) on GaAs nanopyramid in the region with no metal deposition, (d) SEM 45 degree view of nanowire contact on GaAs nanopyramid in the region with metal deposition. We worked with Professor Yi Cui's research group on nanowire mesh transparent [13][14] for our nanostructured III-V solar cell device.

We worked with Professor Yi Cui's research group on nanowire mesh transparent [13][14] for our nanostructured III-V solar cells. The SEM pictures of nanowire

transparent contact on nanostructured III-V solar cell are illustrated in Figure 6.7. Note that the density is too low and the diameters of nanowires are too large. Nevertheless, this provides a solid starting point for further research.

6.8. Summary

In this chapter, we report the device fabrication and I-V characterization of our nanostructured GaAs solar cells. First, the contact is very important for nanostructured solar cells. We investigated ITO (Tin doped Indium Oxide), metal finger (pad) contacts and nanowire transparent contacts. We found that spinning PMMA over the nanostructured surface to create an insulating layer overcame the shorting and leakage problems which commonly exist in nanowire solar cells reported in literature [8].

We measured the I-V characteristics of both a planar control sample and nanostructured solar cells with and without illumination. Comparing the planar structure solar cell with same absorption thickness (200nm), the nanostructured III-V solar cell showed a significantly increased short circuit current and an overall increased efficiency, which is much better overall performance compared to the literature [8].

Since this was just a first proof-of-concept device, the results are very encouraging that there is far more room for improvement. We studied the equivalent solar cell circuit and suggest future work to improve the solar cell fill factor, open circuit voltage and

efficiency. One promising approach is to use nanowire transparent Ohmic contacts to lower series resistance and increase shunt resistance and to collect current from the nano-pyramid surfaces more efficiently.

We deposited a Cu nanowire mesh on our nanostructured solar cells and used SEM to study the density and diameters of the nanowire mesh. This provides a solid foundation for further research.

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Chapter 7 Summary and Contributions

7.1 Summary

First, we demonstrated that nanostructures can enhance light trapping and improve absorption in very thin layers for III-V solar cells. Secondly, nanostructures can potentially reduce the cost of III-V solar cells by enabling growth of III-V solar cells on Si substrates via a nano template that overcomes the differences in lattice constant and by reducing the thickness of the optical absorption and buffer layers. Eventually, the substrate can be a lightweight, flexible and low cost material. Third, for real applications, our nanostructured solar cell has much wider incident acceptance angle that can potentially reduce the need of 2-axis mechanical sun-tracking system. The overall energy harvested during a day (24 hours) by our nanostructure solar cell can be 2X of that of the planar control sample under same growth condition.

Compared to planar structures of the same thickness absorption layer, the nanostructured III-V solar cell showed a significantly increased I_{sc} higher efficiency. While the junctions formed over the nano-template resulted in a decreased V_{oc} and decreased Fill Factor, the overall efficiency was slightly higher, demonstrating a clear proof-of-concept device that has tremendous room for improvement. Based on the results achieved in this research project, one can project that nanostructured, multijunction III-V

solar cells grown on low-cost, flexible substrates can achieve efficiencies exceeding those of single crystalline Si (c-Si) at a lower cost.

This research project has opened many new opportunities of combining nanotechnology with traditional III-V optoelectronics. When nano meets III-V, it just the journey is just beginning!

7.2 Contributions

The main contributions of this dissertation are listed as below:

1. Proposed a novel nano-structured III-V multijunction solar cell design that can provide a path to reduce the cost of III-V solar cells while achieving efficiencies greater than c-Si.
2. The first demonstration of high quality, **single crystalline** III-V (GaAs and AlGaAs) polar material core-shell epi growth on group IV (nanostructured Ge on Si substrate) nonpolar material, with significantly lower anti-phase domain density.
3. Demonstrated critical role of surface kinetics in epitaxial growth on nanostructured material. Demonstrated uniform, conformal epitaxy on high aspect ratio nanostructures.
4. Developed complete processing steps to fabricate a working, single-crystal III-V solar cell on a nanostructured template. Overcame the shorting problem which

always exists in nanostructured solar cells. Compared planar structure solar cell with same absorption thickness, our nanostructured III-V solar cell shows **significantly increased short circuit current and higher overall efficiency.**

5. Proposed a **generic method** of design and fabrication of III-V optoelectronic devices on low-cost substrates (Si, flexible material), for instance, Nanostructured-LED on Si.

7.3 Future Work

1. Using nanowire transparent contact (or other better contact technology other than metal pad in this dissertation) to reduce the series resistance.
2. Improve uniformity of the nano-template, improve the coverage and uniformity of epitaxially overgrown III-V layers, increase the shunt resistance and prevent the leakage current.
3. Increase the spacing of individual nanostructure to enable growth of thicker absorption layers
4. Optimize doping profile and thickness of the PN junctions

<The End>