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Characterization of modulation-doped field-effect transistors with gate lengths down to 600 angstroms

de la Houssaye, Paul Raymond, Ph.D.
Stanford University, 1988

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CHARACTERIZATION OF MODULATION-DOPED FIELD-EFFECT TRANSISTORS WITH GATE LENGTHS DOWN TO 600 ANGSTROMS

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF APPLIED PHYSICS AND THE COMMITTEE ON GRADUATE STUDIES OF STANFORD UNIVERSITY IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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ABSTRACT

The drive to produce faster and faster devices has created intense pressure to shrink device sizes dramatically over the years. Using Molecular Beam Epitaxy (MBE) to grow Gallium Arsenide (GaAs) based structures, vertical dimensions have been reduced to the atomic scale. The recent use of ultrahigh resolution electron beam lithography in device fabrication has made it possible to reduce lateral gate dimensions to less than 0.1 \( \mu \)m. At these dimensions, ballistic transport, velocity overshoot, and other hot-electron effects must be considered.

To investigate these effects, a process was developed to fabricate Field-Effect Transistors (FET's) with recessed gates as small as 550 Å. GaAs MESFET's were fabricated and no velocity overshoot effects observed.

For investigation of hot-electron effects, the Modulation-Doped Field-Effect Transistor (MODFET) is a better device for study due to the lack of doping in the channel (electron transport) region. Given the superior electron transport properties of the Indium Gallium Arsenide (InGaAs) system, an additional improvement can be made on the traditional structure by doubly confining the electrons in an undoped InGaAs channel. Thus two types of MODFET's were fabricated with gate lengths between 2 microns and 550 Å, the first with a standard GaAs channel, the second with an InGaAs channel. DC characterization at room temperature was then carried out. An effective electron saturation velocity was calculated for each device from the peak transconductance. Indications of a peak in the maximum transconductance and effective saturation velocity at a gate length of approximately 0.15 \( \mu \)m were seen in the GaAs channel devices. While the saturation velocity for the InGaAs channel devices was comparable to the GaAs channel devices, no similar ballistic effects were seen for the InGaAs devices. This can be attributed to differences in the scattering characteristics of the two materials systems. From this study, it would seem that a structure with double confinement and/or with a larger \( \Gamma \) to L valley separation than that of GaAs is preferable to obtain the greatest device performance benefits in going to ultra-short gate length MODFET's.
ACKNOWLEDGEMENTS

I am indebted to a great many people, without whose cooperation and support this work could not have been completed successfully.

Most importantly, this work would not have been possible without the immense contribution from my colleague David R. Allee. His contribution includes, most significantly, the operation and redesign of the electron beam control electronics to allow for the writing of the gate patterns, as well as most of the data taking and analysis for the MESFET's. Most of what is presented in Chapter 4 is as a direct result of his efforts. He also assisted in processing some of the wafers, preventing me from going slowly mad during some of the longest processing runs. His pleasant manner throughout our work made it extremely enjoyable.

I am equally indebted to my advisor, Professor James S. Harris, Jr., not only for his technical and personal support, but also for his managerial support in the gathering of funds to proceed. Under his direction, this work has been supported by the Semiconductor Research Corporation (SRC) under contract No. SRC86-11-107, by the Joint Services Electronics Program under contract No. DAAG29-85-K-0048, and by DARPA under contract No. N00014-84-K-0077. Thanks are also due to Professor R. F. W. Pease for his similar support throughout this work, as well as allowing his graduate student, David R. Allee to participate in this extremely successful collaboration.

Thanks is also due to the late Professor G. L. Pearson and his former graduate student Dr. Kevin Malloy. Because of them I had the opportunity to begin acquiring hands on experience with heterojunction device growth using Professor Pearson's old liquid phase epitaxy system.

My thanks goes as well to the rest of the Harris group. Darrell Schlom grew a number of wafers for Dave and me during the early phases of this work. Through Yi-Ching Pao's generosity we were also able to obtain a number of wafers from Varian and benefit from his extensive knowledge of processing and MODFET physics. Cooperative efforts from Phil Pitner and Alex Harwit were instrumental in building up the lab from scratch, no small feat since when the three of
us joined the Harris group we did not have so much as a clean room! Their efforts helped bring together all the necessary equipment and supplies to build these devices. Eric Hellman deserves special thanks for his help in checking the work on multiple conduction paths in Hall bars as described in Appendix A.

Thanks are also due to all the secretaries, especially Sandy Eisensee, Gail Chun-Creech, Lachen Pence, and Paula Perron, without whom life would have been made much more difficult (and much less fun). Thanks are also warmly given to the many friends and family members that enthusiastically gave their love and support during both the exciting and the hard times comprising these years at Stanford. They meant more to me than they will ever know.

Last but not least, I thank all the poor souls who so graciously offered to proof this document. Their help was invaluable.
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**LIST of SYMBOLS**

\[ a = \text{Thickness of channel region (after etching) in MESFET} \]
\[ b = \text{Distance between sensing fingers and Hall bar ends} \]
\[ B, \vec{B} = \text{Magnetic field strength} \]
\[ \beta = \text{Logarithmic proportionally constant of } I_H \text{ and } I_L \text{ on gate length} \]
\[ C = \text{Total capacitance associated with the gate} \]
\[ c = \text{Distance between fingers in Hall bar, as shown in Figure 2.9} \]
\[ d = \text{Gate metal to channel interface distance (after etching) in MODFET} \]
\[ \Delta d = \text{Distance between channel interface and peak of electron wave function} \]
\[ d_{1,2} = \text{Depletion widths as shown in Figure 2.6} \]
\[ \varepsilon = \text{Dielectric constant} \]
\[ \varepsilon_0 = \text{Dielectric constant of free space} \]
\[ \vec{E} = \text{Electric field vector } (E_x, E_y) \]
\[ \Delta E_c = \text{Conduction band discontinuity} \]
\[ E_c = \text{Conduction band energy} \]
\[ E_f = \text{Fermi energy} \]
\[ E_x = \text{Electric field in } x \text{ direction} \]
\[ E_y = \text{Electric field in } y \text{ direction} \]
\[ \vec{F} = \text{Force on electron in magnetic field} \]
\[ g = \text{x distance between source and probe point in Hall bar} \]
\[ g_{m,s}, g_{m,i} = \text{Intrinsic transconductance of the device} \]
\[ g_{mx}, g_{mi} = \text{Extrinsic transconductance of the device} \]
\[ g_{out} = \text{Output conductance of the device} \]
\[ h = \text{Width of depletion region under gate in MESFET (function of gate voltage)} \]
\[ I = \text{Current (general)} \]
\[ I_{ds} = \text{Drain-source current} \]
\[ I_{dss} = \text{Saturated drain-source current} \]
\[ I_H = \text{Source-drain current, device near pinch-off (Kizilyalli et al.)} \]
\[ I_L = \text{Source-drain current, device fully on (Kizilyalli et al.)} \]
\[ \vec{J} = \text{Current density (Sheet density)} \]
\[ k = \text{Boltzmann's constant} \]
\[ L = \text{Length of Hall bar} = 2a + b \]
\[ L_g \] = Gate length
\[ L_{gd} \] = Gate to drain distance
\[ n \] = Number of electrons in the conduction band, equal to \( n_s \) in Appendix A
\[ n_s \] = Sheet carrier concentration
\[ N_c \] = Effective density of states in the conduction band
\[ N_d \] = Activated donor concentration in material
\[ q \] = Charge on electron
\[ \rho \] = Resistivity
\[ \rho_c \] = Contact resistivity (in \( \Omega \) mm)
\[ \rho_s \] = Sheet resistivity
\[ r \] = Half the width of the sensing fingers, or, distance from current source
\[ R_d \] = Drain resistance
\[ R_g \] = End to end gate resistance
\[ R_s \] = Source resistance
\[ R_{\Omega ic} \] = Ohmic contact resistance
\[ t \] = Thickness of Hall conduction layer
\[ s \] = \( y \) distance between source and probe point
\[ \sigma \] = Sheet conductivity tensor
\[ t_g \] = Gate metal thickness
\[ t_{Au, Al, Ti} \] = Au, Al, and Ti gate metal thickness
\[ \tau \] = Gate transit time
\[ T \] = Temperature
\[ \omega_\tau \] = Frequency associated with gate transit time
\[ v, v^\rightarrow \] = Carrier velocity under the gate (or in channel)
\[ v_s \] = Peak (saturated) carrier velocity
\[ V_{1, 2, \text{etc.}} \] = Voltage points on Hall bar, as shown in Figure A.1
\[ V_b \] = Schottky barrier voltage
\[ V_{ds} \] = Drain-source voltage
\[ V_{gs} \] = Gate-source voltage
\[ V_p \] = Pinch-off voltage
\[ V_t \] = Threshold voltage
\[ W \] = Width of Hall bar
\[ W_g \] = Gate width
\[ W_{tot} \] = Total gate width, including connecting line to active area
\[ \mu \] = Low field mobility of electrons (velocity per unit electric field)
### GLOSSARY

<table>
<thead>
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<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>2-DEG</td>
<td>Two-Dimensional Electron Gas</td>
</tr>
<tr>
<td>AlGaAs</td>
<td>Aluminum Gallium Arsenide</td>
</tr>
<tr>
<td>FET</td>
<td>Field-Effect Transistor</td>
</tr>
<tr>
<td>GaAs</td>
<td>Gallium Arsenide</td>
</tr>
<tr>
<td>HMDS</td>
<td>Hexamethyldisilazane (Adhesion Promoter)</td>
</tr>
<tr>
<td>HEMT</td>
<td>High-Electron Mobility Transistor</td>
</tr>
<tr>
<td>HFET</td>
<td>Heterojunction Field-Effect Transistor</td>
</tr>
<tr>
<td>InGaAs</td>
<td>Indium Gallium Arsenide</td>
</tr>
<tr>
<td>LPE</td>
<td>Liquid Phase Epitaxy</td>
</tr>
<tr>
<td>MEBES</td>
<td>Manufacturing Electron Beam Exposure System</td>
</tr>
<tr>
<td>MESFET</td>
<td>Metal-Semiconductor Field-Effect Transistor</td>
</tr>
<tr>
<td>HFET</td>
<td>Heterojunction Field-Effect Transistor</td>
</tr>
<tr>
<td>MODFET</td>
<td>M0dulation-Doped Field-Effect Transistor</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
</tr>
<tr>
<td>MOCVD</td>
<td>Metal-Organic Chemical Vapor Deposition</td>
</tr>
<tr>
<td>MOMBE</td>
<td>Metal-Organic Molecular Beam Epitaxy</td>
</tr>
<tr>
<td>MSG</td>
<td>Maximum Stable Gain</td>
</tr>
<tr>
<td>PMMA</td>
<td>PolyMethylMethAcrylate</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive Ion Etching</td>
</tr>
<tr>
<td>OAI</td>
<td>Optical Associates Incorporated</td>
</tr>
<tr>
<td>SDHT</td>
<td>Selectively Doped Heterojunction Transistor</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscopy</td>
</tr>
<tr>
<td>TCA</td>
<td>1,1,1-Trichloroethane, CH3CCl3 (Methyl Chloroform)</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission Electron Microscopy</td>
</tr>
<tr>
<td>TEGFET</td>
<td>Two-Dimensional Electron Gas Field-Effect Transistor</td>
</tr>
<tr>
<td>UHREBL</td>
<td>Ultra-High Resolution Electron Beam Lithography</td>
</tr>
<tr>
<td>VPE</td>
<td>Vapor Phase Epitaxy</td>
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Chapter 1

Introduction and Goals

From the very inception of the computer, the computing field has been beset by the question of how to build faster and smarter machines. The earlier machines were designed to perform extremely simple repetitive tasks and were extremely bulky for their computing power, ranging from the mechanical to the first electronic digital computers comprised of hundreds of vacuum tubes. Computing speed in the early electronic machines was limited both by the switching speed of the devices as well as the distance between the devices. Complexity of these early electronic machines, and thus their "intelligence", was limited by the power dissipated from the many vacuum tubes necessary. While these problems have improved by many orders of magnitude, they still provide the fundamental limits today, leading us to search for yet smaller, faster devices that use a minimum of power so that they can be incorporated into more complex, denser, circuits.

The first demonstration of the transistor in 1947 by scientists at Bell Laboratories, even though its size was tens of thousands of times larger than today's devices, gave the world hope in this quest. Electron flow was governed by the atomic structure of a piece of semiconductor crystal, instead of the energy intensive thermionic emission and electrostatic control with large metal plates and grids. The ability to manufacture smaller, faster devices with lower power consumption became dependent upon how well electrons could be controlled on an atomic level. The advent of the gallium arsenide (GaAs) material system as a replacement for silicon, with its lower effective mass for the electron and the flexibility allowed by combining it with other similar materials to form confining heterojunctions, produced an even higher speed potential.

A number of techniques have been developed over the years to fabricate these devices. Processing techniques and clean room technologies have been dramatically improved. For
control of vertical dimensions in Si devices, better understanding of ion implant and diffusion processes has been achieved. For devices fabricated in GaAs, the advent of Molecular Beam Epitaxy (MBE) has made it possible to construct device layers with dimensions measured in monoatomic layers.

Control of horizontal dimensions has also been progressing along a similar line, with the improvement of optical lithography technology. Features can be fabricated down to less than 0.5 microns using deep ultraviolet exposure. Simultaneously, electron beam technology has improved to allow the writing of finer and finer lines in various materials. In 1960, features were made in thin membranes with dimensions less than 1000 Å\(^1\). Only recently however, have these ultra-high resolution electron beam lithography (UHREBL) techniques been used in the fabrication of electronic devices\(^2\). Our electron beam exposure system, built at Stanford, has a beam size of as small as 50 Å. This translates to possible feature sizes as small as 350 Å due to scattering in the standard PMMA (PolyMethylMethAcrylate) resist used for pattern transfer. As one approaches these dimensions, electron transport must incorporate ballistic transport, velocity overshoot and other hot-electron transport effects into understanding and modeling the characteristics of ultra-small devices.

Over the past five years, there has been interest in the electron transport properties in GaAs MESFET's (MEtal-Semiconductor Field-Effect Transistors) as a function of gate length. The central question for ultra-short gate devices is whether any ballistic effects should or are observed. The existence of these effects in this material system is relevant to the maximum frequency response one can expect to obtain in these devices, as the device speed is directly related to the transit time under the gate. Classically, in order to increase the switching speed of these devices one should decrease the gate length and thus reduce the gate to source capacitance and increase the intrinsic transconductance. However, in cases where the gate length is sufficiently small, the peak velocity of the electrons in the channel is directly related to the switching speed. Thus if the electrons simply reach a saturated velocity in their transit under
the gate, the device performance would not be expected to improve with decreasing gate length. However, while the higher low-field mobility for electrons in GaAs allows for higher velocities than in Si, electrons are scattered readily off the high concentration of doping centers in the active device area. The electrons are also not heavily confined into a thin channel region, and thus can flow in a large (compared with the gate length) pattern around the bottom of the active gate area. Thus, these devices are not ideal for studying high field transport of electrons in GaAs.

For investigation of hot-electron effects, the Heterojunction Field-Effect Transistor (HFET), or the MODulation-Doped Field-Effect Transistor (MODFET) is a better device for study due to the lack of doping in the channel (electron transport) region. Due to the heterojunction band gap discontinuities which exist in the GaAs/AlGaAs system, extra confinement along with electron screening effects also allow improved electron transport properties. The use of InGaAs as the channel material, with its still higher, low field mobility, allows for even better electron confinement and even higher screening effects. Thus two types of MODFET's were selected for study, the first with a standard GaAs channel, the second with an InGaAs channel. The aim was to compare these structures as a function of gate length down to 550 Å with an eye towards any differences in electron transport in these structures. The aim of this work was not to build an ultra-fast device, but to understand the underlying hot electron transport properties and their implications to ultra-fast devices.

The chapters of this thesis are organized as follows. Chapter 2 provides a background for this effort, including a description of the MBE growth technique and the simple Field-Effect Transistor models and structure, especially as it pertains to electron transport and performance of MODFET's. A description of prior work in small gate length structures is also included. Chapter 3 contains the process development details and final process description. Chapter 4 describes the first test of the process: Results of a test MESFET run. Chapter 5 describes the fabrication, structure, analysis and results of a series of MODFET runs with gate lengths down to 550 Å. A comparison is made between the traditional MODFET with a GaAs channel and the
pseudomorphic, InGaAs channel MODFET in terms of electron transport in the structures.

Chapter 6 is a summary of this work as well as suggestions for further work.
Chapter 2

Background

2.1 MESFET Operation

A simple description of a MEtal-Semiconductor Field-Effect Transistor (MESFET) is illustrated in Figure 2.1. It consists of a layer of semiconductor material which is doped (a small amount of a specific impurity is added to increase the number of holes or electrons in the material, making it p or n-type respectively, and thus decreasing its sheet resistivity) to which two ohmic electrical contacts are formed. One of the contacts is designated the source of electrons (or holes) while the other is designated the drain, depending upon the intended bias on the device. Between the source and the drain, a third metal layer is deposited, this time with the intention not of making an ohmic contact, but instead of forming a Schottky barrier. By varying the voltage on the gate with respect to the source, it is possible to control the flow of electrons (or holes) between the source and the drain.

![Simplified MESFET diagram](image)

Fig. 2.1. Simplified MESFET diagram.
In order to understand how the current is controlled in the MESFET, it is useful to draw a conduction band diagram (or the valance band for holes) as a function of depth within the device. In this work, however, we will be strictly speaking about $n$-channel devices, where the current is carried by electrons. Thus, I will hereafter limit descriptions to electrons and the conduction band.

The conduction band energy ($E_c$) is the minimum energy an electron may have in order to be in an unbound, conductive state, and in a semi-conductor, still be in an allowed state. The Fermi distribution describes the probability of a state with energy $E$ being occupied and is given by

$$F(E) = \frac{1}{e^{(E - E_f)/kT} + 1}.$$  

The Fermi energy ($E_f$) is therefore the energy where the probability of a state with energy $E_f$ being occupied is 1/2. Thus, the number of electrons in the conduction band is related to the difference between the conduction band energy and the Fermi level. In the simple Boltzmann statistics case, the number of electrons in the conduction band is given by

$$n = N_c \exp\left(-\frac{E_c - E_f}{kT}\right).$$

In the MESFET, the junction between the metal and the GaAs forms a discontinuity in the conduction band. The application of a field on the gate with respect to the source will shift the conduction band with respect to the Fermi level near the gate. As this happens, the population of electrons is either reduced or increased under the gate, and a change in the current that flows from the source to the drain will result. (See for example Sze\textsuperscript{3} or Muller\textsuperscript{4} et al.) This is illustrated in Figure 2.2.
Fig. 2.2. Effect of gate-source bias on source-drain conduction in a MESFET. When a bias is applied, the electron concentration changes in the channel.

There are a number of parasitics that must be minimized in a well designed FET to achieve good performance at both dc and at high frequencies. Figure 2.3 illustrates the major dc parasitics. $R_d$ and $R_s$ represent the source and drain resistances respectively. These resistances include both the metal contact resistances as well as the bulk resistance between the contact and the controlled region under the gate. $g_{out}$ represents the output conductance of the device and can be represented by a resistor shorting the ideal FET. The aim of this work was to compare the internal device performance, so care had to be taken to extract the internal values from those that were measured, including these parasitic elements. This will be taken as a given in the rest of this chapter's discussion.
The relative ease with which the electrons move when subjected to an electric field, the "low field mobility" value, is roughly five times higher in GaAs than in Si (e.g. $5 \times 10^3$ vs. $1 \times 10^3 \text{ cm}^2/\text{V-sec}$ for material doped to $5 \times 10^{16}/\text{cm}^3$). This difference has fueled the extensive interest in GaAs Field-Effect Transistors (FETs) and thus this work concentrates exclusively on these devices.

In order to achieve the best performance at high frequencies from these FETs, one is primarily concerned with increasing $f_T$ or $\omega_T$. $\omega_T$ can be looked at as one over the switching time underneath the gate ($\tau$), and is thus given by

$$\omega_T = \frac{1}{\tau} = \frac{\nu}{L_g} = \frac{g_m}{C},$$

where $\nu$ is the carrier velocity under the gate, $L_g$ is the gate length, $C$ is the total capacitance associated with the gate, and $g_m$ is the (intrinsic) transconductance of the device, given by

$$g_m = \frac{dI_{ds}}{dV_{gs}}.$$
$I_{ds}$ and $V_{gs}$ are the drain-source current and the gate-source voltage respectively. As the gate length gets smaller and smaller, the capacitance in the above equation is no longer dominated by the gate capacitance and is modified by other gate parasitics, such as gate interconnect and fringing field capacitances. Thus increasing the transconductance becomes paramount.

For the case where the field from source to drain is low everywhere, the source-drain current is directly related to the drift velocity of the carriers, and thus to the field from gate to source times the carrier mobility. Therefore,

$$g_m = \frac{dI_{ds}}{dV_{gs}} = \left( \frac{\varepsilon W_g}{h} \right) \frac{\mu}{L_g} \left( V_{gs} - V_t \right),$$

where $\varepsilon$ is the dielectric constant for the material between the channel and the gate, $W_g$ is the gate width, $h$ is the depletion layer thickness, $\mu$ is the low field mobility of electrons (velocity per unit electric field), $V_{gs}$ is the gate to source voltage, $V_t$ is the pinch-off voltage (where the carriers are completely depleted under the gate), and $L_g$ is the gate length.

In the case of a high source-drain field (short gate length), particularly when the device is near pinch-off, the velocity of the carriers underneath the gate saturates. Thus there should be no dependance of the transconductance upon the gate length. Under these conditions, we have

$$g_m \sim \left( \frac{\varepsilon W}{a} \right) v_s,$$

where $v_s$ is this peak velocity, and $a$ is the channel thickness. However, as the gate length is further reduced, there may be a point where velocity overshoot occurs and the carrier velocity will again begin to increase as the electric field increases. Under these conditions, the transconductance will have a weak dependence on gate length.
2.2 MODFET Advantages

The existence of dopant atoms acting as scattering centers in the channel of the device is one of the limitations for the MESFET. These scattering centers prevent electrons from reaching ballistic velocities and seriously reduce even the low field mobility of these devices. The solution is to separate the doping atoms from the region of current flow. The Modulation-Doped Field-Effect Transistor (MODFET), otherwise known as the HEMT (High-Electron Mobility Transistor), the HFET (Heterojunction Field-Effect Transistor), the TEGFET (Two-Dimensional Electron Gas Field-Effect Transistor), or the SDHT (Selectively Doped Heterojunction Transistor), among others, was created in order to do this.

The first theoretical work relevant to the invention of the MODFET was done by Gai-Halasz, Chang, Tsu and Esaki at IBM in the late 60's. In this original work, they propose taking advantage of the conduction band discontinuity between AlGaAs and GaAs in order to separate carriers from the doping centers in a superlattice (multiple current path) structure as shown in Figure 2.4.

![Diagram](image)

**Fig. 2.4.** Separation of electrons from the doping centers and thus the scattering centers is achieved by doping the material with a high band gap and leaving the small band gap material undoped.
The standard MODFET consists of a single electron conduction layer where electrons settle in a highly confined region of undoped GaAs just below the AlGaAs/GaAs interface. The quantum nature of the confinement well (where the conduction band dips below the Fermi level in a region that is perhaps only 75 Å wide) allows for a very high concentration of electrons to settle in the well, permitting large screening effects and reduced scattering for electrons flowing parallel to the channel. A simple diagram of a MODFET which is based upon a single interface of the type shown in Figure 2.4 is shown in Figure 2.5.

![Diagram of MODFET](image)

Fig. 2.5. Schematic diagram of the structure of a MODFET alongside a conduction band diagram of the device. The channel electrons are confined in a very small space (approximately 75 Å thick) away from the dopant atoms.
MODFET devices offer further device performance advantages when compared to the simpler MESFET device. The wide band gap AlGaAs material allows for the application of larger forward bias voltages on the gate, increasing noise margins in digital integrated circuits. In concert with the confinement of the electrons adjacent to the interface, a smaller gate to conducting channel distance is obtained (200-300 Å), leading to extremely high transconductances. The high sheet density of electrons in the ungated channel ($10^{18}$/cm$^2$ or higher) leads to a large current carrying capability and the potential for a low source resistance. The screening and reduced scattering of carriers also reduce the noise figure of microwave devices.

In this work, we focus on the electron transport characteristics as they pertain to possible improvements in high speed performance. Because of the minimal scattering of electrons in the MODFET, it is the natural device to use to investigate the electron transport properties. Nonetheless, improper design of a MODFET can create, at bias voltages within the normal device operating range, a second, low mobility conduction path for the electrons in the AlGaAs. The next section illustrates just how this can occur and shows the difficulty in accurately measuring the mobility of such a structure using the common Hall effect method.

2.3 Parasitic MESFET—Second Conduction Path in a MODFET

If one designs a MODFET such that the AlGaAs layer is too thick for the given doping, e.g. if the thickness is greater than the sum of the two depletion regions under a given bias condition:

$$d_1 = \sqrt{\frac{2eV_b}{qN_d}} \quad d_2 = \sqrt{\frac{2eV_1}{qN_d}}$$

then a portion of the highly doped AlGaAs will not be depleted as shown in Figure 2.6.
Fig. 2.6. Conduction band diagram of a MODFET under zero bias with too thick an AlGaAs layer. Electrons can flow between source and drain in the undepleted AlGaAs.

Under this state, current can bypass the MODFET channel and flow through the AlGaAs layer as if it were a simple MESFET. This conduction path is aptly termed the parasitic MESFET, and is illustrated in Figure 2.7.

Fig. 2.7. Physical path of electrons in the AlGaAs layer (parasitic MESFET) in parallel with the normal MODFET conduction layer.

Once the parasitic MESFET begins to conduct current, the MODFET characteristics become difficult to analyze. In this situation, gate voltage variation will predominantly modulate the MESFET channel, while modulation of the two-dimensional electron gas will be greatly reduced. The mobility of (MESFET) electrons in the AlGaAs is much less than in the 2-DEG at the GaAs interface (by a factor of two or three at room temperature, an order of magnitude more at 77 K.) Since the transconductance is a function of both the concentration and velocity of the mobile electrons in the modulated region, one might expect to see two peaks in a plot of extrinsic
transconductance verses gate voltage in such a device. Figure 2.8 shows one of our devices that exhibited this double peaked behavior. Note the large negative threshold voltage in this device. One criterion for eliminating bad devices was to accept only those within a narrow range of threshold voltages near zero volts. This will become clearer when we see the simulations for the layer structures in Chapter 4.

Fig. 2.8. Low field transconductance of a bad device as a function of gate voltage. Note the second peak in the transconductance indicating current flow in the lower mobility AlGaAs layer.

Determination of the two dimensional electron mobility also becomes difficult when such a parasitic MESFET exists. This problem was observed even prior to the emphasis on small geometry devices.

Normally, if one has a single conductive layer, one can measure the mobility and sheet carrier concentrations of the layer by either the van der Pauw or the Hall bar method. The van der Pauw method was used to determine expected sheet carrier concentrations and mobility values for wafers described in later chapters. The principles involved in both methods are
illustrated for the less complex Hall bar case in the first section of Appendix A. However, one of the first MODFET samples tested behaved in a way that could not be explained by the simple model described above. The structure of the sample is illustrated in Figure 2.9. It consisted of a thick, undoped (1 μm) layer of GaAs grown on top of a semi-insulating substrate, followed by a 100 Å undoped spacer layer of Al₀.₃Ga₀.₇As and a Si doped (3 x 10¹⁸), 1000 Å layer of Al₀.₃Ga₀.₇As.

1000 Å Si Doped (3 x 10¹⁸/cm³) Al₀.₃Ga₀.₇As

100 Å Undoped Al₀.₃Ga₀.₇As

2-DEG

1 μm Undoped GaAs

Semi-Insulating GaAs Substrate

Fig. 2.9. Structure which shows a large degree of parallel conduction by virtue of a thick AlGaAs layer.

A Hall bar pattern was defined on the surface with a length of 1075 μm and a width of 125 μm. Center contact spacing was 290 μm, with the width of the center contacts defined at 5μm. Using the equations above, the mobility and sheet carrier concentrations were obtained. A plot of these values as a function of the applied magnetic field shows a strong dependance on field, indicating that multiple conductive paths exist. (Fig. 2.10)
A similar but much smaller magnetic field dependence of the Hall mobility was observed in the early fifties, when measuring Hall and magnetoresistance effects in high-purity p-type germanium\textsuperscript{11}. This was successfully modeled by considering the effect of two types of carriers (heavy and light holes) with different concentrations and mobilities\textsuperscript{12}. Several authors have tried to apply the same equations to the MODFET case\textsuperscript{13,14}. There is, however, a major difference in the MODFET structure—the two conduction paths are separated by a highly depleted AlGaAs layer. This layer effectively insulates the two paths except in the contact regions, causing a multitude of current loops due to the different potentials formed on the different levels. One possible method for extracting the mobilities and sheet carrier concentrations of each layer using a Hall bar is derived in Appendix A.

In the last few years, other authors have addressed this problem in other ways using van der Pauw or magnetoresistance measurements as a function of magnetic field to extract the respective mobilities and sheet carrier concentrations in multiple layer structures\textsuperscript{14-20}. 

Fig. 2.10. Directly measured Hall mobility as a function of applied B-Field. In the absence of multiple layers of conduction with different carrier mobilities, the Hall mobility should stay constant.
2.4 Layer Growth Techniques—Molecular Beam Epitaxy

The starting material for fabrication of a simple GaAs MESFET is fairly easy to make. One only needs to change the doping levels in the uppermost layers. Since one is not particularly worried about scattering centers, one can begin with a wafer sliced off a piece of high resistivity material, implant it with donors, partially anneal the damage away, and process the devices. However, the starting material necessary for MODFET fabrication is more difficult to produce. One needs to grow both the ultimate in high purity, single crystal material with a minimal number of scattering centers, as well as incorporate abrupt compositional and doping changes. In order to achieve this, one needs to employ specialized crystal growth techniques.

The oldest technique for the growth of these layers is the Liquid Phase Epitaxy (LPE) technique\textsuperscript{21-23}. Taking advantage of the solid-solubility curves for GaAs, one grows more GaAs or AlGaAs on top of the seed wafer by putting it in contact with a molten bath of As saturated Ga and lowering the temperature. Different doping or aluminum concentrations can be grown by using multiple baths with different compositions. This method, however, does not yield the atomically smooth, abrupt interfaces required for MODFET's and rarely produces the extremely smooth surfaces necessary for accurate submicron lithography.

An improvement can be realized by growing crystal material from source material in the vapor phase, usually tied up in a hydrocarbon molecule. These techniques include MOCVD (Metal-Organic Chemical Vapor Deposition) and MOMBE (Metal Organic Molecular Beam Epitaxy), a cross between MBE described below and MOCVD. However, carbon impurities from the carrier gas can degrade AlGaAs material properties\textsuperscript{24}.

For MOCVD an added problem occurs. Growth control is achieved by changing the gas flow to the chamber which operates near atmospheric pressure. While proper design of the chamber can reduce the problem, there is a lag time associated with removing the gases previously present. Only recently have structures with a few monolayers precision been successfully grown\textsuperscript{25}. This method's primary advantage is in its capability for high throughput.
For a research effort, however, high throughput is of no concern (though the magnitude of this advantage is open to debate). Thus the method of choice is growth by Molecular Beam Epitaxy (MBE). Employing an ultra-high vacuum chamber, the crystal is grown on the heated substrate from elemental beams of Ga, As, Al, and Si. Control of crystal stoichiometry is easily achieved due to the difference in sticking coefficients on the surface between As-As bonds (very low) and Ga-As bonds (almost unity). The crystal is thus grown in an As rich condition, and the growth rate is controlled by the Ga flux.

Each molecular beam is formed by heating highly pure elemental sources in boron-nitride crucibles to the point where the atomic vapor pressure becomes significant. While the chamber pressure may be as low as \(10^{-11}\) Torr before growth, the chamber pressure is typically in the \(10^{-5}\) Torr range during growth. At these pressures, however, the beam flux can easily be interrupted by placing a shutter in its path, a procedure that can be done in a fraction of a second. Given typical growth rates of 0.5 \(\mu\)m to 1.0 \(\mu\)m per hour, this allows for abrupt changes of doping or composition in the crystal on a monoatomic scale. Knowing precisely how fast growth is occurring allows for precise timing and growth of almost any structure. These methods include the use of such techniques as REED oscillations\(^{26}\) and a computer to control the shutters and temperatures. Figure 2.11 shows a schematic of a simplified MBE chamber. All wafers used in this study were grown using the MBE technique.

### 2.5 A History of Short Gate Length GaAs FET's

While FET's with sub-micron gate lengths have been around for quite some time, the effort to produce GaAs MESFET's and MODFET's with gate lengths of 0.1 \(\mu\)m or less has been going on for only the last three years. Due to the difficulties in transferring a pattern from the resist to an etched structure without loss of resolution, these initial efforts concentrated mainly on producing MESFET devices without any gate recess. Later, as the MODFET design necessitated a recess step, various methods of recessing the gate were tried.
Fig. 2.11. Diagram of a simplified molecular beam epitaxy system.
W. Patrick et al.\textsuperscript{2} were perhaps the first to report the successful fabrication of a GaAs MESFET with a gate length less than 0.1 microns. In their September 1985 paper, they describe the successful fabrication of GaAs MESFETs with gate lengths ranging from 0.36 \( \mu \text{m} \) to 550 Å. Starting from material grown by vapor phase epitaxy (VPE) with an 850 Å \textit{n+}-GaAs active layer doped to 1.5 \( \times 10^{18} \) cm\(^{-3} \), this group from Glasgow University in Scotland produced gates with a direct write electron beam exposure process. Their process involved two layers of PMMA, a 700 Å thick layer of high molecular weight PMMA (350 K), on top of a 900 Å, low molecular weight PMMA (135 K) layer. The undercut profile created with this resist process is described more completely in References 27 and 28. Recess of the gates was accomplished by etching each wafer in 10 second increments in a dilute hydrogen peroxide-ammonium hydroxide solution while monitoring the source-drain current. This procedure was successful because of the reasonably thick PMMA layer (1600 Å total) and an etch depth less than 200 Å. Results of these VPE grown structures were disappointing in that pinch-off did not occur in the smallest device above a 1.2 volt source to drain bias. It is surmised that the lack of an abrupt doping change at the interface due to the limitations of the VPE technique was responsible.

A group at IBM Zurich was able to manufacture GaAs MESFET's with gate lengths down to 1000 Å using a fully implanted process, making a gate recess unnecessary\textsuperscript{29}, since the implant depths can be controlled quite accurately without it. Active and contact regions were defined using separate direct-write e-beam steps on PMMA masked implants. Gate metallization was placed directly on the surface. However, their 0.1 \( \mu \text{m} \) device could not be turned off for source-drain voltages greater than 0.6 volts. Subsequently, IBM Zurich was able to fabricate a very high transconductance (580 mS/mm) recessed gate MESFET, but with a longer, 0.5 \( \mu \text{m} \), gate\textsuperscript{30}.

In all these short gate length structures, the high frequency performance of the device was severely limited by gate resistance. The resistance must be reduced to a minimum. Fabrication of a T-shaped gate, that which is short at the gate-GaAs contact area, yet flairs out above the surface of the GaAs in a T shape, is one obvious solution. Such a T-gate MESFET was
fabricated during the middle of 1985 by General Electric with gate lengths down to 0.25 μm. (Other T-shaped structures with footprints to 0.15 μm were also fabricated.) At the time, the noise figures were the best ever reported for a conventional MESFET (18 GHz, noise figure 1.4 dB with an associated gain of 7.9 dB)\textsuperscript{31}.

This past year, a group from Cornell was able to produce MESFET's with a room temperature transconductance ($g_m$) of 540 mS/mm for 1000 Å MESFET's with a small signal gain of 16 dB at 18 GHz\textsuperscript{32}. This was the highest reported gain at the time.

Meanwhile, fabrication of sub-micron MODFET's began in 1984 with Berenz et al.\textsuperscript{33} and Camnitz et al., a group from Cornell\textsuperscript{34-35}. Both groups reported gate lengths in their MODFET's as small as 0.35 μm. The first paper of Camnitz et al. describe devices with transconductances of 125 mS/mm and 210 mS/mm at 300 K and 77 K respectively. Gate etching was only 100 Å deep through a 350 Å $n^+$ GaAs layer and was accomplished with "wet chemical etching". In his later paper, Camnitz et al. describe a similar device, this time with transconductances of 450 mS/mm at 300 K and 580 mS/mm at 77 K for a 0.33 μm device. Here, gate recessing was accomplished by spray etching with a solution of H$_2$O$_2$ buffered to pH 7 with NH$_4$OH, selectively etching entirely through the GaAs cap layer of approximately 650 Å.

Most recently a collaboration between the National Nanofabrication Facility at Cornell and General Electric has been able to produce a number of devices with gate lengths down to 0.1 μm. Sub-0.1 μm MODFET's were reported by this group in 1987\textsuperscript{32}. Pseudomorphic MODFET's were later reported by this group\textsuperscript{36}, with gate lengths of 0.1 μm with $g_m$ of 540 mS/mm at room temperature. These devices again had record gain and noise results for MODFET's (MSG at 18 GHz was 18.2 dB, with a noise figure of 2.4 dB at 60 GHz and associated gain of ~6 dB). Ga$_{0.5}$In$_{0.5}$As/ Al$_{0.5}$Ga$_{0.5}$As MODFET's with 0.12 μm gate length T-gates were fabricated on a lattice mis-matched GaAs substrate and presented at IEDM\textsuperscript{37}.

A group at Hughes has also recently become active in producing 0.1 μm gate length MODFET's\textsuperscript{38}. This group demonstrated a 15 stage ring oscillator with 0.2 μm gate length
Al$_{0.48}$In$_{0.52}$As-Ga$_{0.47}$In$_{0.53}$As HEMTs fabricated on InP substrates\cite{39} with the shortest reported gate delay (9.26 ps at 66.7 mW/gate for Buffered FET Logic, 7.21 ps at 24.5 mW/gate for Capacitively Enhanced Logic, both at 300 K).

A number of theoretical papers have also been presented on the expected characteristics of small geometry MODFET's and MESFET's. MESFET papers of note include those by C. M. Snowden \textit{et al.}\cite{40}, A. Hiroki \textit{et al.}\cite{41}, and T. A. Fjeldly \textit{et al.}\cite{42}. MODFET papers include M. F. Abusaid \textit{et al.}\cite{43}, M. S. Gupta \textit{et al.}\cite{44}, and K. Yamasaki \textit{et al.}\cite{45}.
Chapter 3

Process Development

3.1 Introduction

Developing the process sequence used was a major task. Given the limited throughput of the electron beam system, the requirement that complete rows of devices were functional in order to make valid comparisons, and the lack of assurance that one was writing on the target die, achieving the highest yield possible for all of the other process steps was mandatory. The main steps are: 1) isolation of the active device areas, 2) formation of ohmic contacts to those areas, 3) etching of the protective cap layer (included for better contact) in the area of the gate and forming the gate itself, and 4) laying down thick metal pads for probing or wire-bonding the devices. Each step corresponds to one mask level. The development of the final sequence is described in this chapter. Essentially the same sequence was used for both MESFET's and MODFET's.

3.2 Mask Design

In designing the mask set, our main consideration was to fabricate a number of small gate length FET's, with the same source-drain spacing, as close together as possible; however, the pads had to be large enough to facilitate wire-bonding or to be probed directly. Our initial contact pad configuration was a compromise between the so called NBS-20 (National Bureau of Standards-20 Pin) configuration, for which probe cards were readily available, and the 150 μm center, four contact pattern necessary for probing with the high-speed Cascade® probes. (Initially two source pads were shorted together to form two grounds. A later revision of one the final mask levels replaced one of the source pads with another gate connection to allow contact to both ends of the gate. This prevented easy probing with the Cascade® probes for devices made
both ends of the gate. This prevented easy probing with the Cascade® probes for devices made with that mask set, but it increased chances for a working device.) However, for the portion of each die dedicated to process monitoring, only the NBS-20 pad configuration was used. Each die in the mask set was identical, with the process monitoring portion and two alignment mark patterns included on each die.

The process sequence can be best illustrated by a diagram showing the alignment mark pattern as shown in Figure 3.1. The mask set consisted of four separate levels, each generated in chrome on glass plates in a MEBES (Manufacturing Electron Beam Exposure System). The first mask was used as the isolation mask, labeled with an "I" within the alignment pattern. The second level was used to pattern the ohmic level metallization, labeled "Ω" on the alignment pattern. This level was designed to be aligned to the "I" level. The third level, labeled "M", was used to pattern the interconnect metal. A fourth level was generated for process testing as an optical gate mask, for use only during preliminary process testing, when electron beam gates were not to be included. This level was labeled "G". Both the "M" and the "I" levels were designed to be alignable to the ohmic level, since the ohmic level is much easier to see in the aligner than the mesa level. To reduce the chance of shorted devices, it was more important to align the "G" and "M" levels to the ohmic level.

Design of the alignment marks should not be rushed, as a well designed set allows for a much speeder completion of the alignment process. The set developed for this work was designed in order to make possible mask to mask alignment to within ±1/2 μm. Three groups of marks with different resolution were included, ranging from very fine to coarse. The coarse patterns included long line patterns to assist in wafer alignment in the non-ideal case of working with a quarter wafer or less. In this case, the angular degree of freedom is very difficult to ascertain due to the inability to use both eyepieces on the aligner. The medium and coarse pattern design was based on the alignment of short line segments and equalizing of open spaces. The finest patterns could barely be resolved, if at all, at 400x, and thus one needed to equalize the shades
Fig. 3.1. Diagram showing a close-up of the alignment pattern replicated twice on each die.
of color viewed through the openings to equalize the portion of metal seen underneath. (400x is a good compromise power for an aligner, having a reasonable depth of field, while allowing one to focus on the both the mask and a thick resist pattern, yet with enough resolution to accurately align mask to mask.) This concept is better illustrated in Figure 3.2.

![Diagram of structure showing principle of fine alignment mark design](image)

**Previous Layer**

**Hole in mask**

**Good Alignment**

**Poor Alignment**

Fig. 3.2. Diagram of structure showing principle of fine alignment mark design. When the given pattern is viewed through the hole shown, the difference in the amount of metal visible shows up as a coloration difference.

It should be noted that one must be careful when designing alignment patterns to take into account how much of the mask plate will be opaque. Otherwise the area available for viewing the substrate during alignment may only consist of a few small gate openings and a small alignment mark opening. This happened on an earlier MODFET mask set; it was impossible to align the mask even in a coarse fashion. Some levels of the present alignment marks, therefore, include large open areas in the course alignment area, despite the seeming waste of chip real estate.

An altogether different problem exists in the alignment of the electron-beam written gates. Each gate must be aligned individually to the ohmic metallization for proper placement. Viewing of the device area can only be done by using the electron column as a SEM (Scanning Electron Microscope). This exposes the viewing area, however, restricting viewing to outside the
device area. Therefore alignment must be done in an area close to the device, followed by a predetermined jump to the gate area just prior to exposure. The patterns to the right and above the device area, but within the ohmic contact pattern, permit precise alignment of the electron beam exposure system, as shown in Figure 3.3.

Fig. 3.3. Drawing of Pattern used on ohmic level for alignment of electron beam to device. Note pattern identification at left (on real devices the identification numbers are mirrored). Source and drain regions are outlined.

Each die consisted of a matrix of such device areas. Separation between each device area was 480 μm, with contact pads 100 μm x 100 μm square on 160 μm centers. Each row had a different nominal source-drain spacing in the ohmic contact metallization level. Row F was special in that the active device area was made large enough for the interconnect metal to connect to the
gate line within the active area. This eliminated the requirement that the gate metal run up the side of the mesa, should serious problems have been encountered with gate metal breakage. Identification of a specific device location on a given die is by this row letter and column number, patterned in the ohmic contact metallization, as shown in Figure 3.4. The rule used for the alignment of the interconnect metal level to the ohmic level was an overly conservative ±2 μm. Therefore, as summarized in Table 3.1, the mask designated interconnect level spacings are 4 μm larger than the source-drain (ohmic level) spacings.

<table>
<thead>
<tr>
<th>Row</th>
<th>Source-Drain Spacing</th>
<th>Interconnect Metal Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>10 μm</td>
<td>14 μm</td>
</tr>
<tr>
<td>B</td>
<td>5 μm</td>
<td>9 μm</td>
</tr>
<tr>
<td>C</td>
<td>3 μm</td>
<td>7 μm</td>
</tr>
<tr>
<td>D</td>
<td>2 μm</td>
<td>6 μm</td>
</tr>
<tr>
<td>E</td>
<td>1 μm</td>
<td>5 μm</td>
</tr>
<tr>
<td>F</td>
<td>2 μm</td>
<td>6 μm</td>
</tr>
</tbody>
</table>

Table 3.1. Source-drain spacings by row identification number alongside the interconnect level metal spacings.

A number of process monitoring areas were also incorporated into the die. Interdigitated finger patterns were included on both the isolation, interconnect and ohmic metallization levels with line and space patterns of 1, 2, 3 and 4 μm's. These turned out to be extremely useful, not only in determining the metallization integrity, but also in determining the resist development endpoint. Standard four point transmission line patterns were included for active area resistance measurements, giving a rough idea of the ohmic contact resistance. These consisted of isolated lines of varying width (labeled on the mask) with similar distances between the probe points. Table 3.2 summarizes the nominal geometries of each line, the distance between the points, and thus the calculated number of squares subtended. A further description of the use of these structures is included in a later section.
<table>
<thead>
<tr>
<th>Nominal Width (µm)</th>
<th>Nominal Length</th>
<th>Total Resistance Squares (Nominal)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 µm</td>
<td>140 µm</td>
<td>7</td>
</tr>
<tr>
<td>10 µm</td>
<td>140 µm</td>
<td>14</td>
</tr>
<tr>
<td>6.5 µm</td>
<td>140 µm</td>
<td>21.5</td>
</tr>
<tr>
<td>6 µm</td>
<td>140 µm</td>
<td>23.33</td>
</tr>
<tr>
<td>5 µm</td>
<td>140 µm</td>
<td>28</td>
</tr>
<tr>
<td>4.5 µm</td>
<td>140 µm</td>
<td>31</td>
</tr>
<tr>
<td>4 µm</td>
<td>140 µm</td>
<td>35</td>
</tr>
<tr>
<td>3 µm</td>
<td>140 µm</td>
<td>46.66</td>
</tr>
<tr>
<td>2 µm</td>
<td>140 µm</td>
<td>70</td>
</tr>
<tr>
<td>1.5 µm</td>
<td>140 µm</td>
<td>93.33</td>
</tr>
<tr>
<td>1.25 µm</td>
<td>140 µm</td>
<td>112</td>
</tr>
<tr>
<td>1 µm</td>
<td>140 µm</td>
<td>140</td>
</tr>
</tbody>
</table>

Table 3.2. Transmission line dimensions and associated number of squares subtended.

Total die size was 3400 µm x 4800 µm. Center to center spacing of each die on the mask was 4000 µm in the horizontal and 5400 µm in the vertical. This left a scribe area of 600 µm on all sides. Additional structures in the device area included a wide device without a gate connection, a pad for capacitance vs. voltage (C-V) profiling, and a series of Kelvin resistance structures.

Figure 3.4 shows a diagram of the complete mask set.
Fig. 3.4. Diagram of the complete mask set. Alignment marks are at the bottom, with transmission line and ohmic contact patterns at the top. Individual devices are in the center region by row number.
3.3 Isolation: Ion Implantation vs. Mesa Isolation

Electrical isolation of the active area of each device is typically done by etching the layer or reducing the conductivity by compensating or trapping the prevalent carrier type. For GaAs devices, fabricated with epitaxial growth on insulating substrates as in this work, this layer is extremely thin, making both approaches relatively easy.

The preferred method is that of conductivity reduction so as to keep the surface as smooth and planer as possible for future lithographic steps. The idea is to create a sufficiently large amount of damage in the GaAs (which is not annealed out) by firing high energy ions into the substrate. A variety of ionic species have been used for this purpose, including protons\textsuperscript{46}, boron\textsuperscript{47}, and oxygen\textsuperscript{48}. The main requirement for choosing the ion species is that they are reasonably light (so that they can penetrate well into the sample) and they do not react with the GaAs under specific processing temperatures to create a doped piece of material (thus lowering its resistivity.)

It sometimes becomes necessary to do a multiple implant to properly isolate the device, since each implant causes damage only within a region described as a Gaussian profile \((R_p \pm \Delta R_p)\). Prior to our emphasis on small gate lengths, we were able to increase sheet resistivity in a MODFET structure (with the two-dimensional electron gas 1100 Å beneath the surface) from 630 \(\Omega/\text{square}\) to over 5 \(M\Omega/\text{square}\). A single layer of thick photoresist was used to mask the ions. \(N_2^+\) ions were first implanted with a dose of \(5 \times 10^{12}/\text{cm}^2\) at 60 keV and again at 80 keV using the same dose. \(N_2^+\) was another ion that was easy to obtain and work with, and was, like boron, oxygen and hydrogen, expected to remain stable, yet cause a sufficient amount of damage to properly isolate the device.

One problem with the use of ion implantation for this work, in conjunction with a thick patterned photoresist layer as the implant mask, was the intermittent existence of an extremely tough to remove, visible scum, left over after the photoresist layer had been removed. This was
unacceptable. One possible option to get around this problem might have been the use of a metal layer to stop the implant, however this would have introduced a large amount of complexity into the process.

Another concern with the use of ion implantation for isolation was that damage in the wafer in close proximity to the device could conceivably cause a high concentration of traps and reduce the sheet carrier concentration in the two-dimensional electron gas layer. At the very least, one should expect to see a smaller effective width for the transistor. As it turns out, mesa isolation produces a reduced active region as well\(^{49}\), however, the effect of damage induced traps was a larger unknown. It was thus decided that complete removal of the conductive layer, i.e. mesa isolation, would be preferable.

Etching solutions will be discussed in detail later when gate recessing is discussed. For this portion, suffice it to say that a 1:1:20 mixture of NH\(_4\)OH:H\(_2\)O\(_2\):H\(_2\)O was used to etch the mesas, using a patterned layer of well-baked (30 minutes at 120 °C) photoresist as a mask. The etch rate was observed to be initially 1 \(\mu\)m/minute immediately after mixing up the solution, dropping to about 0.8 \(\mu\)m/minute after two hours.

One major advantage of mesa isolation is the ability to take advantage of the crystallographic orientation dependance of the etch. The 1:1:20 mixture of NH\(_4\)OH:H\(_2\)O\(_2\):H\(_2\)O forms a gradually sloping angle of approximately 54.7° by revealing the Ga\{1\(\bar{1}\)1\} plane along the [0\(\bar{1}\)1] direction\(^{50}\). Along the [01\(\bar{1}\)] direction the Ga\{2\(\bar{2}\)1\} plane is revealed, which, in principle, forms an angle of 109.5° to the (001) surface plane. In combination with a similar situation which occurs during the gate recess (as will be described later), proper orientation of the wafer reduced the possibility of gate metal breakage over the step into the active area. This is illustrated in Figure 3.5 below.
Fig. 3.5. By proper orientation of the wafer, one can take advantage of the sloping edge to prevent the thin metal line from breaking as it runs into the active area. A further advantage is as an etch assist for the gate.

As an aside, it should be noted that there is disagreement in the literature over which direction forms the 54° sloping edge. My observations in combination with the manufacturer's specifications confirm the work of Adachi et al.\(^{50}\) (as diagramed in Figure 3.5), while Williams\(^{51}\) seemingly describes a situation with the directions reversed. Thus a test sample should be attempted before etching the first real wafer.

### 3.4 Lift-off Techniques

After isolation of the device active areas from the rest of the wafer is complete, ohmic contact must be made to the source and drain regions. This metallization is patterned by again transferring the mask pattern first to photoresist previously deposited on the wafer, and then to a metal layer. This is described below.

For patterning of metal layers on compound semiconductors such as GaAs, deposition everywhere followed by etching of unwanted metal through a photoresist mask is unacceptable. In contrast to the single layer Al metallization used in Si processing, GaAs ohmic, interconnect, and gate metallizations consist of multiple metals with an Au base which are much more difficult to etch\(^{51,52}\). Many metal etches also attack GaAs. For geometries of less than 2 \(\mu\)m, one must use dry etching to etch the metal, perhaps causing radiation damage in the GaAs. Unlike Si, this
damage is not readily removed by annealing. Gold poses a special problem, in that even during deposition at a slightly elevated effective temperature, gold spikes similar to stalactites penetrate into the GaAs crystal, destroying crystal uniformity. This is helpful in forming better ohmic contacts, as will be discussed later, yet is disastrous in device active areas.

Instead, a technique known as “lift-off”, developed in conjunction with electron-beam lithography twenty years ago, is used. This technique involves deposition of the metal layer(s) directly on top of the patterned resist, followed by lift-off of the unneeded metal by dissolving the underlying photoresist, usually with acetone or other organic solvents. The only serious disadvantage to the lift-off technique is that the resist is easily heated too hot during metal deposition. Above about 200 °C resist cross-linking occurs, while at a temperature only slightly warmer, resist carbonization occurs, making it difficult to impossible to remove the resist. In earlier stages of this work when a filament evaporator was used to deposit metal films, a few samples were ruined as a result. It was possible to use such a filament bell jar evaporator only by carefully controlling the time and power to the evaporating filament.

In theory, when compared to methods involving metal etching, better resolution is possible for sub-micron geometries using a lift-off process rather than a metal etch. During etching, significant undercutting of the metal can occur under the etch mask. However, for the lift-off method, great care must be taken in the formation of the resist profile in order that the metal actually comes off the covered areas with good edge definition. There must be a discontinuity between the metal on the GaAs surface and that on the resist layer, not only to allow solvent to penetrate and dissolve the photoresist, but also to prevent ragged edges or inaccurate patterning due to tearing or peeling off of the metal in areas where it should remain. In cases of very thin or brittle metals (this does not include gold), lift-off may still be partially successful where the discontinuity does not exist, though metal edge definition may be poor. With thicker gold films, the metal may not lift off at all, leaving a sheet of metal covering the whole wafer. Should this
occur, the wafer is unusable. Figure 3.6 shows an example of a side view of a poor lift-off profile along side an ideal profile.

The rest of this section will be devoted to exploring the methods used to achieve a good resist profile and thus achieve good lift-off.

![Diagram](image.png)

Fig. 3.6. Ideal vs. non-ideal lift-off profiles. (a) An example of a poor lift-off profile after metal deposition. Should the metal come off the surface at all, one will be left with jagged metal edges as in (b). Metal definition on the surface will be poor from tearing during lift-off. (c) An example of an ideal lift-off profile. Overhang of the photoresist prevents a continuous sheet of metal from forming during deposition.

3.4.1 Single Level Lift-off

The simplest method of doing lift-off is to deposit a thick layer of photoresist on the wafer, develop it carefully to minimize the sloping edges, deposit a thin, brittle metal, and lift-off. This is extremely difficult due to the attenuation of uv light in the photoresist, as well as standing wave effects generated by reflected light from the substrate. Recently a technique using this attenuation to one's advantage has been developed and is in use at a few companies. It involves use of an image reversal technique by exposure of the photoresist to ammonia gas. However, this process is prohibitively expensive to set up in a research lab, and was not readily available when lift-off decisions were made for this work. As an aid to lift-off, several Japanese
companies\textsuperscript{58} use a cotton swab to mechanically scrub off the remaining metal. Though it is definitely open for debate, the general rule of thumb is that if you have a brittle metal (not gold), a metal thickness of less than half the thickness of the photoresist layer replicates the desired pattern in the metal film. It has been my experience, however, that for repeatable metallization this limit is greatly exaggerated. For line widths of a micron or so where use of a cotton swab would not be acceptable due to the fragile nature of the small structures, and where the resist edges are not unduly sharp, a thickness ratio of 1:10 is preferable. Yet this rule will usually work when the geometries are large (10 $\mu m$ or so) and one is not worried about maximum yield or cleanliness, since the cotton swab is not really clean room compatible. We were, however, extremely concerned with having as large a yield and as uniformly sharp a metal profile as possible, as adjacent devices need to be functional, and a limited number of gates could be written.

In some cases, if the underlying substrate is etched prior to metallization with the same photoresist etch mask, the undercut of the substrate material assists in lift-off. This is crucial in the gate formation, as is described in Section 3.6.

3.4.2 Chlorobenzene Assisted Lift-off

In 1977 B.J. Canavello\textsuperscript{59} \textit{et al.} developed the basis for the so called chlorobenzene lift-off method. The process consists of soaking the resist layer in chlorobenzene (other aromatic solvents such as toluene or benzene work also) either before or after ultraviolet exposure. This modifies the top portion of the resist, making the soaked portion of the resist less soluble in the developer solution. The chlorobenzene, however, penetrates the resist very slowly (the extent to which it does will be referred to as the penetration depth), allowing the majority of the resist, which is not penetrated during the soak time, to retain its original solubility. As it turns out, the soaking process is most effective when performed after exposure and prior to a short bake\textsuperscript{60}.

During the development step, the developer is thus presented with four separate areas which will develop at different rates. In the exposed region, the developer first proceeds to slowly
erode the soaked layer until the un-soaked layer is reached. At this time the developing rate increases, such that the exposed, un-soaked region is easily removed. A slight overdevelopment, therefore, should remove a fraction of the un-soaked, un-exposed resist, forming a lip consisting of chlorobenzene treated photoresist. An outline of the process is given in Figure 3.7.

This chlorobenzene lift-off process was developed further by Hatzakis et al.\textsuperscript{61}, and has since been used extensively in many labs for GaAs circuit fabrication. It spite of its widespread use, the very mechanism by which chlorobenzene works is still poorly understood, and the method has a number of unpredictable quirks.

The optimization of the process is extremely difficult. The combined effects of soaking and baking define the all important penetration depth of the chlorobenzene. As Collins et al.\textsuperscript{62}, who go into great detail about the various parameters that one must consider, caution, “too little ... penetration creates an unstable structure with insufficient overhang. Too great a penetration produces structures with poor liftability because of reduced neck height.” Complications include the fact that the top surface of the unexposed region is simultaneously (though slowly) developed away along with the exposed region. This fact makes mid-course correction on a single run chancy, if not impossible, should it be noticed that there is insufficient overhang in the developed structure. The penetration depth must be of sufficient thickness and the development of the exposed region (including the over-development time) of sufficient speed that the lip will retain its structural stability even after it has been thinned during development. Further development, should it become obvious that a variable in the process changed, could just as likely destroy the lip completely as increase the overhang dimension. For a given penetration depth, one must optimize both development and exposure times to have a good, reproducible overhang structure.
Fig. 3.7. Sequence of steps used in the chlorobenzene lift-off process.
However, achieving a repeatable value of the penetration depth is nearly impossible. Some believe that several of the earlier papers even give incorrect data when describing the changes that occur with various changes in process variables. It has been said that the bake temperature must be controlled to within $\pm 1/2 \, ^\circ C$. It has even been alleged that changing lot numbers of chlorobenzene requires a complete re-optimization. Y. Mimura et al. states that a "slight time difference between the solvent soak process and the development process exerts a considerable effect on stencil profile." He also states other "unexpected failures" in the profile production process. His paper in 1986 continues the attempt to show how the whole process works, showing by gel permeation chromatography that the profile formation is controlled by the removal of photoactive compounds (PAC) from a resist film. This contradicts an earlier paper by Halverson et al., which states that PAC removal was minimal and played no major role. Halverson instead cites the removal of residual casting solvent and low molecular weight resin species. Needless to say, the process is neither fully controllable nor fully understood. Portions of IBM (where the process was developed) and other companies involved in the fabrication of GaAs integrated circuits no longer use the chlorobenzene process for their III-V circuits for this reason.

After spending a number of months striving for repeatability in the development of this process, albeit without ovens that were controllable to the extent later alleged to be necessary, it was decided that this method was not suitable. The observation of Allison et al. proved to be true: "Considerable process development is generally required to perfect the chlorobenzene method for a given application." Faith was lacking in the method to produce repeatable line widths on devices with the best of yields. Due to possible contamination from resist residue and further unnecessary processing, we did not wish to be continuously stripping off the resist and starting over again. A much better way was at hand.
3.4.3 Two Level Lift-off with Plasma Buffer Layer

Given the problems described above with the other methods used for patterning the photoresist for lift-off, a method was chosen that was originally developed by Cantos and Dobkin \textit{et al.}\textsuperscript{66,67} based on work by C. Li and J. Richards\textsuperscript{68}. It consists of first spinning a layer of AZ1370-SF photoresist on the wafer, prebaking it for 30 minutes at 85 °C, and then exposing it to a C\textsubscript{2}F\textsubscript{6} (or in his paper a CF\textsubscript{4}) plasma. Fluoridation of the upper surface of the resist causes a thin layer of Teflon like material to be formed. A second layer of AZ-2400 photoresist can then be spun on and pre-baked without danger of resist intermixing. After ultra-violet (uv) exposure, the top layer is developed, the Teflon layer preventing developer penetration into the lower layer. Exposure to an O\textsubscript{2} plasma for a short time destroys the Teflon like layer along with an equal amount of the top resist layer. AZ Concentrate developer is then used to develop out the bottom layer. The AZ Concentrate does not attack the top 2400 photoresist. Metallization of the whole area can then commence. Lift-off in acetone completes the process. Figure 3.8 illustrates the sequence.

It is true that this process is perhaps more complicated than the standard chlorobenzene process, but it has the major advantage, especially for research purposes, of being adjustable midway along the process. Line widths can be monitored and the wafer checked to be sure the top layer is developed. If the C\textsubscript{2}F\textsubscript{6} treated layer begins to break down, this is visible, and the top layer development time can thus be adjusted. O\textsubscript{2} plasma times are not critical and can be longer than necessary. Finally, the overhang distance can be monitored by observing the edge profile in a good high power optical microscope and the lower resist layer developed further if necessary, assuring one of a good resist profile for lift-off. The chlorobenzene process does not allow this flexibility, as further development will simultaneously alter line width and overhang distance in an unpredictable manner as described previously.
Spin AZ 1370-SF Photoresist

Resist

Substrate

Modify with Freon-116 Plasma

Teflon like layer

Spin AZ 2400 Photoresist

AZ-2400 Resist

Develop Top Layer

Oxygen Plasma

Develop Bottom Layer

Metalize

Lift-off

Fig. 3.8. Steps used in the two-level, plasma treated lift-off method.
Another advantage of this process is that, while the line width is determined by a single layer of resist, the total thickness of the resist is the equivalent of two layers. Each layer was spun on at 5000 RPM, yielding a thickness of about 1.1 μm for each layer for a total of 2.2 μm, greatly assisting in lift-off by increasing the resist area exposed to the acetone. The thick resist layer also allows a fraction of the top portion of the resist to overheat (becoming cross-linked and thus insoluble in acetone) during metal deposition. Lift-off may still be successful because the thick underlying resist will allow the overheated layer to lift-off with the metal.

In the best cases, the metal would come off the wafer in less than a minute in a single sheet without any assistance. However, in some cases, assistance came from an artist's type air-brush filled with acetone. This fine spray of acetone helped remove fine particles of metal, especially when it came to lifting off the thin gate metal. The air-brush proved to be much cleaner, more controllable, and far gentler than a cotton swab.

3.5 Ohmic Contacts

It was very important to get the best ohmic contact possible for these devices. To compare devices, it is necessary to determine the intrinsic transconductance \( g_{mi} \) from the extrinsic or measured transconductance. Assuming no correction for output conductance, we have:

\[
g_{mi} = \frac{g_{mx}}{1 - |R_s|g_{mx}},
\]

where \( g_{mx} \) is the extrinsic transconductance and \( R_s \) is the source resistance (ohmic contact resistance plus sheet resistance of channel). Therefore, in order to reduce the error in the calculated intrinsic transconductance generated from measurement error in the source resistance, a low source resistance must be obtained. The ohmic contact resistance is usually a major portion of \( R_s \) in a small MODFET. For a 10 μm FET (the size of devices presented here) with
an intrinsic transconductance of 600 mS/mm and a source resistance of 83 Ω, the measured transconductance will be roughly 400 mS/mm. If the source resistance is 33 Ω, the measured value will be 500 mS/mm. Unfortunately, there is no agreement as to how to make the best ohmic contact.

Recently, uniform ohmic contacts to n-type GaAs have been formed with InAs. InAs abruptly grown on n-GaAs by MBE has formed successful contacts with only a 0.2 eV barrier before any anneal. An 800-850 °C anneal for several seconds removed this barrier\textsuperscript{69,70} forming contacts with resistivities as low as 1x10\textsuperscript{-6} Ω cm\textsuperscript{2}. Success has also been achieved with graded \textit{In}_xGa\textsubscript{1-x}As layers grown on top of n-type GaAs\textsuperscript{71}. A thermally evaporated layer of In formed a similar structure\textsuperscript{72} with a resistance value of 1x10\textsuperscript{-5} Ω cm\textsuperscript{2}. The addition of a nonreactive Pt layer prior to In evaporation reduced the contact resistance to 2x10\textsuperscript{-6} Ω cm\textsuperscript{2} by improving surface morphology in the layers\textsuperscript{73}. Another metal which gives similar results as an intermediate layer is Pd. While Pd does not of itself form an ohmic contact to GaAs\textsuperscript{74,75}, the In/Pd metallization sequence does, with the In diffusing through the Pd film (forming In\textsubscript{3}Pd during deposition). For a GaAs layer doped to 2x10\textsuperscript{18} cm\textsuperscript{-3}, a contact resistance of 0.7-1.5x10\textsuperscript{-6} Ω cm\textsuperscript{2} was obtained with uniform interface morphology\textsuperscript{76}.

The traditional AuGe/Ni/Au system has been employed for a longer time. Ever since Braslav et al. introduced the evaporated AuGe eutectic with a Ni overlayer\textsuperscript{77}, overcoming the serious diffusion problems associated with the use of Sn, the AuGe/Ni system has been in widespread use. Extensive study of the system has ensued\textsuperscript{78-81}, including a number of review papers as referenced by Braslav\textsuperscript{82}. A GeAu alloy forms at the GaAs surface which mixes with the GaAs\textsuperscript{78}. It is hypothesized that during anneal, the germanium diffuses into the GaAs and occupies the gallium sites, acting as a donor in the GaAs. The use of Ni was shown to be a help in making the interface more uniform and stable\textsuperscript{83}. Ni tends to help wet the GaAs surface, reducing balling of the metal, forming smoother metal edges. The presence of nickel in the alloy process seems to generally assist in reducing the contact resistance, perhaps by reacting with surface
oxygen. However, for long anneal times and temperatures, the ohmic contact quality was reduced. T. Kuan was among the first to publish an extensive study of the contact area using Transmission Electron Microscopy (TEM) and SEM. Studies have even been done on ohmic contacts to the two-dimensional electron gas found in MODFET's in this system, the orientation dependance of the contact, and even on the effective reduction of the source-drain spacing due to the metal diffusion (0.15 μm per contact at 420 °C, 30 second anneal). While other variations have been proposed using a Ge/Au based system (e.g. the Pd/Ge/Au system with its claim of smoother surfaces and better defined edges, or the addition of Ag to the metallization), we decided to use the AuGe/Ni system given the large amount of experience with it around Stanford.

After trying a few specific proportions of Ge, Au, and Ni in different orders, the following metallization sequence was settled upon for use in all of the devices presented here. It consisted of 200 Å of Ge, 500 Å of Au, 250 Å of Ni and 1000 Å of Au deposited sequentially using an electron beam evaporator. After lift-off, the layers were annealed at 450 °C for 30 seconds in a furnace or rapid thermal (RTA) annealer.

3.6 Gate Formation

Without taking extraordinary measures, the wavelength of light limits the size features that are reliable and reproducible with optical lithography to the order of a half a micron. While elaborate techniques such as angle evaporation or multilevel schemes with absorptive layers have produced, in isolated areas, feature sizes that approach a tenth micron, optical lithography is not suitable to repeatably pattern devices the order of tenth micron or below.

As far back as 1960, when optical lithography was capable of producing 10 μm features, Mollenstedt and Speidel demonstrated the capability of electron beams to create sub 0.1 μm features on thin electron-transparent membranes thereby reducing backscattering effects. By
1978, 250 Å metal lines with 500 Å periodicity were possible using polymethylmethacrylate (PMMA) as the electron sensitive material. Again using PMMA, Craighead et al. in 1983 produced 100 Å lines on 500 Å centers on bulk substrates. PMMA thus has more than sufficient resolution and adequate sensitivity to meet our needs.

Because the electron beam system employed electrons of a maximum energy of 40 keV, the PMMA thickness was limited to no more than 800 Å to maintain resolution. The thinness of the PMMA layer, however, made our second problem worse—we were attempting for the first time to repeatably and reliably recess (to a depth of as much as 800 Å) 500 Å gates in MODFET structures. The use of the patterned PMMA as the etch mask was necessary, despite the extremely fragile nature of the thin PMMA. Our plan of attack was then to first deposit PMMA onto the surface of the wafer, pattern the PMMA, recess the gate by careful etching, deposit the gate metal and then lift-off the unwanted metal.

3.6.1 Patterning

T. Newman et al. had developed, at Stanford, the e-beam patterning technology to generate metal dots 200 Å in diameter, on 500 Å centers on bulk GaAs. His technique was to first spin on a layer of PMMA (molecular weight of the polymer: 950,000) dissolved in chlorobenzene to a solid concentration of from 0.8% to 1.75% at a spin speed of 8000 RPM, resulting in a film thickness of 250 Å to 650 Å. The PMMA was then pre-baked at 175 °C for a minimum of 4 hours. A custom designed ultrahigh resolution electron beam exposure system with a minimum beam size of 50 Å was then used to write the dots on the PMMA. The exposed wafer was placed in a 3:7 mixture of cellosolve:methanol for 7 seconds to develop the PMMA, followed by a 30 second rinse in pure methanol. An alloy (60:40) of gold and palladium 100 to 200 Å (the maximum expected to lift-off successfully) was then deposited by thermal evaporation and lifted off in boiling acetone in an ultrasonic bath.
There were a number of modifications that had to be made to the above process in order to adapt it to this work. Before any processing with wafers could be attempted, it was necessary to modify the electron beam exposure system so that it could write lines instead of dots, and create a large square area adjacent to the gate line for contact to the interconnect metallization or for direct probing. It was decided that it would be best to create two such patterns, one above and one below the gate, in case the gate metal was not continuous. Line doses were optimized to range from 1.3 to 5.0 nC/cm, with gate dimensions less than 1000 Å determined strictly by the dose used in a single pass of the electron beam. Taking into account the scattering of the beam off the GaAs and within the PMMA, it was felt that lines as small as 350 Å could be written. Figure 3.9 illustrates the pattern the electron beam would take to expose a single small gate.

![Diagram of electron beam travel when writing the gate.](image)

The requirement that we maximize the gate conduction, along with the expectation of metal step coverage difficulties, dictated that a 200 Å thick gate was insufficient. Thus, we needed to use the maximum thickness of PMMA possible without sacrificing line width resolution. Fortunately, the 500 to 2000 Å gate recess necessary for the desired device design provided an undercut region underneath the patterned PMMA that would help maximize the metal thickness that we could successfully lift-off. Another consideration was the possible collapse of the resist film should it be too thin. We decided to use a 2% solution of PMMA dissolved in chlorobenzene, giving a resist thickness of between 600 and 700 Å when spun on at 5000 RPM.
Another concern was that the metal would separate from the substrate during the final lift-off process. This would be very difficult to detect, and would reduce reliability of comparative data between devices. Therefore, an ultrasonic bath was not used. In its place, an air-brush setup, as described previously, was employed. Partially as a result of this milder treatment, however, the main mode of device failure was metal occasionally not lifting off where it should have. Figure 3.10 shows a dark field image of such a device; the metal seems to be attached to the surface only along the mesa etch boundary, possibly because the PMMA was too thin at the ridge when applied. A photomicrograph of a device showing an etch line right on the step corner confirms this hypothesis (Fig. 3.11). It should be noted, however, that, in such cases where lift-off was unsuccessful, very careful probing with a Micromanipulator® probe was sometimes able to remove the unwanted metal and resurrect the device.
Fig. 3.10. Dark field image of a device where gate metal lift-off was not successful. Note the extra metal buckling over the ohmic contact region. The metal extending to the gate and the gate itself are not visible in this picture.
Fig. 3.11. Photomicrograph of device with etch line along mesa step edge. PMMA coverage was not sufficient to prevent citric acid etching and hence metal lift-off in this area becomes questionable.
3.6.2 Gate Recessing—Etch Selection

Development of a recess gate process was quite a challenge. Typical gate recesses include both selective and nonselective etches. Given the geometries involved and thus the high degree of accuracy required, it seemed at first like a selective etch for GaAs over AlGaAs was the best procedure.

In general, the best etching uniformity is one achieved by dry etching techniques. In this case, however, it would have made the processing extremely complicated. In order to achieve sub tenth micron lines, the PMMA was made so thin that it would not withstand dry etching, thus the only possibility would have been to transfer the developed PMMA pattern to a thin layer of metal. The normal rule of thumb for RIE (Reactive Ion Etching) is to have at least two to three times the etch depth in resist thickness. Because of the resist thickness limitations, RIE was out.

The most common selective etch for GaAs over AlGaAs is the so called, superoxol etch$^{99,100}$, comprised of straight 30% by weight H$_2$O$_2$ (hydrogen-peroxide) with a very tiny amount of ammonium hydroxide added to make the resulting pH equal to 7.05±.05. GaAs, however, tends to be removed in sheets with the superoxol etch, which may lead to poor uniformity on the scale of tens of Å. One might expect this sheeting effect to be common to all high concentration peroxide etches, as the etching of GaAs involves two steps, the oxidation of the GaAs with the peroxide and the subsequent removal of the oxidized GaAs into solution with the associated acid or base. Selective etches rely on the second step being rate limiting$^{101}$. The superoxol etch also creates a serious problem for this process as it attacks the PMMA (albeit slowly) as described below.

In the category of nonselective etches, the most common ones are again combinations of either acids or bases with hydrogen peroxide, diluted with water to slow them down (but this time much less peroxide)$^{50,102,103}$. These include phosphoric acid-peroxide and ammonium hydroxide-peroxide among others. These are useful when one has a very thick layer of well
baked photoresist, as in the mesa isolation step described previously. In this case, however, there is only 600 Å of PMMA protecting the surface. Immersion of a PMMA coated surface into both of these etches either removed or visually altered the appearance of the PMMA within as little as a few seconds. This was obviously not satisfactory for a well controlled etch. It is true that Patrick et al.\textsuperscript{2} used an ammonium hydroxide-peroxide etch to recess their gates, but their technique was to repeatedly dip the sample into the etch for 10 seconds at a time so that resist degradation was minimized, and to thus hope that the PMMA was not severely damaged. They also had the advantage of a PMMA thickness that was twice as thick as that employed here (a two level system consisting of 700 Å of high molecular weight (350,000) PMMA on 900 Å of low molecular weight (135,000) PMMA). Our aim was to obtain the best yield that we could get, so that a device comparison would be as valid as possible. We had to use some form of weak (probably organic) etch that would not attack the PMMA at all.

A number of etches were tried by Jones\textsuperscript{104} in an attempt to solve a similar problem, yet with a much thicker PMMA layer (7000 Å). It should be noted that he tried a very dilute ammonium hydroxide (NH\textsubscript{4}OH), hydrogen peroxide (H\textsubscript{2}O\textsubscript{2}) and de-ionized water (H\textsubscript{2}O) etch in a 1:2:400 ratio. This gave an etch rate with the right order of magnitude for gate etching. However, he found that the undercut was excessively large. At etch rates greater than one minute, he observed that the PMMA started to peel up. He cites the explanation of Levy et al.\textsuperscript{105} who concludes that “the relatively electron deficient nature of the GaAs (100) face makes it susceptible to competition for surface bonding by OH\textsuperscript{-} groups. Hence, if a resist such as PMMA is used (which lacks OH\textsuperscript{-} groups), a basic etch should not be used (which would compete for surface attachment).” Better adhesion was found using an acid based etch.

Within the acid based etching system, their first idea was to reduce the etch rate of the phosphoric acid peroxide base etch system by a combination of dilution and increasing the viscosity of the solution. Dilution with ethylene glycol slowed the etch rate, but also destroyed
uniformity. They finally settled on a high phosphoric acid concentration: acetic acid: peroxide etch, a very viscous etch which they said was able to reduce the undercut to 1000 to 2000 Å.

What was needed for this work was an etch that would not touch the very thin PMMA surface. Any resist uplifting was totally unacceptable. As opposed to the process of Jones, a very nonviscous etch was desired, such that mixing and wetting of the very small openings would not be a problem.

Otsubo et al.\textsuperscript{106} describe the properties of the citric acid: peroxide etch system. It was claimed that it would not attack PMMA, but would etch GaAs (and AlGaAs) quite well. The fact that the etch would not attack PMMA, however, also implied that it was a relatively weak etch. Citric acid based etches had come into disuse in GaAs processing because of the etch's inability to cut through any contamination present on the GaAs surface. This was obvious when we tried and failed in our first few attempts at etching through a scratch in a PMMA film. Yet it was felt that this was the proper direction to take, and effort should be concentrated on surface contamination elimination. (A further, more recent discussion on the citric acid etch system can be found in M. Schneider et al.\textsuperscript{107})

Another advantage to using the citric acid based etchant was the ability to take advantage (as in the mesa etch case with the ammonium hydroxide based etch) of the crystallographic orientation to form advantageous etch profiles. The situation is more complex than for the ammonium hydroxide case. Multiple planes are revealed by cleaving along a (0\textsuperscript{1}1) direction when etching in GaAs, forming a structure resembling a hand-drum, instead of the reverse mesa-shaped structure seen in sulfuric acid or ammonium hydroxide based etches (Fig. 3.12)\textsuperscript{106}. This would still tend to assist in cleaning out the bottom surface of a recessed trench. As the percentage of Al is increased, the etch gradually becomes more isotropic\textsuperscript{107}. However, the region that we are mostly concerned with is the upper GaAs highly doped cap and the possibility of its shorting to the gate. Almost all of the etching takes place in this top layer, so the isotropy of the etch in AlGaAs is unimportant.
Fig. 3.12. Typical etch profiles for the citric acid based etch in GaAs. Two cleavage directions are shown: (a) (100) the plane and (b) the (011) plane. From Otsubo et al.¹⁰⁶

Adachi et al.¹⁰⁸ also suggested an etch solution composed of HCl, CH₃COOH, and K₂Cr₂O₇ aqueous solution which they claimed did not attack such photoresists as AZ-1370J. However this system was not tried.

Working from a stock solution of 50% citric acid by weight, a 10:1:30 solution of citric acid (stock): H₂O₂ : H₂O was prepared just prior to etching. It was impossible to etch anywhere on a
wafer that had been through the ohmic contact formation and anneal. The next section describes what we believe was occurring to prevent the etching and the steps taken to solve the problem.

3.6.3 Gate Recessing—Surface preparation

Initially, an adhesion promoter, a hexamethyldisilazane (HMDS) containing mixture, was employed to assist in resist adhesion for the ohmic contact step, thereby providing better control of the fine line lithography. Although common in silicon processing, its value in GaAs processing is controversial. We nonetheless used the procedure recommended for Si processing: cover the wafer with concentrated HMDS for 10 seconds, then spin off at 5000 RPM. However, this created problems both for etching with citric acid and the quality of ohmic contacts.

It was later found\textsuperscript{109} that HMDS's action is on Si is to make the surface more wettable, yet does not in itself couple with a GaAs surface. The only positive factor in HMDS's use with GaAs is its ability to scavenge any hydroxyls on the surface. However, since the adhesion promoter contains two silazane molecules within its chemical structure, a thin film of SiO\textsubscript{2} is deposited. Upon O\textsubscript{2} plasma treatment, the SiO\textsubscript{2} film becomes glassified, thus forming a layer impervious to the etch solution. Even though a 2–5 second C\textsubscript{2}F\textsubscript{6} or CF\textsubscript{4} plasma treatment should remove this layer, it was decided to omit the HMDS entirely.

The nonuniformity in etching the gate recesses with the thin SiO\textsubscript{2} film on the surface underscored the fact that, for the dimensions that were dealing with, the ultimate in clean surfaces was necessary. Simply degreasing and cleaning in an O\textsubscript{2} plasma was insufficient. Any residual long chain organics left on the surface from the degreasing could become carbonized, producing a barrier to the etch. Residual Al\textsubscript{2}O\textsubscript{3} or AlO\textsubscript{2} sputtered on the surface from the aluminum electrode during the plasma clean would also not be removed.

To be assured of presenting the cleanest surface possible to the citric acid etch, the following cleaning procedure was developed. After the ohmic contacts were alloyed, a complete
degrease was done to remove the majority of any long chain organics. The wafer was then exposed to an O₂ plasma for 60 seconds. Then, making sure that the wafer was dry, the wafer was placed in concentrated HF for 10 seconds, followed by a de-ionized water rinse, blow dry, a concentrated H₂SO₄ dip for 10 seconds, a de-ionized water rinse, and then an ammonium hydroxide:water (1:25) solution dip for 10 more seconds. The wafer was then blown dry under N₂ and PMMA was immediately spun on.

The rationale for each of these steps is as follows. It should be noted that none of these steps should appreciably etch the GaAs, even though a series of very strong acids is used. The reason is that there is minimal oxygen present. To minimize the danger of water oxidizing the surface, the water is allowed to sit for at least 10 minutes before it is used as rinse water. The concentrated HF removes any residual SiO₂, any AlO₂ or Al₂O₃ deposited, as well as any Ga and As oxides. The concentrated H₂SO₄ removes the remaining organics, also removing any oxidized GaAs. Rinsing removes the remaining H₂SO₄ which could cause serious problems with the PMMA. The final NH₄OH dip removes any oxide, but because of the ammonium hydroxide’s volatility, a rinse is not necessary, only a long blow dry with nitrogen. The wafer is not dried in an oven, since it was felt that this would do more harm than good, since the level of contamination inside the oven is difficult to ascertain. This cleaning process enabled us to obtain repeatable, clean etching of the substrate in the region where the gate was to be placed.

Immediately after etching (and de-ionized water rinse) the wafers were placed in a Temescal E-Beam evaporator for gate metal deposition. The metals used were Ti, for better adhesion, Al for conduction, without the problem of Au inter-diffusion into the GaAs, followed by a thin layer of Au (deposited begrudgingly) to allow us to see the devices in the SEM. Ti and Au thicknesses were always about 100 Å, whereas the Al thickness ranged from 300 to 700 Å. Lift-off was then performed in a solution of warm acetone, with some gentle assistance given with the airbrush setup filled with acetone as described previously.
Final completion of the device consisted of using the two-level plasma interlayer resist system as used in the ohmic contact formation to define the interconnect metal level. After exposure and development of the pattern, the wafer was placed in the electron-beam deposition system to deposit in sequence, approximately 250 Å Ti, 500 Å Pt, and 2500 Å of Au. The Ti was used as a highly reactive metal that promotes adhesion, while the Pt was used as a barrier between the GaAs and the upper level gold. The thickness of the pure gold had to be greater than 2000 Å, as otherwise thermal-compression bonding would be difficult.

A sample run sheet for these devices is given in Appendix B, showing all remaining details of the process.
Chapter 4

Tuning the process—MESFET results

Much of what is presented in this chapter is a direct result of the work of my colleague, Dave Allee, who, along with writing the gates for all the devices, in both those described in this and the following chapter, took and analyzed almost all of the MESFET data, and was involved in their processing.

4.1 MESFET Wafer Structure/Fabrication

Initially, to maximize yield by allowing for a wide latitude in processing, the channel layer was chosen to be thicker and have lower doping than would be used for optimized, high performance MESFET's.

The starting substrate was a semi-insulating GaAs wafer. MBE was used to grow a 0.4 \( \mu \text{m} \) thick undoped buffer layer, followed by a 0.18 \( \mu \text{m} \) thick active channel layer doped with Si to 3x10\(^{17}\)/cm\(^3\). A 0.12 \( \mu \text{m} \) cap layer doped with Si to 2x10\(^{18}\)/cm\(^3\) completed the growth. Then, as described in Chapter 3, the device was isolated, ohmic contacts attached to the source and drain, gates defined, recessed, and metallized, and finally interconnect metallization patterned. A schematic diagram of the target structure is shown in Figure 4.1.

Our target etch depth was 2000 Å (1200 Å cap plus 800 Å into the channel). The threshold voltage for low drain-source voltage is given by:

\[
V_t = V_b - \frac{q N_d a^2}{2 \varepsilon},
\]

where \( q \) is the charge on an electron, \( N_d \) is the donor concentration in the channel layer, \( a \) is the thickness of the channel layer, \( \varepsilon \) is the dielectric constant of GaAs, and \( V_b \) is the Schottky barrier
Fig. 4.1. Target MESFET structure for first test run.

height. Assuming a barrier height \( V_b \) of 0.6 volts, an etch depth of 2000 Å yields a threshold voltage of \(-1.4\) volts, while etch depths of 1600 Å and 2400 Å give threshold voltages of \(-3.3\) and \(-0.12\) volts respectively. This allows plenty of freedom to miss the target etch depth and still have a depletion mode device. If the gate recess is over-etched, an enhancement mode transistor will result. Under these circumstances, an unduly high source resistance will result from lateral etching between the gate metal and the cap layer.

We preferred to etch the recess in a single unmonitored step to maximize uniformity from device to device. Thus the etch rate of the citric acid etch (about 450 Å/minute) was carefully calibrated using a dummy wafer. A correction was needed to account for the 50 to 100 Å of material removed in the cleaning process. Etch rate monitoring was not necessary, even though the actual etch rate might be significantly different from the calibrated rate, given the range of acceptable average etch depths.

Eighteen functional MESFET's were produced and examined in a high resolution (Hitachi S-800) Scanning Electron Microscope (SEM) to measure the physical gate length and observe the physical characteristics of each device. These observations revealed gate lengths ranging from 900 Å to 0.64 \( \mu \)m. DC characteristics of each device were then obtained.
4.2 Gate Formation Results

Figure 4.2 is a low magnification view of a 900 Å gate length MESFET. The gate recess is visible between the source and drain metallization. The interconnect metallization overlaps the ohmic and gate metallization and extends to the bonding pads. Figure 4.3 shows a higher magnification view of the gate region of the same device. Here the gate is visible in the center of the recess, running up the side of the mesa into the active region, and back down on the opposite side.

Figure 4.4 shows a extremely high magnification view. Note the flatness of the etched region. As described more fully in Chapter 3, the orientation of the wafer in conjunction with the preferential nature of the citric acid etch encourages a flatter bottom.

The SEM examination revealed a gate recess width substantially larger in the source-drain direction than the gate metallization itself (Fig. 4.4). It is speculated that when etching the recess through the PMMA opening, significant lateral etching occurred causing an undercut. Yet the PMMA remained mostly intact, allowing for the definition of the much narrower electrode, staying remarkably well attached to the GaAs surface. Comparison between the expected line width written in the PMMA and the actual gate length, however, did show that the PMMA sagged as a result of the undercut, resulting in a larger resist opening. The minimum recessed gate length for these MESFET's was 900 Å, while metal features as small as 200 Å were obtained in earlier test structures with this PMMA lift-off technology without any recessing\textsuperscript{98}. Both the MODFET's described in the next chapter and an optimized MESFET run which was fabricated later did not have such a thick cap and active layer to etch through, and thus, as expected, a significantly shorter gate length was obtained.
Fig. 4.2. Low magnification view of a 900 Å gate length MESFET. Recess trench is visible as a vertical line in the center of the picture between the two gate connections. Gate itself is not visible.
Fig. 4.3. Medium magnification view of a 900 Å gate length MESFET. The gate line can be observed running up the side of the mesa and back down the other side.
Fig. 4.4. High magnification view of a 900 Å gate length test device. Note the uniformity of the recessed area where the gate is placed.
Since we had a connection to both ends of the gate, in theory it was possible to obtain a
good indication of the quality of the metal film by comparing measurements of end to end gate
resistance as a function of the gate length to that expected for bulk metal. However, the thin
metallization sequence of Ti/Al/Au (150 Å/ 500 Å/ 200 Å) made making a measurement
difficult. The small a cross sectional area made the gates act as extremely low current fuses, especially in
the even thinner region where the gate crosses over the mesa step. After destroying a few
devices by forcing too much current through the gate with a curve tracer (or HP4145A
Semiconductor Parameter Analyzer), the plot shown in Figure 4.5 was obtained.

For a large metal line, one expects the resistance of the line to be given by:

\[ R_g = \frac{W_{tot}}{L_g \cdot t_g} \rho, \]

where \( L_g \) is the gate length, \( \rho \) is the resistivity of the metal line, \( t_g \) is the gate thickness, \( W_{tot} \) is
the total gate width including the connecting metal between the thick interconnect metal and the
active device. Interpolating from the values tabulated from Kaye et al.\textsuperscript{110}, the resistivity of each
component metal used in the gate is obtained at room temperature: Ti (44.4x10\textsuperscript{-6} Ω cm), Al
(2.75x10\textsuperscript{-6} Ω cm), and Au (2.28x10\textsuperscript{-6} Ω cm). We might therefore expect an overall resistivity of

\[ \rho = \left( t_{Au} + t_{Al} + t_{Ti} \right) \left( \frac{t_{Au}}{\rho_{Au}} + \frac{t_{Al}}{\rho_{Al}} + \frac{t_{Ti}}{\rho_{Ti}} \right)^{-1} = 3.1 \times 10^{-6} Ω cm. \]

As expected, the data showed a resistance which was inversely proportional to gate length for
sufficiently long gates. However, from the slope of the larger gate length portion of Figure 4.5 (50
Ω μm) we obtain an equivalent bulk resistivity of 13.5 x 10\textsuperscript{-6} Ω cm. Thus, even for the longer gate
lengths, we observe significant effects of grain boundaries on the resistivity. Additionally, for
devices with gate lengths less than 0.12 μm, a far more pronounced effect was observed. We
speculate that this sharp upturn in the curve is due to formation of much smaller grains and
possibly uneven metal deposition, which becomes very significant at these dimensions.
Fig. 4.5. Plot of gate resistance vs. the inverse gate length. Length of line measured is approximately 30 µm.

It should be noted that a low gate resistance is necessary for obtaining a high $f_{\text{max}}$ and low noise figure. The gate resistance measured here was much too large to expect good high frequency characteristics from the device.

The Schottky gate characteristics were, however, quite good. The gate leakage for most devices was 15 nA for one volt of reverse bias. The barrier heights were determined to be between 0.55 and 0.65 eV, with an ideality factor of between 1.2 and 1.7.

### 4.3 Device Results

A typical I-V curve for a 900 Å MESFET is shown in Figure 4.6. One of the first things apparent in this figure is the unusually low dc output conductance in the saturated region of the device. The measured output conductance value of 8 mS/mm was quite typical of all of these MESFET devices, which is better than most values in the literature. However, given that the gate is virtually self aligned to the recess in the very thick cap layer, and considering the strong depletion character of the devices, one could see how such a value might be expected.
Fig. 4.6. Current vs. voltage characteristics of a 900 Å gate length MESFET. Gate voltage ranges from –5 volts to 0 volts in 1 volt increments.

The thick cap layer employed in these devices also had another advantage: a very low source resistance ($R_s$), both from decreased ohmic contact resistance, and from better conduction in the layer leading to the gate. As described in Chapter 2, a high source resistance has the effect of significantly reducing the extrinsic transconductance with respect to that available intrinsically, thus reducing the high frequency performance of the device. At the expense of a number of devices, the resistance was measured by monitoring the drain source voltage, while forward biasing the gate with respect to the source, and approximating the source resistance as that voltage divided by the current. As expected, the measured values of the source resistance were extremely low, ranging between 0.3 and 0.5 Ω-mm.
The contributions of ohmic contact resistance and sheet resistance components were then determined using a four-point probe approach. The various structures that are most commonly used in this category are discussed in detail by Loh et al. The cross bridge Kelvin resistor and a version of the transmission line tap resistor were included in the mask set. The ohmic contact resistance and sheet resistivity were 0.09 Ω-mm and 120 Ω/square, respectively.

Since each of our gates were individually written by e-beam, the heavily doped cap layer was still present on all of these structures. Thus, the use of the structures for determining sheet and contact resistivities was limited to the MESFET’s only, since in the MODFET the cap layer is uncoupled from the active layer, and the value of ρc to the cap layer is not necessarily identical to ρc to the two-dimensional electron gas layer. In the MODFET case, measurements using these structures were only useful in determining an upper bound on the ohmic contact resistance.

Figure 4.7 shows the peak measured extrinsic transconductance values as a function of gate length. Due to the low source resistance and output conductance, the correction from the extrinsic to the intrinsic values was roughly constant at 10 to 15%. These values ranged from 220 to 250 mS/mm, and at first glance appeared roughly independent of gate length as would be expected assuming an equilibrium saturation velocity in the channel without velocity overshoot or ballistic electron effects. In this case the transconductance would be given by:

\[
\mathcal{g}_m = \frac{v_s \varepsilon W_g}{h},
\]

where \(\varepsilon\) is the dielectric constant, \(W_g\) is the gate width, \(h\) is the width of the depletion region under the gate, and \(v_s\) is the electron saturation velocity. The measured data, when substituted into the above equation, with \(h\) set equal to the total channel thickness, indicates a saturation velocity of approximately 1.2x10^7 cm/sec, in agreement with the previously reported values.
Fig. 4.7. Transconductance as a function of gate length for the first MESFET's.

Values of drain-source saturation current ($I_{dss}$) at zero volts gate to source voltage as a function of gate length are shown in Figure 4.8. $I_{dss}$ increases from 4.5 mA for a device with a gate length of 0.64 $\mu$m to 7.5 mA for a gate length of 900 $\AA$. Assuming the velocity saturation model holds as indicated above, then $I_{dss}$ is given by:

$$I_{dss} = q N_d v_s W_g (a - h),$$

where $a$ is the channel thickness, $h$ is the width of the depletion region under the gate, $N_d$ is the doping concentration in the active layer, $q$ is the electronic charge, $v_s$ is the electron saturation velocity, and $W_g$ is the device width. Using this equation, we estimated the etch depth for each device. With the saturation velocity of $1.2 \times 10^7$ cm/sec found previously, we obtained the results shown in Figure 4.9. The estimated etch depth varied over a range of almost 500 $\AA$ (25% of the total etch depth), and decreased as the gate length decreased.
Fig. 4.8. Saturation current as a function of gate length. Note the rise in saturation current as the gate length is reduced, indicating nonuniform recess etching.

Fig. 4.9. Channel thickness as calculated from the measured saturation current.

This observation is consistent with measurements of the threshold voltage of each device. (See Section 5.4 for a complete description of the measurement method.) Using the equation for the threshold voltage for a low source-drain voltage given earlier in Section 4.1, an effective etch depth can be calculated. As shown in Figure 4.10, this depth indicates that there is substantial variation in the etch depth as the smaller gate lengths are approached. This effect can
be explained if the citric acid etch rate is being rate limited by the transport of the reactants in and out of the narrow gate opening. Shorter gate lengths would result in a shallower etch and thus a thicker active channel. For the MODFET structure, an etch depth variation of this magnitude would be unacceptable, given the higher doping level in the channel.

![Graph showing threshold voltage vs. gate length](Image)

**Fig. 4.10.** A plot of the threshold voltage vs. gate length also indicating a change in etch depth as a function of gate length.

It should also be noted that the lateral etch distance obtained from the SEM pictures could be correlated quite well with the etch depth obtained from the saturated current (Fig. 4.11). Given that the lateral etch distance should be approximately equal to the etch depth from the crystal orientation previously mentioned, this acts as a check on the use of the saturated current as an effective method of obtaining the actual etch depth. The y intercept is close to the origin providing the reassuring result that zero undercut corresponds to zero etch depth. Using the measured etch undercut and the linear correlation determined above, $I_{dss}$ could be predicted to within ±10% for any device. Not only could the general trend of increasing $I_{dss}$ with decreasing gate length be reproduced, but the scatter in the $I_{dss}$ values for a given gate length was
predictable. This indicated that in our MESFET's, for gate lengths down to 900 Å, no significant deviation from the simple velocity saturation model was seen, and thus no case for velocity overshoot effects could be made.

$$y = -231.1589 + 1.2122x \quad R = 0.95$$

![Graph showing etch depth vs. lateral etch width.](image)

Fig. 4.11. Etch depth vs. lateral etch width.
Chapter 5

MODFET Results—GaAs and InGaAs Channel MODFET's

As described in Chapters 3 and 4, a process for fabricating short gate length devices had been developed and tested by successfully fabricating MESFET's. The first portion of this chapter describes the fabrication, dc characterization, and analysis of short gate length AlGaAs/GaAs MODFET's, were the electrons are singly confined within the quantum well at the AlGaAs/GaAs interface. The second portion of this chapter describes the fabrication, dc characterization, and analysis of MODFET's utilizing a thin undoped InGaAs layer in between the AlGaAs/GaAs interface. It was expected that the reduced scattering and double confinement found in the InGaAs MODFET's would afford better device characteristics.

5.1 GaAs Channel MODFET—Layer Structure

A semi-insulating (100) GaAs wafer with a suitable MODFET layer structure grown upon it by MBE was obtained from Y.-C. Pao at Varian. The layer structure, not unlike that of a standard MODFET structure, consisted of a superlattice buffer layer (4 layers each of 100 Å undoped Al$_{0.3}$Ga$_{0.7}$As interspersed with 100 Å of GaAs), followed by a 4000 Å undoped GaAs buffer layer, a 300 Å Al$_{0.26}$Ga$_{0.74}$As layer doped at 2x10$^{18}$/cm$^3$ with Si, a graded Al composition layer of 150 Å doped at 4x10$^{18}$/cm$^3$ followed by a 600 Å cap layer doped at 4x10$^{18}$/cm$^3$ with Si. GaAs layers were grown at 0.85 μm/hour, while the AlGaAs layers were grown at a rate of 1.13 μm/hour. A schematic cross sectional view and an energy band diagram of the device are shown in Figure 5.1.

After growth the wafer followed, with only minor changes, the same processing sequence as previously described in Chapter 3. Ohmic contacts were annealed at 450°C for 30 seconds in a furnace annealer instead of a rapid thermal annealer. Following Y.-C. Pao's experience$^{113}$, we
Fig. 5.1. (a) Layer structure and (b) energy band diagram for GaAs channel MODFET structure.
employed a furnace anneal to obtain a more consistent, lower resistance ohmic contact, a more critical parameter for peak MODFET performance.

More importantly, in the case of MODFET's, the gate recess was monitored by measuring the source-drain saturation current as a function of etch depth for a range of device sizes. This entailed etching in several stages, despite worries about the introduction of contamination. In each case, initially a slow decrease of source-drain current at a constant voltage \( V_{ds} \) was expected, along with a corresponding decrease in the linear to saturated transition point in the I-V curve, followed by a sharp decrease in the current.

To determine the end point for the etch, the expected saturation current was calculated. Assuming a sheet carrier concentration of \( 1.4 \times 10^{12}/\text{cm}^2 \) (as previously measured on a similar wafer using Hall-effect measurements, and in agreement with the simulation presented later in Figure 5.8) and a saturation velocity of \( 1.2 \times 10^7 \text{ cm/sec} \) (as confirmed in Section 4.3), the saturation current \( (I_{dss}) \) is given by:

\[
I_{dss} = q n_s v_s = 2.7 \text{ mA}.
\]

Table 5.1 summarizes the measured saturation currents as a function of total etch time.

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<th>Run R32 GaAs Channel Devices:</th>
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<td><strong>Device Label</strong></td>
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<tr>
<td>-------------------</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>D1A5</td>
</tr>
<tr>
<td>D2A5</td>
</tr>
<tr>
<td>D2A4</td>
</tr>
<tr>
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</tr>
<tr>
<td>D2B2</td>
</tr>
<tr>
<td>D2B4</td>
</tr>
</tbody>
</table>

Table 5.1. Saturation current (4 volts source to drain) as a function of gate recess etch time. Data is from GaAs MODFET run.
After gate metallization and lift-off, interconnect metallization (with 2500 Å of gold) completed the fabrication process. All MODFET's were then characterized (dc) at room temperature. A representative example of an I-V curve is shown in Figure 5.2.

![Graph of I-V curve](image)

**Fig. 5.2.** Typical I-V curve for the GaAs channel MODFET device. This particular device has a gate length of 800 Å. Gate voltage ranges from −1 to 0.4 volts in 0.2 volt increments.

### 5.2 Gate Resistance Measurement

Gate resistance was measured on each device, not only identify bad devices with open gates, but also to determine general gate metal quality. The MODFET's were even easier to destroy than were the MESFET's, given the thinner gate metallization employed. Thus, rather than use a curve tracer (or HP4145A Semiconductor Parameter Analyzer), a 1, 10, or 100 nA current source was used to drive current along the gate electrode, while separate probes were used to monitor the voltage drop across the gate; even so, precautions against voltage spikes and static charge proved necessary.
As with the MESFET gates, the quality of the metal in the gate lines could be determined from a plot of the gate resistance as a function of the inverse gate length (Fig. 5.3). Since the aluminum thickness had been reduced to 300 Å (and the Ti and Au thickness reduced to 100 Å each), it was far more difficult to put down an even metal layer, and grain effects would be expected to become more pronounced. The thickness of the metallization over the 45° mesa step was, at best, 300 Å. Coverage over both mesa steps without any high resistance regions would not be expected for the shorter gates. Thus the increased resistance of shorter gates was even more pronounced, as shown in Figure 5.3.

![Gate Resistance vs. 1/Gate Length](image)

**Fig. 5.3.** Gate resistance as a function of inverse gate length for thinner gate MODFET structure. For the bulk case, a linear relationship should ensue.

### 5.3 Calculation of Peak Intrinsic Transconductance Values

As with the MESFET’s, the first task was to extract intrinsic transconductances from the measured (extrinsic) values. This distinction is important because the MODFET’s, as opposed to the MESFET’s, had high enough source resistances to make the difference significant. However, finding the best way of accurately determining the source resistance was more difficult. Forward
biasing the gate with respect to the source and measuring the voltage at the drain, as was done with the MESFET's, was not acceptable. First of all, too many MESFET's had been destroyed using this method, and it was unclear just how much damage to the devices had been done in the process. Secondly, more voltage would have to be applied to get current to flow through the roughly 300 Å thick insulating AlGaAs layer.

Measuring adjacent devices without gates was helpful in determining a lower bound on the source resistance (one half the source-drain resistance); however that was the extent of its usefulness, due to the presence of the upper, highly conductive GaAs cap layer acting as a shunt resistance in parallel. There were also problems with uniformity of the structures and contacts if the measured points were too far from the actual devices. Table 5.2 summarizes these values.

<table>
<thead>
<tr>
<th>Run</th>
<th>Type (Letter)</th>
<th>Source-Drain Nominal Spacing (µm)</th>
<th>Average Resistance $R_{sd}/2$ (Ω)</th>
<th>Number in Average</th>
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</thead>
<tbody>
<tr>
<td>R32</td>
<td>A</td>
<td>10</td>
<td>65</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>5</td>
<td>37</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>3</td>
<td>25</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>D</td>
<td>2</td>
<td>19</td>
<td>4</td>
</tr>
</tbody>
</table>

Table 5.2. Adjacent devices source-drain resistance divided by two. Since these resistances include the highly doped GaAs cap layer, they only give a lower bound on the source resistance.

The only method that was left open for measuring the source resistance with any degree of accuracy was the following. Low field I-V measurements were taken in the range of 0 to 0.01 volts source-drain bias within a range of gate biases. The source resistance was estimated from these measurements as half the maximum slope asymptotically approached for small forward bias voltages. These resistances ranged from 50 Ω to 140 Ω depending on the source-drain spacing of the device. Figure 5.4 shows a typical measurement.
Fig. 5.4. Low field (0.01 $V_{ds}$) I-V curve of a GaAs MODFET. The source resistance can be estimated from the slope of the curves as asymptotically approached with increasing gate voltage. Gate voltage ranges from -1.3 volts to 0.3 volts.

Intrinsic transconductances were then measured for all devices in source-drain voltage increments of a quarter of a volt over the full range of meaningful gate voltages. The peak value was recorded as well as the corresponding values of $V_{ds}$ and $V_g$. This peak room temperature extrinsic transconductance was measured to be as high as 415 mS/mm for the conventional MODFET device.

Ordinarily one would be tempted to simply calculate the intrinsic values of $g_m$ from the following equation, as was done with the MESFET case,

$$g_{mi} = \frac{g_{mx}}{1 - \frac{g_{mx}}{g_{mn}}}.$$  

This assumes, however, that the output conductance of each device is nearly zero. For the MESFET case, the output conductance was unusually small and thus it could be ignored. However, this was not the case for the MODFET's as was seen previously from the sample I-V
curve shown in Figure 5.2. Therefore, the output conductances were also measured in the region of peak transconductance from the I-V curves of the devices. From these measurements the intrinsic transconductance was found using the following, more complete equation\textsuperscript{114}.

\[ g_{mi} = \frac{g_{mi}^0}{1 - (R_s + R_d)g_{out}} \left( 1 + R_s g_{mi}^0 \right), \quad \text{where} \quad g_{mi}^0 = \frac{g_{mx}}{1 - R_s g_{mx}}, \]

and where \( g_{mi}^0 \) is the intrinsic transconductance, uncorrected for output conductance, \( g_{mx} \) is the extrinsic transconductance, \( g_{out} \) is the output conductance, \( R_s \) is the source resistance, and \( R_d \) is the drain resistance. Figure 5.5 shows the intrinsic transconductance as a function of gate length for these devices, fully corrected by using the previous equation.

![Intrinsic Transconductance vs Gate Length](image)

Fig. 5.5. Intrinsic transconductance as a function of gate length, fully corrected.

### 5.4 Etch Depth Variance Correction

As described in Section 2.1, the peak intrinsic transconductance is directly proportional to the gate capacitance and inversely proportional to the gate transit time thus:
\[ \varepsilon m, \text{maximum} = \frac{C_g}{\tau}. \]

It was the purpose of this work to investigate the properties of the two-dimensional electron gas underneath the gate. The primary interest was therefore in \( \tau_d \), the gate transit time. However, the capacitance varies as a function of the distance between the gate and the electron channel and thus also the recess etch depth. If one assumes the same etch variation in the MODFET as observed in the MESFET, this correction could indeed be a major one and could perhaps make any meaningful interpretation impossible. At best, the etching of a gate recess within lines as small as 300 Å necessarily implies some sort of etch depth variation from device to device. It was thus absolutely critical to measure this variation and correct for it as accurately as possible.

Accurate measurement of etch depth could not be made with SEM pictures due to the lack of good depth resolution. Cleaving each piece would have been destructive. Thus the best method available to us was to estimate the etch depth from the electrical measurements as follows.

The source-drain current \( (I_{ds}) \) was measured in the linear, very low field region of each device, with the source-drain voltage \( (V_{ds}) \) held constant at 10, 30, and 50 mV. Assuming that all the current was carried in the two-dimensional electron gas layer, and short channel effects can be neglected, \( I_{ds} \) is given by

\[
I_{ds} = \mu \frac{W_g}{L_g} C \left( V_g - V_t - \frac{V_{ds}}{2} \right) V_{ds},
\]

where \( \mu \) is the mobility of the conducting layer, \( C \) is the capacitance of the gate, \( V_g \) is the gate voltage, \( V_t \) is the threshold voltage, \( V_{ds} \) is the drain-source voltage, \( L_g \) is the gate length, and \( W_g \) is the width of the gate. When \( V_{ds} \) is sufficiently small, i.e. when \( V_{ds} \ll V_g - V_t \), short channel effects are minimized and the above equation can be reduced to the following:

\[
I_{ds} = \mu \frac{W_g}{L_g} C (V_g - V_t) V_{ds}.
\]
From this it is clear that the threshold voltage can be determined by the intercept of each linear region with the $I_{ds} = 0$ line. A typical example of this is shown in Figure 5.6.

![Graph showing $I_{ds}$ vs. $V_{gs}$ at fixed $V_{ds}$ for determination of threshold voltage. Source-drain voltage was 0.01, 0.03, and 0.05 volts. The linear region of the curves intersect the x axis at the same point, so short channel effects can be ignored.](image)

Fig. 5.6. $I_{ds}$ vs. $V_{gs}$ at fixed $V_{ds}$ for determination of threshold voltage. Source-drain voltage was 0.01, 0.03, and 0.05 volts. The linear region of the curves intersect the x axis at the same point, so short channel effects can be ignored.

Note that for this device, as for all others, all linearly extrapolated $V_{th}$ values for each $V_{ds}$ agreed, assuring it was in a low enough field region that short channel effects on the threshold voltage could be ignored.

Each of the threshold voltages measured for these GaAs channel devices were plotted as a function of gate length. In the MESFET case, there was a strong downturn in the threshold voltage as the gate length approached 0.1 μm (Fig. 4.6). Figure 5.7 shows the threshold voltage as a function of gate length grouped according to the source-drain spacings. Within each group, most of the devices fell within a very narrow range of threshold voltages. As opposed to the MESFET's, the etch rate did not seem to fall off as the gate length was reduced. For the
MODFET, the threshold voltage seemed, if anything, to increase slightly with reduced gate length for the smaller gate lengths.

This rise in the threshold voltage as the gate length was reduced was quite puzzling initially. The same effect was observed with the InGaAs devices (discussed later). Upon closer examination, it became clear that for the MODFET's, the proximity of the ohmic contacts to the gate region was more important than the gate length itself. Similar effects with peroxide based etches have been seen by others, where it is presumed that electrolysis effects act to change the etching rate\textsuperscript{115}. Indeed, the difference in etch rate (especially for AlGaAs), when a stainless steel or a Teflon holder is used, can be quite large\textsuperscript{101}. Thus such an observation was understandable. Etch depth variation in the MODFET structures would be reduced due to the two competing effects!

![Graph showing threshold voltage vs. gate length for different runs.](image)

**Fig. 5.7.** Threshold voltage vs. gate length for different runs.

The next step was to convert the observed threshold voltage into a recess depth, using a combination of a simple MODFET model and numerical (3-D Poisson Solver, assuming a Fermi-Dirac distribution) device simulations. We refer to the conduction band diagram of the GaAs
channel MODFET as shown in Figure 5.1. $\Delta E_c$ is calculated from the empirical equation for the band gap, assuming a 63-37% conduction-valence band split$^{116,117}$:

$$E\gamma_{s}(x) = 1.424 + 1.247x = 1.424 + .324\text{ with } (x = 0.26),$$

therefore,

$$\Delta E_c = 63\% (0.324) = 0.204 \text{ eV.}$$

The Schottky barrier height ($V_b$) was taken to be 0.8 volts for the metal to AlGaAs interface. Using the depletion approximation for the band structure we have, at pinch off,

$$V_p + V_b - \Delta E_c = \frac{qN_d d^2}{2 \varepsilon},$$

where

$$\varepsilon(Al_{0.26}Ga_{0.74}As) = 12.37 \varepsilon_0,$$

and $\Delta E_c$ is the conduction band discontinuity at the GaAs-AlGaAs interface, $N_d$ is the doping in the AlGaAs region, $d$ is the gate metal to channel interface distance (after etching), $q$ is the charge on an electron, $V_b$ is the Schottky barrier voltage, $V_p$ is the pinch-off voltage. From this equation, knowing the original channel depth prior to the gate recess etch, one obtains a direct relation between the etch depth and the measured pinch-off voltage.

Application of the above equations is straightforward for recess depths greater than 750 Å. This was the case in all but a few devices. However, a minor complication is present for the remaining few, caused by the graded composition in the upper portion of the AlGaAs layer. Upon closer examination, one realizes that the extra doping in the layer tends to cancel the effect of the Al composition grading. Near pinch-off, the conduction band diagram for the graded layer looks similar to a constant composition, ungraded layer. Even so, a number of calculations and device simulations were made to ensure a proper recess variation correction. Given the narrow range of

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threshold voltages measured (and accepted as detailed below), a simple linear approximation, calculated from both the simulations and the depletion approximation, was of sufficient accuracy.

It should be noted that devices with $V_{th}$ much less than $-1$ volt were ignored in the analysis. This was done for two reasons. The above correction was only first order, so the larger the spread of data, the less accurate the correction. Also, as the threshold voltage becomes more negative, there is a greater chance of parallel conduction in the parasitic MESFET$^{118}$ in the AlGaAs layer (Section 2.3). Figure 5.8 shows a simulation of the GaAs MODFET's fabricated, showing the onset of parallel conduction as the concentration of the carriers in both MODFET and parasitic MESFET layers as a function of gate voltage. If the threshold voltage becomes too negative, one even sees two peaks in the transconductance curve, as we saw in one of our under-etched devices (Fig. 2.8).

Fig. 5.8. Simulation of MODFET structure showing carrier concentrations in both the two-dimensional electron gas (solid line) and the onset of parallel conduction (dotted line). Simulation is for GaAs MODFET with 300 Å AlGaAs between the gate and the channel.
Another group of devices was also eliminated from consideration where the peak $g_m$ was found to be at a gate voltage larger than a few tenths of a volt, or those with $V_{th}$ greater than zero volts. This was due to the large source resistance that led to large uncertainties in the measured transconductance, as well as the difficulty of making sure that one had a true peak, since measurement could not be attempted for gate voltages exceeding 0.3 volts without risking destroying the device. None of our devices had self-aligned implants. Thus, if a device was heavily over-etched and the device characteristics approached that of an enhancement mode device, the region between the gate and the source or drain $n^+$ cap became a very high resistance region.

For the remaining devices, the actual etch depth was determined. Etch depth variation from device to device was found to be within roughly a 100 Å range for adjacent devices with similar source-drain spacings. The measured etch depth was then used to calculate a correction for the peak transconductance. This value we will call the “effective” saturation velocity as is described in the following.

5.5 Effective Saturation Velocity Comparison

Assuming velocity saturation holds in the channel underneath the gate, to first order for small MODFET’s (a reasonable assumption, given that source-drain voltages at the peak transconductances are over one volt), the peak intrinsic transconductance is given by$^{119-121}$

$$g_{m,peak} = \frac{C_s}{\tau} = \frac{\varepsilon W_g V_s}{d + \Delta d},$$

where $C_s$ is the gate capacitance (derivative of the electron sheet density with respect to the gate voltage), $\tau_d$ is the transit time under the gate, $\varepsilon$ is the dielectric constant, $d$ is the distance between the gate and the channel, $V_s$ is the saturation velocity, $W_g$ is the gate width, and $\Delta d$ is the
distance between the peak or average of the electron wave function and the physical interface which is approximately 80 Å. Using the etch depth found in the previous section, an effective saturation velocity was calculated for each device from the peak intrinsic transconductance. This saturation velocity was a better figure for comparison from device to device than the peak transconductance due to the inclusion of etch depth variances. Figure 5.9 shows this effective saturation velocity as a function of gate length for the GaAs channel MODFET's.

![Diagram showing saturation velocity vs. gate length](image)

**Fig. 5.9.** Effective saturation velocity as a function of gate length for GaAs channel MODFET's. The dotted line indicates the effect of correcting for the gate to drain distance (200 Å).

One necessary additional correction, if one is to equate the above data with the true saturation velocity, is to include the estimated additional length beyond the physical gate electrode that the electrons have to traverse in the saturated regime. The carrier transit time should now be modified to include this longer effective gate length:

\[ \tau = \frac{L_g^*}{v_s} = \frac{L_g + L_{gd}}{v_s}, \]
where $L_{gd}$ is the distance between the $n^+$ cap layer on the drain side and the gate$^{122,123}$. Since $L_{gd}$ is, in actuality, the length of the region where electrons traverse with saturated (or ballistic) velocities beyond the gate edge, the exact length is unclear, without extensive Monte Carlo simulations. This length, however, can be considered a constant for different gate lengths and similar geometries. The effect of this correction is to raise the saturation velocity an increasing amount as the gate length is reduced. The dotted line in Figure 5.9 is an approximation of this correction for $L_{gd}$ equal to 200 Å. It therefore should be noted that a downturn in the saturation velocity is not necessarily observed. However, the peak in the maximum transconductance as the gate length is reduced beyond a value near 0.15 μm is still valid, even when corrected for etch depth variations.

It should also be noted that much of the random scatter in the saturation velocity curve in Figure 5.9 for the short gate lengths appeared to come about when the correction for non-zero output conductance was made. Yet the correction, while technically necessary, did not change the final result. For comparison, a plot of the effective saturation velocity assuming the output conductance was fixed at zero mS is shown in Figure 5.10.

The presence of a peak in this effective saturation velocity (to be looked upon as a corrected form of the intrinsic transconductance) can be explained by looking carefully at the work of Kizilyalli et al.$^{124}$ In his work, he simulated a similar GaAs MODFET structure using the three moment Boltzman Transport Equation. The main difference between our structures and his was that he set the distance between the source and drain to be equal to three times the gate length, while our structures had fixed source to drain spacings.

Kizilyalli et al. considered the source-drain current as a function of gate length for a constant source-drain voltage of 0.9 volts. He considered two specific regimes of transistor operation by fixing the gate-source voltage at two values. At a gate-source voltage of 0.39 V, the device was fully on. Associated with this gate source voltage was the source-drain current, $I_{HS}$. At
a gate-source voltage of −0.21, the device was near pinch off. Associated with this gate-source voltage was the source-drain current, $I_L$.

If no velocity saturation, overshoot, or ballistic effects are observed, then as described in Section 2.1, the velocity is simply proportional to mobility: $I_H \propto L_g^{-1}$ and $I_L \propto L_g^{-1} (\beta=1)$. However, if velocity overshoot (ballistic) effects dominate current transport, the proportionality factor ($\beta$) will become larger than 1, as the electrons continue to go ever faster with shorter gate lengths. On the other hand, if electron transport is dominated by velocity saturation, the current will no longer rise with the higher fields experienced with shorter gate lengths, due to the mobility reduction that the electrons have experienced by scattering into the L band.

When the device is operating in a region where the channel is nearly depleted at the drain end ($I_L$), most of the accelerating field is located in a very narrow region. During a large fraction of the electron's travel, it is strictly in a drift region. Thus, velocity overshoot effects dominate the description of the electron's motion. In the full on state ($I_H$), however, the electron has plenty of
space to slowly accelerate to the saturated velocity and stay at that velocity. Thus as the fields increase due to the reduction in the gate length, the current flowing from source to drain should not increase nearly as much. Indeed, for the specific geometry Kizilyalli et al. simulates, he finds $\beta$ to be 0.7 for $I_H$ and 1.2 for $I_L$:

$$I_H \propto L_g^{-0.7} \quad \text{and} \quad I_L \propto L_g^{-1.2}$$

From the above equations it becomes clear that there will be a point where the source-drain current will increase faster with decreasing gate length near pinch-off than it will when the device is fully on, or:

$$\frac{\partial I_H}{\partial L_g} \leq \frac{\partial I_L}{\partial L_g}$$

When this begins to occur, the I-V curve is being squeezed from the bottom, and a further rise in the transconductance is not expected. He estimated this critical gate length by assuming the currents keep their basic functional dependence ($\beta=0.7$ and 1.2) as the gate length is reduced and extrapolating back to the point where the above condition holds. For his GaAs channel MODFET, he estimated this point to be about 0.15 $\mu$m. Looking at Figure 5.9, this value is remarkably close to the value observed.

5.6 InGaAs MODFET’s—Superior Electron Transport

InGaAs channel MODFET's have a number of advantages over their GaAs channel counterparts. In addition to the better electron confinement and better shielding due to higher electron concentrations in the well, InGaAs has a higher low field mobility, and a larger $\Gamma$ to $L$ valley separation (ranging from 1.16 eV for InAs to 0.31 eV for GaAs) as is illustrated in Figure 5.11$^{125}$. An additional advantage is the possibility of better electron confinement from the backside at the GaAs-InGaAs interface.
Fig. 5.11. Nonlocal pseudopotential calculation of band structure for (a) GaAs and (b) InAs. The relevant energy eigenvalue transition is from $\Gamma_6$ to $L_6$. Reprinted courtesy of J. Chelikowsky. 

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This improved confinement should reduce short channel effects and one would thus expect that the peak $g_m$ would occur at a smaller gate length than observed for the GaAs MODFET, given a similar structure. Thus it was decided to try to fabricate small gate length MODFET's in the InGaAs channel system.

5.7 InGaAs MODFET's—Structure and Results

An InGaAs structure, very similar to the earlier GaAs MODFET wafer, was grown by Y.-C. Pao at Varian. The structure was grown on a semi-insulating GaAs substrate. It consisted of the same superlattice buffer layer, followed by a 2200 Å undoped GaAs buffer layer, a 120 Å In$_{15}$Ga$_{85}$As undoped channel layer, a 20 Å undoped Al$_{21}$Ga$_{79}$As spacer layer, a 500 Å Al$_{21}$Ga$_{79}$As layer doped to 2x10$^{18}$/cm$^3$ with Si, and a 600 Å GaAs cap layer, Si doped to 4x10$^{18}$/cm$^3$. A schematic diagram of the structure showing a side view of the completed MODFET and an energy band diagram for the device area are shown in Figure 5.12.

Two separate e-beam writing runs (R33 and R36) on two different quarters of the InGaAs MODFET wafer were completed due to a lack of sufficient data in the small gate length region of the first run. Source drain currents were again monitored in both cases in an effort to stop the etching at the proper time. As the sheet carrier concentration was higher in the InGaAs channel device ($n_s=2.4 \times 10^{12}$/cm$^2$), the target saturation current was therefore calculated to be much higher ($I_{dss, calculated} = 4.6$ mA) than for the GaAs channel MODFET. Table 5.3 shows the source-drain current as a function of etching time.
Fig. 5.12. (a) Layer structure and (b) band diagram for InGaAs channel MODFET.
Run R33—First Run InGaAs Devices:

<table>
<thead>
<tr>
<th>Device Label</th>
<th>Gate Length (µm)</th>
<th>Etch Time (Seconds)/Source-Drain Current (mA)</th>
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</thead>
<tbody>
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<td>30</td>
</tr>
<tr>
<td>D1A1</td>
<td>2.32</td>
<td>5.9</td>
</tr>
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<td>D1A2</td>
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<td>0.2</td>
<td>6.95</td>
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<tr>
<td>D1B3</td>
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<td></td>
</tr>
<tr>
<td>D2A1</td>
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</tr>
<tr>
<td>D2B3</td>
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<td>8.7</td>
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</table>

Run R36—Second Run InGaAs Devices:

<table>
<thead>
<tr>
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<th>Etch Time (Seconds)/Source-Drain Current (mA)</th>
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<tr>
<td>D2C5</td>
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</tr>
</tbody>
</table>

Table 5.3. Saturation current (measured at 2 volts source-drain) as a function of etching time.

After gate and interconnect metallization, complete characterization was performed on the InGaAs channel MODFET in the same manner as the GaAs MODFET. Room temperature extrinsic transconductances reached 340 mS/mm for the pseudomorphic MODFET's. Measurement of the source resistance and the output conductance in the same manner as before yielded extrinsic transconductances of up to 450 mS/mm.

For calculating the effective channel depth, device simulations were not available (as they were for the GaAs channel MODFET). The lack of accurate values for the X and L valley effective masses (and to a lesser extent the heavy hole effective mass) have made such simulations difficult. Thus, the best available data was used with the depletion approximation to construct a model of the conduction band near pinch-off and calculate the values for channel depth.
The biggest difference between the two models was an effective $\Delta E_c$ difference of 0.13 eV between the In$_{.15}$Ga$_{.85}$As and the GaAs material$^{117, 126, 127}$, thus $\Delta E_c$ is given by:

$$\Delta E_c (\text{Al}_{.21}\text{Ga}_{.79}\text{As}—\text{In}_{.15}\text{Ga}_{.85}\text{As}) = .13 + (1.247)(0.21)(0.63) = .294 \text{ eV}.$$  

The conduction band diagram for the InGaAs channel device is shown in Figure 5.12. Using the same equation as before,

$$V_t + V_b - \Delta E_c = \frac{q N_a d^2}{2 \varepsilon},$$

and knowing the layer thicknesses prior to the gate recess, one again gets a relationship between the etch depth and the threshold voltage. In this case, the structure is less complicated, without any graded layer to worry about. The equation for the effective saturation velocity can then be applied.

The effective saturation velocity of these devices as a function of gate length is shown in Figure 5.13. The values of the GaAs channel devices are shown on the same graph for comparison. The InGaAs channel devices do not seem to show any real fall off of the peak effective saturation velocity as was observed in the GaAs channel system—but experimental scatter may mask such an effect.

A number of points should be made. First, the lower InGaAs data point at about .07 $\mu$m is probably a spurious one, given the large cluster of data points with virtually the same gate length above it. It is extremely easy to measure the peak transconductance of a good device and receive a low value, simply by having a bad probe contact and not realizing it. Secondly, the data shown above for the InGaAs MODFET's came from two separate runs. If the results are broken up into
two sets, there is a slight increase in the effective saturation velocity as the gate length is reduced
in one, and a flat dependence in the other.

![Saturation Velocity vs Gate Length](image)

**Fig. 5.13.** Effective saturation velocity comparison between the InGaAs channel MODFET and the GaAs channel MODFET. The GaAs data are represented as the solid line shown in Fig. 5.9, while the individual points are shown for the InGaAs MODFET.

The physical dimensions of both the InGaAs and the GaAs channel devices were as similar as we could make them. The etch depths for both the InGaAs and the GaAs MODFET's were for the most part, a little above 750 Å, leaving a little less than 350 Å between the gate and the channel. Thus the distance between the n+ cap and the gate was also the same. All in all, an electron in both devices should experience similar electric fields as it is propelled through the channel of the device.

This geometrical similarity between the structures is very important in making a comparison between them. First of all, it should be noted that the saturation velocity should also be corrected for the effective gate length for the InGaAs channel devices in the same manner as that proposed for the GaAs devices. As opposed to the GaAs case, such a correction would most definitely cause the effective saturation velocity to continue to rise as the gate length is reduced.

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well below 0.15 μm. Secondly, it allows us to consider why the InGaAs channel MODFET's might support a continued rise in the peak transconductance (or a larger rise in saturated electron velocity) as the gate length is reduced below 0.15 μm, whereas the GaAs MODFET's do not. To do that, we return to the work of Kizilyali et al.\textsuperscript{124}.

When the device is in the nearly pinched off state ($I_L$), ballistic effects dominate, and there is little change in the current as the gate length is reduced. Minimal differences should be seen in this state between the InGaAs and the GaAs devices. However, in the fully on state ($I_H$), where the saturation effects dominate, the advantages of the InGaAs channel are more pronounced. Mobility reduction due to scattering into the L band will occur at higher electric field (a shorter gate length), as the electron will have to acquire more energy to achieve the transition, given the larger $\Gamma$ to L spacing. During its stay in the $\Gamma$ band, it will benefit from the higher low-field mobility of InGaAs. The electrons will also benefit from the better confinement from the backside of the InGaAs channel device as the electron's energy is increased, reducing scattering into the lower mobility bulk GaAs. The crossing point signaling a leveling off of the transconductance should occur at a shorter gate length for the InGaAs channel device.

A number of factors can serve to uniformly increase the InGaAs channel device's effective saturation velocity with respect to the GaAs MODFET's values. A decrease in the value used for the conduction-band offset ($\Delta E_C$) at the InGaAs-AlGaAs interface will increase the calculated effective saturation velocity, though only slightly (a drop of 0.2 eV will raise all values by about 5%). This does not seem unreasonable, given the recent paper by Menéndez et al.\textsuperscript{128} who concludes that, in disagreement with previous work, the valence-band offset is larger that the conduction band offset in the InGaAs-GaAs system for low ($x=0.05$) indium content. Another factor that is more serious is the accuracy of the AlGaAs doping level. As little as a 12% reduction in the actual doping level from that used in the calculation of the etch depth will cause all values of the effective saturation velocity to rise by another 5%. A 20% change (or more) in each wafer's doping level from that used would not be unreasonable. Thus it would be unwise to conclude
anything about the absolute magnitude of the true saturation velocity to within 15 or 20% of the values listed. For example, it would be completely erroneous to conclude from the figure that the saturation velocities for the InGaAs channel devices were lower than for the GaAs devices, an observation which would contradict the higher expected saturation velocities for the InGaAs material. It is entirely possible that the actual saturation velocity in the InGaAs channel is indeed higher than that of the GaAs.

Another point of comparison can be made from an applications point of view if one looks strictly at the peak transconductance of the two types of devices as a function of gate length. A higher peak transconductance is desired for the best high speed performance as described in Chapter 2 (though there is no substitute for an actual high frequency measurement), the InGaAs channel device becomes more attractive at the shorter gate lengths. For design of MODFET's with a similar physical structure, in order to take full advantage of the small gate size below 0.15 μm, going to a structure with double confinement and an InGaAs channel is preferable. By proper design of such a structure, it should be possible to continue to improve device performance by reducing the gate length below 0.1 μm. Monte Carlo simulations should be used to assist in optimizing the device design, with particular focus on reducing the effective gate length.

5.8 Summary

In this chapter the fabrication of GaAs channel and InGaAs channel MODFET's of similar geometrical design were described. Complete dc characterization of each device was performed. The peak intrinsic transconductance was obtained from the extrinsic value in conjunction with the measured source resistance and output conductance. The actual etch depth was obtained from a combination of the low field threshold voltage and the theoretical band structure of the device. Use of an effective saturation velocity instead of directly comparing the peak intrinsic
transconductance permitted a first order correction for the variation in etch depth from device to device, though the variance itself was less than expected. Equating the curves with the actual saturation velocity should be done only after making corrections for the effective gate length and allowing for vertical shifts of the curves due to doping and conduction band discontinuity uncertainties.

The effective saturation velocities as a function of gate length were compared for both types of devices. For the GaAs channel device a peak in the transconductance was observed at approximately 0.15 μm in agreement with the theory of Kizilyalli et al.\textsuperscript{124}. For the InGaAs channel, \textit{doubly confined structure}, no peak in the maximum transconductance was observed. It is postulated that the double confinement, in combination with the decreased scattering and reduced electron effective mass expected in the InGaAs channel, would cause movement of such a peak to a shorter gate lengths.

The implication of this work for the fabrication of high speed devices and circuits is that a shorter gate length MODFET is not necessarily a better, faster device. The utmost care needs to be taken to consider the scattering properties of the electrons in the device on the length scales that are being considered, especially as one approaches 0.1 μm gate lengths. From this study it would seem that a structure with double confinement and/or with a larger \Gamma to \textit{L} valley separation than that of GaAs is preferable to obtain the greatest device performance benefits from going to ultra-short gate length MODFETs.
Chapter 6

Summary and Suggestions for Further Work

We have explored and successfully demonstrated the fabrication and characterization of small geometry GaAs Field-Effect Transistors, specifically the MESFET and the MODFET with channels as short as 500 Å.

MESFET's exhibited values of transconductance of about 250 mS/mm for gate lengths of 900 Å to 0.5 μm, and decreased for the shortest gate lengths, implying negligible velocity overshoot effects. Scaled devices with intrinsic transconductances of approximately 500 mS/mm and gate lengths to 650 Å also did not show appreciable velocity overshoot effects.

Traditional GaAs channel MODFET's and InGaAs channel MODFET's with a bottom electron confining layer were fabricated with gate lengths from 2 μm to 550 Å. The effective peak saturation velocities (the transconductance corrected to first order for recess depth nonuniformities) were then compared as a function of gate length. For gate lengths down to about 0.2 μm, as velocity overshoot effects become more important, the peak transconductance in the MODFET is expected to increase as the gate length is reduced\textsuperscript{129}. As expected, our GaAs channel MODFET's showed an increase in the peak, saturated velocity as the gate length was reduced to 0.15 μm. As the gate length was reduced even further, a decrease in the peak effective saturation velocity was observed for the GaAs channel MODFET, agreeing with the prediction of Kizilyalli \textit{et al.}\textsuperscript{124} for a maximum transconductance at a gate length of about 0.15 μm. However, for the InGaAs confined channel device, virtually no dependence on gate length of the transconductance was observed. It is postulated that the extra confinement of the electrons in the channel afforded by the structure of the InGaAs device, along with the higher energy necessary for electrons to scatter from the Γ to L band in the InGaAs channel, prevented electron scattering at the electric fields associated with device operation in the short gate limit. More work
is necessary to further explore these effects. From this study it would seem that a structure with
double confinement and/or with a larger \( \Gamma \) to \( L \) valley separation than that of GaAs is preferable to
obtain the largest device performance benefits from going to ultra-short gate length MODFET's.

For continuation of this work, the process should be changed to allow the formation of a
T-shaped gate electrode in a manner so as not to sacrifice resolution. The most obvious limitation
to this work was the inability to meaningfully measure the high frequency characteristics of the
devices due to the high resistivity of the thin gate electrode. Our concern with trying to achieve
the smallest gate electrode possible lead us to stay with a proven electron-beam writing technique
which had demonstrated the capability of fabricating 200 Å metal features, despite its restriction of
gates only 500-700 Å thick.

A full Monte Carlo simulation of the devices should be carried out. This would determine
the proper correction for the effective saturation velocity curves and the true effective gate
length. Thus we would better know just how much of a downturn (if any) is expected in the GaAs
channel MODFET's as the gate length is reduced to below 0.15 \( \mu \)m. A more detailed simulation
could determine the fields and velocities seen by an electron in the channel, and thus be better
able to confirm the transport model. The true saturation velocities could also be calculated and
compared in more detail.

The technology developed here for devices that have single gates with lengths on the
order of 500 Å can also be employed to make devices with multiple lines on the same length
scale. Once this is achieved there are a host of possibilities, including the making of superlattice
like structures in the lateral plane of the crystal, otherwise known as lateral surface superlattice
devices\textsuperscript{130, 131}, corrugated gate MODFET structures\textsuperscript{132}, or perhaps even a lateral resonant
tunneling field-effect transistor\textsuperscript{133}. 

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Appendix A

Determination of Mobility and Carrier Concentration of Separate Hall-bar Samples Connected in Parallel

A.1 Introduction

As demonstrated in Chapter 2, under certain circumstances, the parasitic MESFET in a MODFET structure may begin to conduct. Under these conditions, a Hall effect measurement no longer will simply measure the mobility and sheet carrier concentration of the two-dimensional electron gas layer. Instead, the situation can be best modeled by two, noninteracting layers, connected only in the region of the ohmic contacts. If the layers were unconnected, given the different sheet resistivities and mobilities of the carriers in the two layers, application of a current under a magnetic field would generate different electric fields in each of the layers. Connected, these fields would cause a number of loop currents to flow between the layers.

We will first look at the case of a single layer Hall bar sample. After deriving the general Hall effect equations for determining the mobility and carrier concentration in this layer, we will then consider the case of two Hall bars connected at six points, and how, by utilizing multiple measurements at different magnetic fields, the mobilities and carrier concentrations in each layer might be extracted.

A.2 Single Layer Hall Bar Measurement

Consider a single Hall bar of the form shown with the shaded sections being ohmic contacts to the semiconductor bar:
where $r$ is one half the width of the sensing fingers and $x$ and $y$ represent the coordinate system for fields, currents, etc.

In order to make calculations easier to follow we will universally define the current density as the sheet density (the usual current density times the Hall bar thickness), and the carrier density as the sheet density (usually defined as $n_s$, the sheet carrier density). This will prevent a thickness factor being carried throughout.

The relationship between the current and electric fields is usually given by

$$\vec{E} = \rho \vec{J},$$  \hspace{1cm} (1)

where

$$\rho_{xx} = \rho_{yy} = \frac{1}{n q \mu},$$ and $$\rho_{xy} = \rho_{yx} = \frac{B}{n q}. $$  \hspace{1cm} (2)

Letting

$$\sigma = \rho^{-1},$$  \hspace{1cm} (3)

the alternative way of relating the current to the electric field is given by
\[ \vec{J} = \sigma \vec{E}, \]  

(4)

where

\[ \sigma_{xx} = \sigma_{yy} = \frac{n \mu q}{1 + \mu^2 B^2}, \]  

(5)

and

\[ \sigma_{yx} = -\sigma_{xy} = \frac{n \mu^2 B q}{1 + \mu^2 B^2}. \]  

(6)

Then if we impose the conditions for a Hall measurement:

- Apply a magnetic field perpendicular to the plane of the paper (vector with magnitude \( B \)).
- Source current out of the left end of the bar and sink it out of the right by applying a voltage \( V_2 - V_1 > 0 \).
- Measure \( V_3, V_4, V_5 \), and \( V_6 \) while drawing a negligible amount of current out of the sensing fingers.
- Make the bar sufficiently long so that the \( E \)-field in the center that will be developed as a result of current flowing from left to right with the magnetic field on will not be affected by the presence of the contacts at the ends. This condition implies that there will be no current flowing from top to bottom in the region of concern near the center. Under these conditions,

\[ J_x = \sigma_{xx} E_x + \sigma_{xy} E_y, \]  

(7)

and

\[ J_y = 0 = \sigma_{yx} E_x + \sigma_{yy} E_y, \]  

(8)

therefore,

\[ E_y = -E_x \frac{\sigma_{yx}}{\sigma_{yy}} = -\frac{n \mu^2 B q}{n \mu q} = -\mu B E_x, \]  

(9)
thus,

\[ \mu = \frac{E_y}{E_x B} \]  \hspace{1cm} (10)

The assumption that the bar is sufficiently long, along with equation (10), implies that

\[ I \propto E_x \propto E_y, \]  \hspace{1cm} (11)

and thus \( E_x \) and \( E_y \) are constant everywhere (within the area of consideration in the center). So in this case we can determine the sheet carrier concentrations and mobility (which is assumed constant throughout this piece of semiconductor) from the voltages measured at each of the four points \( V_3, V_4, V_5, \) and \( V_6 \):

\[ E_x = \frac{V_1 - V_2}{2a + b} = \frac{V_3 - V_4}{b} = \frac{V_5 - V_6}{b}, \]  \hspace{1cm} (12)

\[ E_y = \frac{V_5 - V_3}{W} = \frac{V_6 - V_4}{W}, \]  \hspace{1cm} (13)

so from (12),

\[ V_3 - V_4 = (V_1 - V_2) \frac{b}{2a + b}, \]  \hspace{1cm} (14)

and from equations (4-8),

\[ I = J_x W = W n \mu q \left[ \frac{E_x}{1 + \mu_2 B^2} - \frac{\mu B E_y}{1 + \mu^2 B^2} \right]. \]  \hspace{1cm} (15)

Using equations (10) and (12),

\[ I = W n \mu q \left[ \frac{E_x}{1 + \mu_2 B^2} + \frac{\mu_2 B^2 E_x}{1 + \mu^2 B^2} \right] = W n \mu q E_x = W n \mu q \frac{(V_1 - V_2)}{2a + b}, \]  \hspace{1cm} (16)

or, as expected,
\[
    n = \frac{1}{q \mu \rho} = \frac{I}{q \mu E_x W}.
    \tag{17}
\]

So, from equations (12) and (17),

\[
    V_1 - V_2 = \frac{\rho I (2a + b)}{W},
    \tag{18}
\]

and from equation (14),

\[
    V_3 - V_4 = \frac{\rho I b}{W},
    \tag{19}
\]

and from equation (10), (13) and (17),

\[
    V_5 - V_3 = -B \mu \rho I.
    \tag{20}
\]

A.3 Two Separate Hall Bars, Connected

Now let us consider the case of two separate Hall bars, connected as if by wires only at the contacts. Each of these layers will have different carrier mobilities, and different carrier concentrations. Current can now flow in and out of the contacts previously used only to sense the voltages, flowing between the layers through these connections. However, the net current out of the sensing fingers will still be zero (we will use a very high resistance volt meter), and the net current out of the left and right side will still total \( I \).

If one considers a point in the center of the Hall bar, all currents are invariant under coordinate inversion plus time reversal symmetry. From this we immediately obtain that, for each layer, the currents flowing into the contacts \( V_3, V_4, V_5, \) and \( V_6 \) are related as:

\[
    I[V_3] = -I[V_6] \quad \text{and} \quad I[V_5] = -I[V_4].
    \tag{21}
\]

Therefore, it immediately follows that since

\[
    I[V_3] + I[V_4] + I[V_5] + I[V_6] = 0,
    \tag{22}
\]

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we can consider the current that flows between adjacent layers as that due to three separate current loops as shown in Figure A.2 and A.3.

![Diagram of current loops](image)

Fig. A.2. Diagram showing one of the of interacting current loops in a Hall bar fabricated with two noninteracting current layers with different mobilities ($V_{1,2}$ current loop). The total current in each layer is $I$ plus that due to the loop.

![Diagram of current loops](image)

Fig. A.3. Diagram showing the remaining two current loops in a Hall bar fabricated with two noninteracting current layers with different mobilities.

The two loops shown in Figure A.3 can be looked at as two sets of identical current loops as shown in Figures A.4 and A.5, by defining the loop currents in terms of the diagonal loops shown in Figure A.3:

\[ I_{3-4} = I_{4-5} = \frac{I_{4-5} + I_{3-6}}{2}, \]

and

\[ I_{5-6} = I_{4-6} = \frac{I_{4-5} - I_{3-6}}{2}. \]
Fig. A.4. Figure showing identical $V_{3.5}$ and $V_{4.6}$ current loops.

Fig. A.5. Similar figure showing identical $V_{3.4}$ and $V_{5.6}$ current loops.

Thus, in order to find the relations between the mobilities and carrier concentrations as a function of the measured voltages, magnetic field, and source current, we need only consider the voltages generated from three separate currents under a magnetic field: the source current $I$ and the two loop currents. These can be considered separately, and then using superposition, combine them in the end. Thus we will solve:

- **Case 1:** Current ($I_1$) is sourced in $V_1$ and sunk out of $V_2$. No current will flow out of the probing fingers, $V_{3,4,5,6}$. This is the simple case of one level revisited.

- **Case 2:** Source current ($I_2$) in $V_3$ and sink it out of $V_3$. No current will flow in or out of any other point. Use artificial boundary conditions such that the edges are staggered by one-half the finger spacing ($b$). Calculate the voltages at all points generated. Take this result and by adding it to the identical case of sourcing in $V_6$ and sinking it out of $V_4$, and calculate the case of current $I_2$ flowing through both loops at the same time with the proper boundary conditions. (The two cases will add to give the proper conditions.)
Case 3: Source current ($I_3$) in $V_3$ and sink it out of $V_4$. Again, no current will flow in or out of any other point. Calculate the voltages at all points generated. Proper boundary conditions are satisfied at once.

In each of these cases, our aim is to determine the relationship between the source currents and the voltages:

\[ V_1' = V_1 - V_2, \]  \hspace{1cm} (25)

\[ V_2' = V_5 - V_3, \]  \hspace{1cm} (26)

\[ V_3' = V_3 - V_4. \]  \hspace{1cm} (27)

We have almost completely solved the first case as above:

\[ V_1' = \frac{(2a + b)}{n \mu q W} I_1 = \rho \frac{(2a + b)}{W} I_1, \]  \hspace{1cm} (28)

\[ V_2' = -\frac{B}{n q} I_1 = -B \mu \rho I_1, \]  \hspace{1cm} (29)

\[ V_3' = \frac{b}{n \mu q W} I_1 = \rho \frac{b}{W} I_1. \]  \hspace{1cm} (30)

It is prudent to first solve the general case here before proceeding to the third case, as the second case is a special case of the third, while the third case requires solution of the general case.

We will first consider the general case by looking at an infinite sheet of current sources (including image sources), each sourcing or sinking a current $I_2$, arranged in such a way to fulfill the boundary condition that no currents will flow in or out of the edge of the sample (with the exception of the real sources). Each will be considered a point source. This is illustrated in Figure A.6.
Fig. A.6. Layout of real and image sources for calculating the voltage generated between two symmetrically placed points in the general case of two sources placed on the center line of a rectangular sample, evenly spaced from the upper and lower edges as shown.
At a distance $r$ from the source, the potential from a single source is given by

$$\phi - \phi_0 = \frac{I}{2\pi} \rho_s \ln(r),$$

(31)

where $r$ is the distance from the source to the point of measurement. For a dipole source, the difference in potential is given by

$$\phi_2 - \phi_1 = \frac{I}{2\pi} \rho_s \ln \frac{r_1}{r_2}.$$  

(32)

Ollendorff\textsuperscript{136} uses the above equations to calculate the potential distribution at a point $(x,y)$ away from the case of a line of current sources, sinking at infinity:

$$\phi - \phi_0 = \frac{I}{2\pi} \rho_s \ln \left[ 2 \sqrt{ \frac{\sin \left( \frac{\pi}{T} \right)}{\sinh \left( \frac{\pi}{T} \right)} x + \frac{\sinh \left( \frac{\pi}{T} \right)}{\sinh \left( \frac{\pi}{T} \right)} y } \right],$$

(33)

where $l$ is the spacing between the sources, and $x$ and $y$ are defined as shown in Figure A.7.

![Diagram showing a coordinate system for potential of a line of sources as described in equation (33).](image)

Fig. A.7. Coordinate system for potential of a line of sources as described in equation (33).

We must sum the contribution of each line of sources to the voltage difference $\Delta V$. For purposes of convergence, we need to sum in groups of four (current conservation would necessitate summing in minimum groups of two, one positive line with one negative line). Once the special case of the center two sources is taken care of, we need only sum over the positive $x$ direction and multiply the result by two due to symmetry considerations.
For purposes of simplicity, we can pull $I$ and $\rho$ out of the summation, by defining a series of numerical constants, $(a_n)$, only dependent on the geometry, by the following equation:

$$\Delta V = I \rho \left[ a_0 + \sum_{n=1}^{\infty} a_n \right],$$

(34)

where each $a_n$ will be defined as the contribution ascribed to four lines (with the exception of $a_0$ which includes only the center two real sources). Thus, $a_0$ is given by:

$$a_0 = \left( \frac{\Delta V_{\text{Source line 0 (n=0)}}}{I \rho_s} - \frac{\Delta V_{\text{Source line 0 (n=0)}}}{I \rho_s} \right),$$

(35)

$$= \frac{1}{2 \pi} \ln 2 \sqrt{\sinh^2 \left( \frac{\pi (f - 2c - s)}{l} \right) + \sin^2 \left( \frac{\pi g}{l} \right)} - \frac{1}{2 \pi} \ln 2 \sqrt{\sinh^2 \left( \frac{\pi s}{l} \right) + \sin^2 \left( \frac{\pi g}{l} \right)},$$

(36)

or

$$a_0 = \frac{1}{\pi} \ln \sqrt{\frac{\sinh^2 \left( \frac{(f - 2c - s) \pi}{l} \right) + \sin^2 \left( \frac{\pi g}{l} \right)}{\sinh^2 \left( \frac{s \pi}{l} \right) + \sin^2 \left( \frac{\pi g}{l} \right)}}.$$

(37)

Similarly, for $n > 0$, and multiplying by two to include the identical contribution from $n < 0$,

$$a_n = \frac{1}{2 \pi} \ln \left( \frac{s_{11} s_{41} s_{22} s_{32}}{s_{12} s_{42} s_{21} s_{31}} \right),$$

(38)

where

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\[ s_{11} = \sinh^2 \left( \frac{(m + 1) - s}{l} \pi \right) + \sin^2 \left( \frac{\pi g}{l} \right), \]  
\[ s_{12} = \sinh^2 \left( \frac{(m + 2) + 2c + s}{l} \pi \right) + \sin^2 \left( \frac{\pi g}{l} \right), \]  
\[ s_{21} = \sinh^2 \left( \frac{(m + 2) - 2c - s}{l} \pi \right) + \sin^2 \left( \frac{\pi g}{l} \right), \]  
\[ s_{22} = \sinh^2 \left( \frac{(m + 1) + s}{l} \pi \right) + \sin^2 \left( \frac{\pi g}{l} \right), \]  
\[ s_{31} = \sinh^2 \left( \frac{(m + 2) - s}{l} \pi \right) + \sin^2 \left( \frac{\pi g}{l} \right), \]  
\[ s_{32} = \sinh^2 \left( \frac{(m + 2) + 2c + s}{l} \pi \right) + \sin^2 \left( \frac{\pi g}{l} \right), \]  
\[ s_{41} = \sinh^2 \left( \frac{(m + 3) - 2c - s}{l} \pi \right) + \sin^2 \left( \frac{\pi g}{l} \right), \]  
\[ s_{42} = \sinh^2 \left( \frac{(m + 2) + s}{l} \pi \right) + \sin^2 \left( \frac{\pi g}{l} \right), \]  

and where

\[ m = 2(n - 1). \]  

Now that the general case is solved, we can now solve without much difficulty the second case.

In all cases we define the current source or sink to be of radius \( r \). \( r \) will be defined as one-half the width of the sensing fingers. The actual source will look like a half circle at the finger. We assume that the ohmic contacts have this shape, though the final result should have very little to do with this. Thus, in the case where the current source and the sensing points are the same set of fingers, the sensing points will be \( r \) away from the source.
We need to consider two sets of sources, as mentioned previously, or alternatively, calculate $V_3-V_3$ and add in $V_6-V_4$ to the $V_3-V_3$ value, as the two sets are identical. For the second case, to calculate $V_5-V_3$,

$$f = W, \quad l = 2a + b, \quad s = I, \quad g = 0, \quad c = 0. \quad (48)$$

and to calculate $V_6-V_4$,

$$f = W, \quad l = 2a + b, \quad s = I, \quad g = b, \quad c = 0. \quad (49)$$

As an example, we use the dimensions of the sample Hall bar that was used for the measurements described in Chapter 2:

$$a = 345 \, \mu m \quad b = 290 \, \mu m \quad W = 125 \, \mu m \quad r = 2.5 \, \mu m,$$

$$L = 980 \, \mu m$$

For case two, for $V_3-V_3$,

$$f = 125 \, \mu m, \quad l = 980 \, \mu m, \quad s = 2.5 \, \mu m, \quad g = 0, \quad c = 0, \quad (50)$$

and

$$\text{Sum}_1 = 2.202775.$$ 

For case two, for $V_6-V_4$,

$$c = 125 \, \mu m, \quad L = 980 \, \mu m, \quad s = 2.5 \, \mu m, \quad g = 290, \quad c = 0, \quad (51)$$

and

$$\text{Sum}_2 = 8.6839198 \times 10^{-4}.$$ 

Therefore, the total effect of $I_2$ flowing through the voltage arm contacts, $V_3$ and $V_6$, is that,
\[ V_5 - V_3 = I_2 \rho (\text{Sum}_1 + \text{Sum}_2) = I_2 \rho \ 2.2036. \] (52)

For the perpendicular contributions, the voltage is only dependent on the total amount of current flowing across the two points, so,

\[ V_3 - V_4 = I_2 \rho \mu B, \] (53)

and

\[ V_1 - V_2 = I_2 2 \rho \mu B. \] (54)

We now must solve the third case.

For \( V_3 - V_4 \) we have,

\[ f = L = 980 \ \mu m, \quad l = 125 \ \mu m, \quad s = 2.5 \ \mu m, \quad g = 0, \quad c = 345 \ \mu m, \] (55)

and

\[ \text{Sum} = 2.9600116. \]

\( V_1 - V_2 \) will be identical to \( V_3 - V_4 \). The perpendicular component is then

\[ V_5 - V_3 = I_3 \rho \mu B. \] (56)

Now that all of the separate cases have been solved, we can now solve for each voltage in terms of the current flowing in each loop, invert the matrix relating the two to solve for the currents in terms of the voltages, and then use current superposition to satisfy the external boundary conditions.

To solve for the voltages in terms of the currents we obtain:

\[
\begin{bmatrix}
V'_1 \\
V'_2 \\
V'_3
\end{bmatrix} = \begin{bmatrix}
V_1 - V_2 \\
V_3 - V_4 \\
V_5 - V_3
\end{bmatrix} = r_5 \sigma \begin{bmatrix}
I_1 \\
I_2 \\
I_3
\end{bmatrix},
\] (57)

where each of the matrix elements come from the solutions to the cases considered in the preceding pages. Substituting the values obtained into \( \sigma \) we obtain:
\[ \sigma = \begin{bmatrix} 7.84 & 2\mu B & 2.960 \\ -\mu B & 2.2036 & \mu B \\ 2.32 & \mu B & 2.960 \end{bmatrix} \] (58)

Therefore,
\[ \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \frac{1}{\rho_s} \begin{bmatrix} V'_1 \\ V'_2 \\ V'_3 \end{bmatrix} \] (59)

and
\[ \sum_{1}^{\text{Number of layers}} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} I_{\text{tot}} \\ 0 \\ 0 \end{bmatrix}. \] (60)

Thus, to solve for \( \kappa \) and \( \mu \) for each layer, we minimize,
\[ \left| \left( \sum_{1}^{\text{Number of layers}} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} - \begin{bmatrix} I_{\text{tot}} \\ 0 \\ 0 \end{bmatrix} \right) \right|. \] (61)

Given the nonlinear terms introduced upon inversion of the \( \sigma \) matrix, for a system with \( \kappa \) layers, for each measurement of the system with a unique B-Field, the above equations generate three nonlinear equations in \( 2\kappa \) unknowns, each of which must be minimized with respect to \( \kappa \) and \( \mu \) of each layer. It should be noted that the third equation can be degenerate with respect to the other two, so the number of unique equations is not necessarily three.

There are two serious problems with this analysis that need to be quantified as to their effect. The first is the approximation of the current source as a point contact with a radius equal to one-half the finger width. This is probably a reasonable assumption, given the geometry of the ohmic contacts. The second, more serious assumption is that the contacts between the two layers has zero resistance. This could seriously impact the model. The resistance of the contacts
between layers in a MODFET structure is not only appreciable, but difficult to predict accurately. As opposed to the single layer structure, where current flow can be made as small as is necessary by measuring the voltage of the probe points with a sufficiently high resistance voltmeter, in the case of the multiply connected structure, such currents are intrinsic to the measured values. The addition of the resistance to the model will make the measured values closer to that which would be observed with only the top, parasitic MESFET, if the MESFET has sufficient carriers.
Appendix B

Nanometer MESFET/MODFET Process Schedule

A. Grow epitaxial layers with MBE

B. Isolation

1. Degrease wafer if wafer has been sitting out of MBE for a day or more:
   a. Boil in TCA for 10 minutes
   b. Soak in room temperature acetone for 10 minutes
   c. Boil in methanol for 10 minutes
   d. Soak in room temperature isopropyl for 10 minutes
   e. Blow off wafer with nitrogen gun

2. Deposit photoresist:
   a. Singe wafer for 20 minutes (minimum) at 150 °C
   b. Let cool for 5 minutes
   c. Blow off wafer with nitrogen gun
   d. Spin AZ1370-SF photoresist: 5000 rpm, 30 seconds
   e. Clean resist off bottom of wafer with acetone
   f. Pre-bake resist coated wafer for 30 minutes at 85 °C
   g. Let wafer cool for 10 minutes
   h. Blow off wafer with nitrogen gun

3. Expose photoresist: Ultraviolet expose in contact aligner (6.3 seconds, 9.2 W/cm², measured at 400 nm)

4. Develop photoresist:
   a. Immerse in 1:1 AZ Concentrate developer:H₂O, 60 seconds (20 seconds after clearing), constant mild agitation, ~21 °C
   b. De-ionized water rinse, 40 seconds, constant mild agitation
   c. Light blow dry with nitrogen gun
   d. Postbake 25 minutes @ 85 °C
   e. Let wafer cool 10 minutes
   f. Blow off with N₂

5. Etch mesas
   a. Etch in 1:1:20 NH₄OH:H₂O₂:H₂O @ 20-21 °C (etch rate is 1 μm/minute fresh, 0.8 μm/minute after 2 hours)
   b. Rinse in de-ionized water for 30 seconds

6. Strip photoresist
   a. Soak in boiling acetone 10 minutes (heated in warm water bath—Acetone is HIGHLY FLAMMABLE!—Keep well away from hot plate!)
   b. Rinse in boiling methanol, 5-10 minutes
   c. Soak in room temperature isopropyl for 10 minutes
   d. Visually observe. O₂ plasma if necessary (100 W, 200 mTorr, see step C-7)

* Development times will vary with temperature, age of developer, bake conditions, etc. Times listed are only a guide, as conditions may indicate more or less time, including the necessity, after visual inspection, to develop again for extra time.
C. Ohmic Contacts

1. Degrease wafer if wafer has been sitting around for more than a day or so:
   a. Boil in TCA for 10 minutes
   b. Soak in room temperature acetone for 10 minutes
   c. Boil in methanol for 10 minutes
   d. Soak in room temperature isopropyl for 10 minutes
   e. Blow off wafer with nitrogen gun

2. Deposit bottom layer photoresist:
   a. Singe wafer for 30 minutes at 120 °C
   b. Let cool for 5 minutes
   c. Blow off wafer with nitrogen gun
   d. Spin AZ1370-SF photoresist: 5000 rpm, 30 seconds (~1.1 μm thick). Check photoresist uniformity
   e. Clean resist off bottom of wafer with acetone
   f. Pre-bake resist coated wafer for 30 minutes at 85 °C
   g. Let wafer cool for 10 minutes
   h. Blow off wafer with nitrogen gun

3. Plasma harden bottom layer:
   a. Place on alumina block under deposition plate approximately halfway from center to reduce etching
   b. Expose to C2F6 plasma in Technics PE-II planer etcher* at 26 sccm, 300 W, 50 seconds (Plasma pressure should be ~210 mTorr, background pressure ~30-50 mTorr).

4. Deposit top layer photoresist:
   a. Spin Shipley Microposit 2400, 5000 rpm, 30 seconds (~1.3 μm thickness)
   b. Clean photoresist off bottom of wafer with acetone
   c. Prebake 25 minutes at 85 °C
   d. Let cool 10 minutes
   e. Blow off with N2

5. Expose resist (both top and bottom layers): ultraviolet exposure in contact aligner (14.7 seconds, 9.2 W/cm², 400 nm line)

6. Develop top layer
   a. Immerse in 1:4 Microposit 2401 developer: H2O, 40 seconds constant mild agitation at 18 °C
   b. De-ionized water rinse 15 seconds
   c. N2 blow dry
   d. Visually observe—uniform coloring should be observed in developed areas, repeat b-d if necessary (usually 10 seconds more needed)

7. Plasma etch hardened layer (step 3)
   a. Technics PE-II, O2 at 27.7 sccm, 100 W, 1 minute, plasma pressure is 200 mTorr
   b. Visually inspect: cloudy to clear

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*Note: System must be scrubbed with abrasive pad regularly to remove AlF2 buildup and kept free of unwanted oxygen leaks. Times and pressures will vary based on condition of system.
8. Develop bottom layer
   a. 1:1 AZ developer:H₂O 50 seconds 21 °C
   b. Visually inspect for complete development and overhang
   c. 20 seconds additional O₂ plasma (usually necessary)

9. E-beam deposit metals:
   a. Ge 200 Å
   b. Au 500 Å
   c. Ni 250 Å
   d. Au 1000 Å

10. Lift-off
    a. Soak in acetone 5 minutes
    b. Remove metal under acetone stream with air brush, finally soaking in clean acetone
    c. Rinse in methanol
    d. Rinse in isopropyl
    e. Blow off wafer with nitrogen gun

11. Anneal: 30 seconds at 450 °C furnace (or RTA)

D. Nanometer Gate Fabrication

1. Wafer degrease: Degrease wafer if wafer has been sitting around for more than a day:
   a. Boil in TCA for 10 minutes
   b. Soak in room temperature acetone for 10 minutes
   c. Boil in methanol for 10 minutes
   d. Boil in isopropyl for 10 minutes
   e. Blow off wafer with nitrogen gun

2. Pre-PMMA deposition final clean*: 
   a. O₂ plasma clean (Technics PE-II planer etcher, 27.7 sccm O₂, 100 W, 45 seconds)
   b. Dip in concentrated HF, 15-20 seconds
   c. Heavy de-ionized water rinse (Use water that has been sitting for at least 10-15 minutes)
   d. Blow off wafer with nitrogen gun
   e. Dip in concentrated H₂SO₄, 10 seconds
   f. Heavy de-ionized water rinse
   g. Blow off wafer with nitrogen gun
   h. 1:25-30 NH₄OH:H₂O, 10-15 seconds
   i. Through N₂ blow dry

* Note: Steps b-i and 3a must be done without delay between steps, minimizing exposure to air and to heat generated when wafer is placed in rinse water (steps c and f). Rinse water must stand to reduce dissolved O₂.
3. Deposit PMMA
   a. Immediately spin 2% PMMA (8000 rpm., 30 seconds, thickness ~700 Å)
   b. Clean PMMA off bottom of wafer with acetone
   c. Prebake wafer (4 hours, 175 °C)
   d. Let cool 20 minutes
   e. Blow off with N₂

4. Write gates with UHREBL

5. Develop PMMA:
   a. Immerse in 3:7 cellosolve:methanol (7 seconds, very critical)
   b. Immerse in methanol (10 seconds)
   c. Rinse in isopropyl (30 seconds)

6. Recess gates:
   a. 10:1:30 citric acid (50% by weight stock solution):H₂O₂:H₂O at 21 °C
      Etch depth (nm) = 6.8 + 29.4 × t[minutes]
   b. De-ionized water rinse 30 seconds

7. E-beam deposit metals:
   a. Ti 80-100 Å
   b. Al 300-500 Å
   c. Au 100-200 Å

8. Lift-off
   a. Soak in acetone 5 minutes
   b. Remove metal under acetone stream with air brush, finally soaking in clean acetone
   c. Rinse in methanol
   d. Rinse in isopropyl
   e. Blow off wafer with nitrogen gun

E. Final Metallization

1. Repeat steps C1-C6

2. Metal deposition (e-beam)
   a. Ti 250 Å
   b. Pt 500 Å
   c. Au 2000-2750 Å

3. Lift-off
   a. Soak in acetone 5 minutes
   b. Remove metal under acetone stream with air brush, finally soaking in clean acetone
   c. Rinse in methanol
   d. Rinse in isopropyl
   e. Blow off wafer with nitrogen gun

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