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Studies of the nucleation and growth of gallium arsenide on silicon by molecular beam epitaxy

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Stanford University, 1988

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STUDIES OF THE NUCLEATION AND GROWTH OF GALLIUM ARSENIDE ON SILICON BY MOLECULAR BEAM EPITAXY

A DISSERTATION SUBMITTED TO THE DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING AND THE COMMITTEE ON GRADUATE STUDIES OF STANFORD UNIVERSITY IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

by Stephanie Maxine Koch

August 1988
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ABSTRACT

The heteroepitaxy of gallium arsenide on silicon provides a means of combining gallium arsenide optoelectronic devices and high-speed electronics with silicon integrated circuits. While gallium arsenide/silicon technology has advanced considerably in the past few years, problems with the structural quality of the gallium arsenide/silicon films greatly impede further progress. The aim of the work described in this dissertation is an understanding of the initial stages of gallium arsenide/silicon growth and their effects on the quality of the gallium arsenide layers. All of the films were grown by molecular beam epitaxy (MBE) and analyzed by a number of characterization methods, including transmission electron microscopy (TEM), Rutherford backscattering spectrometry (RBS), and reflection high energy electron diffraction (RHEED).

Gallium arsenide/silicon nucleation occurs in the form of islands, which are compressively strained in the plane of the film due to the 4% lattice mismatch. As the islands gradually coalesce to form a complete film, the film crystallinity improves considerably, and the strain relaxes as a result of misfit dislocation formation. We find that island formation causes surface morphology degradation, and island coalescence appears to be the source of additional defects. Beginning the growth with a low-temperature buffer layer greatly improves the surface morphology without degrading the crystallinity of thick films. Both ion channeling and cross-sectional TEM show a marked change in the defect density in the region of the buffer layer/overlayer interface.

The silicon substrates we employed had been intentionally misoriented from (100) in order to create a staircase of steps on the silicon surface. Cross-sectional TEM images show that these steps tend to form step bands during the substrate heat treatment prior to the growth. The vast majority of the gallium arsenide islands nucleate at these step bands and grow along them. The island shape depends on the degree and direction of the substrate misorientation from the [100] surface normal, reflecting the underlying step arrangement. The planar compressive strain within the islands is affected by these steps as well. The implications of these findings on the optimal substrate misorientation and preparation procedure are discussed.
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CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 Introduction

Several decades ago, the fabrication of transistors was seriously hindered by problems in crystal growth and semiconductor processing. Subsequent improvements in these areas paved the way for greatly improved transistors and ultimately integrated circuits, which have now reached a level of very large scale integration (VLSI). Initially, alterations in the electrical properties of semiconductors were limited simply to the adjustment of dopant types and concentrations. More recently, electronic devices have also utilized compositional changes in the material, leading to the development of lasers and becoming the foundation for nearly all optoelectronic devices. More recently, the interface between two different semiconductors has formed the basis for new device concepts. New techniques in materials synthesis are now bringing about other important advances, providing ways of growing structures that had been only theoretical concepts several years ago. Currently, structures can be made smaller than the electron wavelength, such that quantum mechanical effects that are unimportant in bulk materials are now completely dominant. In fact, crystal growers can deposit junctions as abrupt as a single atomic layer. Such technological advances permit the fabrication not only of improved transistors and integrated circuits, but also of radically different electronic devices, which will have applications to high data rate communications and eventually to ultra-high speed computers [1].

One important emerging technology is the possibility of combining Si and compound semiconductor technologies. Si is the dominant semiconductor used in
electronic devices today. Its advantages include a stable native oxide and availability. Perhaps most importantly, the ease of processing Si led to the development of a well-established Si processing technology which is the foundation of today's electronic and computer industries. Presently, very large diameter wafers can be produced and extremely complex circuits can be routinely manufactured. Although Si will almost certainly remain the dominant semiconductor in the future, there is a growing trend to use other semiconductors. In particular, GaAs, AlGaAs, Si-Ge, InGaAs, InGaAsP and HgCdTe are now used in applications for which Si is unsuitable. GaAs, the most widely established compound semiconductor, offers a number of advantages over Si: it has a direct bandgap, necessary for efficient light absorption and emission in optoelectronic devices, and a higher electron mobility, making faster devices possible. The different band structures of other semiconductors provide variations in such properties as carrier effective mass, bandgap, and transport behavior, useful for other applications. In addition, the alloy composition of Si-Ge, ternary and quaternary semiconductors can be adjusted to tailor the bandgap ($E_g$) and lattice parameter ($a_0$) to desired values. With binary and ternary materials, however, $E_g$ and $a_0$ are not independent variables -- this is the case only for quaternary materials over a limited compositional range. By combining the particular features of these different materials, extremely complex and versatile structures can be achieved.

A great deal of work is currently being done to prepare thin films of these semiconductors for device applications. However, only a limited number of semiconductors, particularly Si, GaAs and InP, are available for use as substrates for these thin films; many other materials are prohibitively difficult to prepare in bulk quantities, or are simply unsuitable as substrate material. For this reason, the preparation of films that are lattice-mismatched to the substrate is now receiving considerable attention.

The combination of GaAs and Si is particularly compelling because these materials are by far the most important semiconductors in use today. There are a number of reasons for this: numerous devices have been designed specifically for Si and GaAs, their
properties are complementary, and both materials possess a highly developed processing technology. The goals of GaAs and Si integration include optical interconnects, optoelectronic integrated circuits (OEIC) and monolithic integration of ultra-high speed GaAs with high density Si VLSI. In addition, Si wafers can be used merely as substrates for GaAs integrated circuits: they are available in larger sizes than GaAs wafers; they are less brittle, cheaper, and have a higher thermal conductivity than GaAs. This latter property is important for heat removal in both device and IC applications and in minimizing dislocations in bulk crystal growth. In large diameter (>4") bulk growth of GaAs, the poor thermal conductivity of the material leads to large thermal gradients; the resulting stress is relieved by dislocation formation or, in the worst case, fracture. Thus, for very large area substrates, some form of heteroepitaxy may offer the only solution.

There are basically three ways to integrate GaAs and Si devices and circuits. First, separately packaged devices or ICs can be combined on a circuit board. Second, devices or circuits can be hybrid mounted in the same package. Finally, Si and GaAs devices can be monolithically integrated by epitaxial growth of GaAs on Si. In both the non-integrated and hybrid approaches to combining GaAs and Si, the complication of interconnection, with the resulting parasitic inductances and capacitances, leads to such problems as noise, line reflections, resonances and additional power consumption, which often outweigh the potential advantages. This can be overcome only by growing GaAs directly on Si and combining the different devices monolithically. Because GaAs cannot withstand the high temperatures needed in Si device processing, the Si devices need to be fabricated before the GaAs is grown on the wafer.

While the advantages of this technology have been apparent for some time, the GaAs/Si growth itself has proven to be extremely difficult. One problem is that the lattice parameter of GaAs is 4.1% larger than that of Si at room temperature. In addition, there is a factor of two difference in thermal expansion coefficients between the materials. Because the value for GaAs (6.86ppm/deg C) is larger than for Si (2.6ppm/deg C), tensile stresses
develop in the GaAs parallel to the GaAs/Si interface upon cooling from the growth temperature; this leads to wafer bowing and even crack formation in layers thicker than 4 or 5 μm. These lattice and thermal expansion coefficient mismatches are responsible for the high defect densities observed in the material. In addition, because a compound semiconductor is being grown on an elemental material, defects known as antiphase domains may also occur, unless specific precautions are taken to prevent their formation.

Only a few years ago, breakthroughs in crystal growth permitted high-quality GaAs to be grown on Si for the first time. Since then, much research has been devoted to GaAs and Si integration. Many device structures have already been fabricated, and more work is currently being done to improve existing devices and to fabricate more advanced ones. Unfortunately, progress on the more difficult devices, particularly lasers, has been hampered by structural problems with the GaAs. Part of the problem is that much device research has been done at the expense of materials research; when problems with the GaAs became apparent, little materials science knowledge was available for their solution. The goal of this dissertation is to contribute to the understanding of GaAs/Si epitaxy, both for technological reasons (the improvement of the material for device applications) and scientific ones (a better understanding of heteroepitaxy in general). In particular, the emphasis of this work is on the correlation of substrate structure, nucleation processes and thick film growth. All of the films were grown by molecular beam epitaxy (MBE) and analyzed by a number of characterization methods, including transmission electron microscopy (TEM), Rutherford backscattering spectrometry (RBS), and reflection high energy electron diffraction (RHEED).
1.2 Heteroepitaxy

This section consists of a brief overview of several aspects of crystal growth which are fundamental to understanding the GaAs/Si research we have done. Since this is a brief summary of a very broad field, the reader is referred to the pair of books on epitaxial growth edited by Matthews [2] for further information on this topic.

Crystal growth is a means of creating an ordered structure from a disordered one. Atoms from a disordered phase (vapor, liquid or solid) successively bond to a crystalline substrate, which serves as a template for the growth, to produce a new crystalline material. When the deposited material is single crystal with a definite orientation relationship with respect to the substrate, the growth is termed *epitaxy*, from the Greek roots *epi* ("upon") and *taxis* ("order, arrangement").

There are a number of conditions necessary for epitaxy to occur [3]. One is that the impinging atoms need enough kinetic energy, typically provided by heating the substrate, to be able to diffuse on the substrate surface until a correct lattice position is found; if not, amorphous or polycrystalline material will form instead. Another requirement is that the epitaxial material and substrate must have sets of lattice planes which can line up nearly exactly with one another.

Epitaxy can be divided into two categories: homoepitaxy, in which the epilayer and substrate are composed of the same material, and heteroepitaxy, in which the composition and sometimes the crystal structure of the two materials are different. An example of homoepitaxy is the growth of GaAs on GaAs substrates; device structures are commonly produced in situ in this manner by changing the doping of successive GaAs layers. Heteroepitaxy is usually done when the goal is to use both materials for a particular application, or when the substrate offers advantages in cost, availability and strength; all of these apply for GaAs/Si growth. There are a number of problems, however, that often arise in heteroepitaxial growth.
Fig. 1-1. a) Commensurate growth, b) incommensurate growth.

One such difficulty is defect generation. There is often a difference in the lattice plane spacing between the epilayer and substrate; this misfit is defined as $100(b-a)/a$, where $a$ and $b$ are the lattice constants of the substrate and overgrowth, respectively. The lattice constant is $5.654\text{Å}$ in GaAs and $5.431\text{Å}$ in Si, so there is a $4.1\%$ lattice mismatch between the two materials at room temperature. Because of lattice mismatch, stresses develop in the growing film, leading to the nucleation of such defects as misfit dislocations, which serve to accommodate the misfit. In cases where the misfit is too great, epitaxy is not possible at all.

Misfit dislocations generally do not form immediately at the beginning of growth. Generally, a growing film will first be strained so that its lattice planes normal to the surface line up with those of the substrate; this is termed commensurate growth. For cubic materials, this causes a tetragonal distortion of the material, the extent of which is determined from Poisson's ratio. As the growth proceeds and the volume of the film increases, the strain energy in the film increases to the point where dislocation formation becomes energetically favorable, and dislocations are then nucleated; this is termed incommensurate growth. These two situations are shown schematically in Fig. 1-1. The
Fig. 1-2. The three growth modes: a) planar (Frank-van der Merwe); b) Stranski-Krastanov; c) Volmer-Weber.

thickness beyond which incommensurate growth occurs is known as the critical thickness and has been theoretically predicted for the deposition of uniform layers [4,5]. However, as will be discussed in Ch. 4, this analysis is altered when nonplanar film growth occurs.

Another consequence of heteroepitaxy is that the film structure is often affected by the substrate material used. In contrast to homoepitaxy, uniform film deposition does not occur in most cases of heteroepitaxy. More commonly, clusters form, either directly on the substrate (Volmer-Weber growth) or on a thin layer of the grown material (Stranski-Krastanov growth). These three basic types of growth structures are illustrated in Fig.1-2.

There are a number of reasons why a particular growth mode is energetically preferred for a given heteroepitaxial system. Quantitative analysis by Venables and Price [6] predicts that the growth mode depends on the ratio of the binding energy of atoms within the epilayer to the adsorption energy of epilayer atoms on the substrate. More recently, molecular dynamics computer simulations by Grabow and Gilmer [7] indicate that misfit and epilayer-substrate interactions determine the equilibrium form of the epilayer; their results are summarized as follows. Planar, or Frank-van der Merwe, growth is expected only when there is a strong epilayer-substrate interaction. Even if there is such an
interaction, it will not influence the growth after several layers are deposited. If there is lattice mismatch, clustering will then occur on top of this thin epilayer, leading to Straski-Kraotonov growth. This is because the strain energy due to misfit can be reduced by forming three dimensional clusters, which are closer in energy to bulk material. In addition, the surface energy is minimized because of the low surface to volume ratio. When there is little or no epilayer-substrate interaction, as in the case of Volmer-Weber growth, islanding occurs immediately at the onset of growth. Although these considerations determine the equilibrium configuration of the films, kinetics determines the form that actually occurs. At low temperatures, for instance, a metastable state rather than an equilibrium state may grow instead.

A problem specific to the growth of compounds on elemental materials is antiphase domain (APD) formation. For GaAs/Si epitaxy, the problem lies in the fact that both the diamond cubic (Si) and zincblende (GaAs) structures are composed of two interpenetrating FCC sublattices. The (100) plane is primitive; i.e., it consists of atoms in only one of the two FCC sublattices. A real (100) surface contains steps, and if these steps are an odd number of atomic layers high, atoms in both sublattices will be on the surface. This presents a problem when GaAs is grown on such a Si surface. Bringans et al. [8] showed that As has a strong affinity for a Si(100) surface. This finding, coupled with the fact that the Si preheat and cool-down occurs under a high As background pressure, leads to the conclusion that GaAs growth on Si usually starts with As-Si bonds. Therefore, GaAs nucleated at opposite sides of a step that is an odd number of atomic layers high will grow together to form an antiphase boundary, as shown in Fig. 1-3. Depending on the plane in which the APB exists, the boundary may be electrically neutral (equal numbers of Ga-Ga and As-As bonds) or charged (having more or one type of bond than another). While there have been no conclusive studies directly linking APDs to poor device performance, it is quite likely that they affect electrical and optical characteristics, particularly if the defects are electrically charged. For the (100) orientation, this problem can be avoided if all the steps
Fig. 1-3. Antiphase domains in GaAs/Si due to single atomic layer steps on the Si surface.

are an even number of atomic layers high and the nucleating species is of a single type (i.e. As).

1.3 Summary of GaAs/Si research to date

The interest in using Si as a substrate for GaAs solar cells stimulated the first GaAs/Si work [9-13]. Solar cells require large device areas, and Si substrates are larger, less expensive, stronger, and lighter than GaAs substrates, features particularly important for space applications. The prevailing view at the time, however, was that it is impossible to grow good GaAs directly on Si because of the large lattice mismatch and thermal expansion coefficient difference [11, 14]; the poor results of the few attempted GaAs/Si growths were seen as confirmations of these predictions [12, 14]. Instead, researchers resorted to using Ge as an interlayer between the GaAs and Si, because GaAs and Ge have similar lattice constants and thermal expansion coefficients. Other work showed that
excessive autodoping from the Ge substrate deteriorated device performance [12], so the
growth of GaAs directly on Si remained a desirable but unattainable goal.

High-quality GaAs/Si can now be grown despite the lattice and thermal expansion
coefficient mismatches. In hindsight, one can attribute the failure of the early growths to
other causes. One likely factor is the difficulty in obtaining clean Si surfaces. It is
necessary to remove surface oxides and residual carbon contamination on the Si prior to the
growth: the native oxides on silicon are amorphous and act as a barrier for epitaxy on Si,
and carbon contamination on the Si surface creates unwanted nucleation sites for the
epitaxy. Unfortunately, the inherent stability of the oxides and the extremely strong bond
between C and a clean Si surface [15] makes these species difficult to remove unless very
severe heat or chemical treatments are used. RCA and other earlier common chemical
cleans used prior to MBE growth form an oxide that can be desorbed in UHV between
800°C-900°C; however, they require a brief flash cleaning at approximately 1150°C to
remove the residual C [16,17]. This high temperature is impossible to achieve in
conventional III-V MBE systems. Thus, early attempts to grow GaAs/Si were hampered by
poorly cleaned surfaces. As in the early vapor phase GaP/Si work [18], poor surface
cleanliness, particularly incomplete oxide removal, may have been a problem for GaAs/Si
MOCVD growth as well. The fact that Ge/Si growth was successfully accomplished is
probably due to the relative ease with which Ge [19] recrystallizes in solid phase epitaxy
compared to GaAs [20]. Growth on oxides and use of less than optimal growth
procedures were the most likely causes of the rough surface morphology and the
polycrystallinity of these early films [12, 14].

Several years after these initial attempts, new applications, particularly
optoelectronic integrated circuits and monolithic integration of ultra-high speed GaAs with
high density Si VLSI, led to renewed GaAs/Si growth efforts. Because of several
breakthroughs in crystal growth and wafer preparation, high-quality GaAs was grown
directly on Si for the first time in 1984 [21]. This achievement greatly surprised and
encouraged the research community, which had previously thought that good GaAs/Si growth was impossible.

Three developments in particular were responsible for this success. The first was the development of relatively convenient, low temperature Si cleaning techniques. In one method, the substrate is heated above 800°C and exposed to a Ga beam; this reduces the SiO_2 to Ga_2O, which is volatile at 600°C [22]. This technique removes the oxide but still leaves small amounts of carbon on the surface. Ishizaka et al. [23,24] developed another cleaning procedure which is now the most commonly used technique for GaAs/Si growth. The process consists of sequential forming and etching of a thin oxide layer on the Si. The last step of the procedure is designed to form a non-stoichiometric oxide which desorbs below 800°C. Most importantly, the surface is free of C after the oxide desorbs. DLTS and SIMS measurements by Xie et al. suggest that there is still a small amount of residual C left on the surface [25-27] after this cleaning procedure. However, this method is a substantial improvement over earlier techniques.

The second factor contributing to the success of GaAs/Si was the separation of the nucleation and growth phases in a two-step growth process, first described by Wang [21]. This involves the growth of a buffer layer at a slow rate and low substrate temperature, followed by a device layer using conventional GaAs homoepitaxial conditions. As will be discussed in Ch. 4, our work shows that this process increases the nucleation density and therefore improves the surface morphology of the resulting GaAs films. Several workers have suggested that the growth is begun at low temperatures to ensure that a monolayer of As bonds to the Si in order to prevent APD formation. Urberg et al. [28], however, have found that As strongly bonds to Si and does not desorb unless the wafer is heated to 650°C or higher. In addition, photoemission work by their group [29] show that a layer of primarily As bonds to the Si even if a Ga layer is deposited before the GaAs is grown.

The third breakthrough was the suppression of antiphase domains by using substrates tilted off the exact (100) orientation. Although such vicinal substrates had been
used previously in other types of epitaxy [30], Masselink et al. were the first to employ them expressly for antiphase domain prevention in GaAs/Si [31]. The mechanisms for this defect suppression is still unclear, and will be discussed in Ch. 5.

In the past few years, nearly all types of GaAs and heterojunction devices have been fabricated directly on Si. All majority carrier devices (MESFETs, MODFETs, etc.) are comparable to homoepitaxial GaAs devices, while the performance of minority carrier devices (bipolar transistors, lasers, etc.) is inferior. In particular, room temperature laser operation has been achieved, but only with very short lifetimes [32]. Comparison with conventional GaAs lasers [33] suggests that the source of the problem is the combination of lattice and thermal expansion coefficient mismatches, because of the structural and electrically active defects they create in the GaAs layers. The reader is referred to several reviews of GaAs/Si devices [34-36] for further details. While significant progress in GaAs/Si technology has been made, it is clear that further understanding of the growth and defect generation is necessary for the realization of such important goals as optoelectronic integrated circuits.

1.4 Dissertation outline

This thesis is organized in the following manner. Chapter 2 describes the various experimental techniques and procedures used to grow and analyze the GaAs/Si layers. The structure and strain in films of various thicknesses are discussed in Chapter 3. These findings are integrated to yield a description of the structural evolution of GaAs/Si films from the very beginning of growth to the completion of thick films. The remainder of the thesis focuses on several specific aspects of GaAs nucleation on Si. In Chapter 4, nucleation processes are investigated and correlated with the structure of thicker films.
Chapter 5 examines the role of substrate surface steps in GaAs/Si growth. Finally, conclusions and suggestions for future work are presented in Chapter 6.
CHAPTER 2

EXPERIMENTAL TECHNIQUES AND PROCEDURES

This chapter describes the MBE growth procedure used to prepare the films in this research, and the analysis methods used to characterize them. Background information and the specific procedures used for each of the techniques is given. At the risk of oversimplification, the purpose of this chapter is to provide enough information for the basic understanding of the methods and data discussed in this thesis.

2.1 MBE and MOCVD

MBE and metal-organic chemical vapor deposition (MOCVD) are the two methods currently used to grow GaAs/Si. MOCVD falls into the broader category of vapor phase epitaxy (VPE), the method in which streams of gases flow over the substrate and react to form the growing film. The gases in VPE are typically small amounts of hydrides or halides in a flow of an inert gas such as hydrogen, which assists in the gas transport; in MOCVD, organometallic source gases are used instead. Chemical reactions occur among the gases on or near the substrate, and the reaction products are incorporated into the growing film. High substrate temperatures are often necessary to catalyze the reactions. The gas flow around the substrate creates a gas layer near the substrate surface that serves as a transition between the flowing gases and the static substrate surface. Across this stagnant layer or boundary layer, as it is called, there are temperature and concentration
gradients. The rate-limiting step in the growth is either the diffusion of gases through the boundary layer or the surface chemical reactions, depending on the substrate temperature.

Like VPE, MBE [37] employs gaseous source material, but the methods differ in a number of ways. Rather than a gas stream, a conventional MBE source is simply an elemental solid or liquid that is heated to produce a beam of vapor which is directed toward the substrate. This occurs in an ultra-high vacuum (UHV), the condition in which the background pressure is less than $10^{-8}$ torr. The mean free path of the species is long compared to the transit distances and thus all reactions occur on the substrate rather than in a boundary layer over the substrate. Shutters in front of the individual sources are opened and closed during the growth, permitting the growth of extremely abrupt junctions. Greater dimensional control is possible with MBE than VPE because the growth is slower (1μm/hr typically as opposed to several μm/hr for VPE) and there is no boundary layer near the substrate. VPE also typically involves higher substrate temperatures, which may be harmful to device structures already existing on the substrate. A particularly important advantage of MBE is that UHV surface analytical equipment can be used in the substrate preparation and growth chambers. This permits the study of substrate cleaning procedures and growth processes, which is particularly valuable for the growth of new materials.

There are several disadvantages of MBE, however. The molecular beams have a finite radius, so that they uniformly reach wafers at most 3" in diameter in current MBE systems. In contrast, larger wafers can be used in MOCVD. The latter technique also uses higher growth rates and less elaborate wafer loading procedures, so that higher throughputs are possible.

2.1.1 The MBE System

A typical MBE system consists of separate wafer loading, storage, and growth
chambers. A schematic diagram of the growth chamber of the MBE system in our laboratory, a Varian Gen II, is shown in Fig. 2-1. The growth chamber essentially consists of source material, a substrate holder and heater, analytical equipment, and pumps, surrounded by the stainless steel chamber walls. The material from which the epilayers are grown and doped is contained in eight Knudsen effusion cells, each containing one element. The effusion cells contain pyrolytic boron nitride (PBN) crucibles, which are separately heated by individual furnaces surrounding them. Each furnace is individually controlled and separated by baffles to minimize interactions between them. A thermocouple, used for temperature measurement and feedback, is positioned at the bottom of each crucible. Growth is accomplished by heating each source, creating a vapor pressure above the solid or liquid source. Because all the sources are pointed directly at the substrate, this gives rise to beams of atoms or molecules from each source which travel through the vacuum and impinge on the wafer. The flux of any given source is terminated
by shuttering off the opening in front of it. The shutters can be opened and closed in less than 0.5 sec, giving the grower precise control over individual monolayers grown.

The growth rate, composition, and doping concentration in a growing film are set by the fluxes from the appropriate effusion cells. The cell temperature necessary to produce the desired flux from an ideal effusion cell is determined from the equilibrium vapor pressure of the source material and the geometry of the MBE chamber. Because of the non-ideality of real effusion cells [38], accurate determination of the fluxes needs to be done experimentally. In the growth chamber, the pressure increase when a shutter is opened is measured by a "beam flux monitor", an ion gauge which is rotated into the substrate position during the flux measurements. For the growth of III-V semiconductors such as GaAs, the relative fluxes of the Group V and Group III species needs to be determined. Because ion gauges measure the density of the gas [39], the relative average velocities must be considered in determining the fluxes from these "beam equivalent pressures".

The gallium and arsenic used for GaAs growth are generated in the following ways. Monoatomic Ga evaporates from molten elemental Ga in the source crucible. The arsenic flux consists of either As$_4$ or As$_2$ molecules. As$_4$, used for the GaAs growths in this investigation, is produced by the sublimation of elemental arsenic. As$_2$ is the equilibrium species over GaAs and can be formed by either heating GaAs or by thermally cracking As$_4$.

Also shown in Fig. 2-1 is the analytical equipment in our growth chamber. The quadropole mass spectrometer is used to detect the gaseous species present in the chamber. The electron gun and phosphor screen are used in reflection high energy electron diffraction (RHEED), which is discussed below.

In our system, the substrate is wired to a molybdenum holder and mounted on a substrate heater. The heat is provided radiatively from resistively heated tungsten coils, and a thermocouple is positioned in close proximity to the back of the wafer. Accurate
substrate temperature measurement is difficult because the thermocouple measures the temperature of the cavity at the back of the wafer, which often differs substantially from the temperature of the front surface of the wafer; calibrations are done with infrared pyrometers, which are still not entirely accurate. The temperature variation across a 2" GaAs wafer is less than 6° [40]. In addition to being heated during growth, the substrate is also rotated to ensure uniform exposure to the incoming beam fluxes. This rotation reduces the growth rate variation across the wafer from 25% to roughly 2%.

In order to grow extremely high-quality single crystal material used for electronic devices, the MBE growth apparatus must meet stringent requirements. The material for electronic devices must be purer than 10 ppb. This means that the MBE system must be made with inert and ultrapure materials inside the chamber that can withstand high temperatures; refractory metals are most often used because they meet these criteria. In addition, special equipment is needed to rotate and translate parts in UHV, and to connect the electronics inside and outside the machine. The source material for the films must also be of the highest purity. These matters are discussed in considerable detail in Ref. 41, an excellent guide to UHV equipment in general.

Impurities are also controlled by maintaining a low background pressure in the growth chamber, particularly of the species H2O, CO, CO2, CH4, H2 and O2. A variety of pumps are used, each of which is designed to pump particular molecular species or work in a given background pressure. In our system, an ion pump, cryopump, and titanium sublimation pump are used in the growth chamber. Liquid nitrogen flows in the double walls surrounding the substrate and enclosing the chamber; this serves to cool the walls so that stray impurities in the chamber will adsorb to the walls rather than bouncing around until they hit the wafer; CO2 and H2O in particular are very effectively pumped in this manner. In addition, the system is heated ("baked") after each time the growth chamber is opened to replenish sources or to do repairs. This serves to desorb, or "outgas" impurities.
in the chamber, which are pumped during the bake until a low pressure is reached. After
the bake, pressures on the order of 10^{-11} torr are reached.

In order to repeatedly load wafers into the system without disturbing the ultra-high
vacuum in the growth chamber, MBE systems are partitioned into several chambers,
separated by gate valves. Our Varian Gen II MBE system actually consists of four
chambers: a loading chamber, transition tube, and two growth chambers. The loading
chamber is routinely opened to air and stores 11 wafers at once. Each wafer and holder is
heated to desorb excess moisture before being transferred to the transition tube. This
loading chamber is normally evacuated to 10^{-6} torr, so that when the valve between it and
the transition tube is opened, the transition tube is never exposed to pressures higher than
that. The transition tube, called that because it is used to transfer wafers to either of the two
growth chambers attached to it, stores up to 16 wafers. It is typically pumped to a pressure
of 10^{-9} torr. Whenever any of the chambers is opened to atmosphere, dry nitrogen is
pumped through it, maintaining a positive nitrogen pressure to minimize any contamination
from air entering the chamber.

2.1.2 MBE Growth

Before molecules impinging on the substrate surface become incorporated into the
growing film, several processes can occur, as shown in Fig. 2-2. Molecules with enough
kinetic energy diffuse on the surface and may undergo chemical reactions. Some of the
impinging atoms eventually re-evaporate from the substrate; the fraction of incident
molecules that adsorb is given by the "sticking coefficient". Some of the molecules are
incorporated into the growing film. These processes depend in part on the strength of
interaction between the adsorbate and the surface. Physisorption occurs when there is only
weak bonding, such as van der Waals interactions. In contrast, chemisorption takes place
when stronger bonds, such as covalent bonds, are formed.
Fig. 2-2. Interactions among impinging gas molecules and a solid substrate surface.

In his pioneering work on GaAs growth kinetics, Arthur [42] found that the growth rate is determined by the Ga flux and that arsenic adsorption and reactions are rate-limiting. A number of years later, Foxon and Joyce [43, 44] developed a detailed model for GaAs growth; the findings for (100) GaAs growth using As₄ are briefly summarized here. The sticking coefficient of Ga is unity for the temperatures typically used during growth [42, 45]. After Ga atoms chemisorb to the surface, pairs of As₄ molecules react on adjacent Ga atoms. For each As₄ pair, four atoms are incorporated into the growing crystal and the remaining four desorb as an As₄ molecule. The rate-limiting step and the As₄ sticking coefficient depend on the relative populations of arsenic and gallium on the surface, which are determined by the relative fluxes. For \( J_{Ga} \ll J_{As_4} \), the As₄ sticking coefficient is proportional to the Ga flux. There are many As₄ molecules on the surface available for reaction, so the rate-limiting step becomes the arrival of As₄ molecules, a first-order process. For \( J_{Ga} \leq J_{As_4} \), the sticking coefficient is independent of \( J_{Ga} \) and asymptotically approaches 0.5, which is the upper limit because of the As₄ reaction mechanism. In this case, the population of As₄ molecules on the surface is low, and the growth rate is limited by the encounter and reaction of pairs of As₄ molecules on adjacent
Ga atoms, a second-order process. Unless $J_{Ga} << J_{As4}$, however, excess Ga is incorporated into the growing film; for this reason, the growth is done with excess As$_4$ flux to ensure stoichiometric growth. With As$_2$, the process is simpler; the growth occurs by first order dissociative chemisorption of the As$_2$ on single Ga atoms [44].

One important consideration for GaAs growth is the desorption of arsenic and Ga when heating the (100) GaAs surface. Above 325°C, an As-rich surface will desorb up to 0.5 monolayers of arsenic as As$_2$, leaving behind a Ga-rich surface [46]. Above 575°C, dissociative evaporation of GaAs becomes significant [47]. The congruent sublimation temperature of GaAs, in which the fluxes are related by $J_{Ga} = 2J_{As2}$, is 625-635°C [46,48]. Between 575°C and the congruent sublimation temperature, the GaAs evaporation rates vary between 0.01 and 1.0 monolayers/sec, being controlled by the desorption rate of Ga, which in turn is determined by the equilibrium vapor pressure of Ga over GaAs [46]. Above the congruent sublimation temperature, As$_2$ is desorbed preferentially, leaving behind excess Ga that agglomerates to form droplets on the surface.

These events have important consequences for the choice of optimal parameters for growing high-quality GaAs with mirror-smooth surfaces. Provided that a very clean GaAs substrate is used, single crystal GaAs can be grown homoe epitaxially at temperatures as low as 92°C [49,50]. However, GaAs films grown at temperatures below roughly 480°C under normal conditions are of high resistivity [51,52] and have high concentrations of deep levels [53,54]. Higher growth temperatures are therefore needed to produce high quality films. On the other hand, the upper limit of the substrate temperature is determined by the As arrival rate which prevents non-congruent GaAs sublimation. This means that higher As fluxes are needed for higher temperature growth. Below 640°C, the growth rate is nearly independent of substrate temperature, implying that the sticking coefficient of Ga remains nearly unity [45]. The usual range for good GaAs MBE is between 550° to 630°C.

Optimal GaAs MBE growth also depends on the V/III flux ratio. The growth is done with an As-stabilized surface, the conditions for which depend on the V/III flux ratio,
substrate temperature and orientation. The growth is usually done with just enough As flux to maintain an As-stabilized surface, so that non-stoichiometric growth is avoided. Too high an As flux gives rise to high deep level concentrations [53,55], possibly associated with [As]Ga antisite defects.

2.2 Surface reconstructions and RHEED

Since the "quality" of the substrate surface greatly influences epilayer growth, the surface structure is very important for the growth. The position of atoms on the surface of materials is often quite different from the corresponding positions in the bulk. The reason is that the environment around surface atoms is considerably different from that deeper in the crystal: there are fewer atomic neighbors, and there may be dangling bonds created because of the missing atoms. As a result, the surface energy can often be lowered by the rearrangement of atoms on or near the surface. Often the distance between the first and second outermost atomic layers changes due to atomic relaxation. When this occurs, the unit cell of a given surface plane is still identical to that from the equivalent plane in the bulk. However, rearrangements can also include altered in-plane bond lengths and angles, and often new bonds among surface atoms are formed as well. In these cases the surface is said to reconstruct, and a different surface unit cell results. The reconstruction of crystal surfaces often changes considerably with temperature, adsorbate coverage, and, for alloys, with surface stoichiometry. An excellent discussion of surfaces and reconstructions can be found in the text by Somorjai [56].

The structures of reconstructed surfaces can be denoted in the following way when the angle between the lattice vectors on the surface is the same as in the bulk [57]. The general form is p(nxm)Rθ° or c(nxm)Rθ°, for primitive and centered unit cells, respectively. This indicates that the surface unit cell is nxm times larger than the bulk unit
cell for that plane. $\theta^\circ$ is the angle of rotation between the two unit cells. The "p" is often omitted as is the "$\theta^\circ" if there is no angle of rotation. As an example, a unit cell in the (2x1) reconstruction, common on Si (100) surfaces, is shown in Fig. 2-3.

On the unreconstructed (100) surface of both Si and As-terminated GaAs, there are dangling sp$^3$ bonds. As shown in Fig. 2-4, the orbitals on adjacent atoms tend to bond with one another to form surface dimers. The resulting surface reconstruction is 2x1 on the Si surface. The dimers on the GaAs surface can be arranged in different ways, leading to different reconstructions.

In the growth of GaAs (100), two principle surface reconstructions are observed, depending on the surface composition. During "As-stabilized" conditions, an As-rich (2x4) surface is seen, while the Ga-rich (4x2) surface appears during "Ga-stabilized" growth under typical homoepitaxial conditions. Other reconstructions, such as (3x1), (1x6), (4x6) and (3x6), are observed within very narrow ranges of growth conditions [59].

For MBE growth, these surface reconstructions are observed in situ with RHEED, an extremely useful tool for monitoring the structure of the wafer surface before and during growth. From the diffraction pattern, the presence or absence of the substrate oxide can be
Fig. 2-4. Schematic diagram of dimerization on an As-terminated GaAs surface (from Ref. 58).

determined, allowing one to determine the conditions necessary to desorb the oxide. Amorphous, polycrystalline, and single crystal films can be distinguished. RHEED is also used to monitor the changes in surface structure when the fluxes of the different molecular species are altered during growth [60]. In addition, by measuring the time-dependence of the diffraction intensity during growth, the growth rate can be accurately calibrated [61, 62].

RHEED is done by aiming the electron beam, typically 10 keV, at a glancing angle of 1-2° to the substrate. The electron beam is also normal to the source fluxes, so that RHEED can be done during the film growth. The electron penetration depth is only several atomic layers, so that the surface structure, rather than the bulk, gives rise to the diffraction pattern. The wavelength λ (in Ångstroms) corresponding to an accelerating voltage V (in volts) is given by
\[ \lambda = \sqrt{\frac{150}{V(1 + 10^{-6} V)}} \]

For 10keV electrons, the corresponding wavelength is 0.12Å.

The conditions for diffraction can be determined from the Ewald sphere construction for the reciprocal lattice. The reciprocal lattice in this case consists of a two-dimensional array of reciprocal lattice rods, which are elongated along the direction normal to the crystal surface. The intersection between the Ewald sphere and these reciprocal lattice rods gives rise to streaks of diffracted intensity. This is shown in Fig. 2-5 for a simple square surface lattice.

Fig. 2-5. Schematic diagram of the origin of RHEED streaks from a square reciprocal lattice (from Ref. 63).
Using Bragg's law, \(\lambda=2d\sin\theta\), and the diffraction geometry, the periodicity of the surface can be determined from the diffraction pattern by

\[
a = \frac{\lambda L}{t},
\]

where \(L\) is the distance between the surface and the screen, and \(t\) is the separation between the streaks. In contrast to transmission electron diffraction, in which a two-dimensional diffraction pattern is obtained, the RHEED pattern shows only one dimension in reciprocal space. The patterns from two azimuths are needed to determine the complete surface reconstruction.

For surfaces that are not reconstructions on single crystal films, other RHEED patterns are observed. When the surface is rough and the electron beam penetrates the asperities, diffuse spots, located at the intersection of the Ewald sphere with the bulk reciprocal lattice, are observed. Surface facetting gives rise to chevrons rather than spots. As in transmission electron diffraction, hazy patterns indicate amorphous material and rings indicate polycrystalline material.

2.3 Characterization Techniques

2.3.1 Transmission Electron Microscopy

In TEM [64], a beam of electrons impinges upon a thin (<1\(\mu\)m thick) sample and passes through it. In the process, many of the electrons undergo Bragg diffraction and are separated into different beams, each corresponding to the set of planes doing the diffracting. By manipulating these diffracted beams with the apertures and magnetic lenses in the microscope, one can choose which beams to use to form the image. The resulting
image gives information about the sets of planes involved in the diffraction. Films can be examined in plan-view or in cross-section, depending on whether the electron beam is perpendicular or parallel to the epitaxial interface, respectively.

TEM can be used to image lattice defects such as dislocations and stacking faults. These defects alter the positions of the lattice planes and therefore affect the electrons travelling through the material. The strained material near a dislocation core, for example, consists of curved planes that locally increase the number of diffraction events. If the image is formed from the electrons transmitted rather than diffracted in the sample, dislocations will appear dark compared to the surrounding areas. Conversely, in an image formed from a diffracted beam, these defects will appear bright and the background dark. Such diffraction contrast is also used to image other defects as well.

Under certain conditions, one can obtain extremely high resolution images which show the actual lattice of the sample. What appears as a single atom is actually the projection of an entire row of atoms through the thickness of the TEM specimen. For GaAs and Si, the two atoms at each lattice point cannot be resolved with high resolution TEM (HRTEM), so they appear as a single spot.

2.3.2 Rutherford Backscattering Spectrometry

In RBS [65], high-energy $^4$He ions impinge on the atoms in the sample, collide with them, and recoil from them. Information about the composition and structure of the sample is obtained from the positions and energies of the backscattered $^4$He ions. The incident ions and the atoms in the specimen can be approximated to be billiard balls undergoing elastic collisions. By measuring the energy of the $^4$He ions backscattered from the surface of the sample, one can determine the composition of the surface.
Because the lattice of a crystal is relatively open, not all of the ions are immediately backscattered. Other $^4$He ions travel through the sample, losing energy through inelastic interactions in the process. When these ions are eventually backscattered after travelling some distance through the sample, they have less kinetic energy than those ions backscattered from the surface atoms. A depth scale on the backscattering spectra is obtained by accounting for this energy loss. The thickness of the film can also be determined in this way.

Crystallographic information can also be obtained from this technique. This method can be easily visualized by viewing a molecular model of a crystal. Viewing down a low-index zone shows the crystal to consist of arrays of atomic channels. If one tilts the crystal to a random orientation away from a low-index zone axis, however, the atomic arrangement appears random, as if the material were amorphous.

In the scattering chamber, the sample is mounted on a goniometer which allows it to be tilted with respect to the incoming ion beam. When the sample is positioned such that the $^4$He ion beam is closely aligned with a low-index zone axis, the ions are backscattered in the following manner. A certain fraction of the ions are backscattered from the surface atoms, giving rise to a "surface peak" in the backscattering spectrum. The remaining ions in the beam tend to be steered to the center of the columns, where the probability of backscattering is the least, by Coulombic interactions with the sample. As a result, there is a sharp reduction in the backscattered yield from atoms immediately below the surface, giving rise to a minimum in the backscattering spectrum. The value of this minimum, normalized to the value from a spectrum obtained from a random orientation, is given by $\chi_{\text{min}}$, the "minimum aligned yield". The value of $\chi_{\text{min}}$ is used to assess the crystalline quality of a material. Under the backscattering conditions used for our work, the $\chi_{\text{min}}$ for a perfect GaAs crystal is roughly 3%.

Not all of the ions continuing through the crystal reach the back of the sample, however. A significant fraction of the beam is "dechanneled" due to collisions with defects.
Fig. 2-6. Sample RBS spectrum from a 3000 Å GaAs film grown at 575°C (courtesy S J. Rosner).

and atoms displaced by thermal vibrations. These dechanneled ions have a much higher probability of being backscattered than the channeled ions. As a result, more and more ions are backscattered as they progress deeper into the crystal. Correspondingly, the measured backscattered yield increases with depth. The slope of the spectrum, therefore, is an indication of the defect density in the sample.

The backscattering yield as a function of depth (channel number) from a GaAs film is shown in Fig. 2-6. The right edge is due to backscattering from the sample surface and the left edge corresponds to the GaAs/Si interface. Because Ga and As atoms have different masses, backscattering from the GaAs surface actually gives rise to two edges slightly displaced from one another; due to limits in resolution, they are superposed in this spectrum. Lower channel numbers represent less energetic particles which have been backscattered from increasing depth into the sample.
2.4 Experimental Procedures

The majority of the substrates employed in this investigation were 2 inch, p-type (boron-doped) Si wafers having resistivity >10 $\Omega$-cm. A number of different wafer orientations were used, each with surface normal oriented several degrees from the [100] surface normal, as determined by x-ray diffraction.

The wafer cleaning procedure utilized is the method developed by Ishizaka et al. [23,24]. (Following the general practice of GaAs/Si growers, this cleaning method will be referred to as the "Shiraki clean"). The first step is the degrease: 10 minutes each in boiling trichloroethane, acetone, and boiling methanol, followed by a 5 minute rinse in deionized water. The wafers are then subjected to two cycles of oxidation and oxide removal in boiling HNO$_3$ for 7 minutes and a 40:1 buffered HF solution for 30 seconds, respectively. Next, the wafers are boiled in NH$_4$OH:H$_2$O$_2$:H$_2$O [1:1:3] solution for 7 minutes and again dipped in the HF solution for 30 seconds. Finally, the wafers are boiled in an HCl:H$_2$O$_2$:H$_2$O [3:1:1] solution for 7 minutes to form a thin, volatile surface oxide. The wafers are rinsed in deionized water for 5 minutes after the degrease and after exposure to each etchant. Following the last rinse, the wafers are spun dry and immediately loaded into the loading chamber of the MBE machine. After the pressure is pumped down to 10$^{-6}$ torr, the wafers are heated in the load chamber to remove any excess moisture (typically 40 minutes at 400°C). Immediately before the growth, the surface oxide is thermally desorbed in the growth chamber at 880°C for 10 minutes with an As$_4$ ambient of 10$^{-7}$ torr.

The basic growth procedure described below is typical of GaAs/Si MBE growth presently done by various laboratories; all of the samples for this investigation were grown using variations (each of which is noted in the discussion of the particular samples) on the following procedure. After the oxide is desorbed, the wafer is cooled to the growth
temperature. The wafer is then exposed to an \( \text{As}_4 \) flux of \( 10^{-5} \) torr in order to ensure that a monolayer of As completely covers the Si. The actual growth procedure involves two stages: a 100 nm "buffer layer", grown at 0.4 \( \mu \text{m/hr} \) at a low temperature (typically 405°C), followed by an "overlayer" growth using conventional homoepitaxial conditions (1.0 \( \mu \text{m/hr} \), 575°C and with an \( \text{As}_4/\text{Ga} \) ratio of 3.3). Unless otherwise noted, the growth is terminated by shuttering the Ga beam after the buffer is grown and resumed only after the wafer temperature reached 575°C; the arsenic flux is maintained during this transition stage and also during the post-growth cooling to maintain an As-stabilized surface.

TEM characterization of the films was done using several different microscopes. The majority of the plan-view images were obtained with a JEOL 200CX high resolution microscope, operating at 200 kV with point-to-point resolution of 2.5 Å, located at Hewlett-Packard. High-resolution cross-sectional microscopy was done using the Atomic Resolution Microscope (ARM) at Lawrence Berkeley Laboratories, operating at 800 kV with a point-to-point resolution of 1.6 Å, and the JEOL 2000FX at AT&T Bell Laboratories, operating at 200 kV with a point-to-point resolution of <3 Å. Specimens were prepared for cross-sectional microscopy by gluing strips of the material face-to-face using an epoxy; the entire structure was then mechanically backside thinned and then ion milled to electron transparency. Plan-view samples were prepared by chemical etching in an acetic acid: hydrofluoric acid: nitric acid mixture, after mechanical thinning in some cases.

Ion channeling was done with 2 MeV \(^4\text{He}^+\) ions using a General Ionex Tandetron tandem accelerator. A Si barrier detector was used to detect the backscattered particles. The total flux for the measurements was 30 \( \mu \text{C} \).

A Cu K\( \alpha_{1} \) x-ray source was used for the double-crystal x-ray rocking curve measurements; due to instrumental broadening, the minimum resolution of the peaks is roughly 80 arc-sec.
CHAPTER 3

STRUCTURAL EVOLUTION OF GaAs/Si FILMS

The structure of GaAs/Si films changes considerably during the first micron of growth, particularly during the first few thousand Ångstroms. Not only does the morphology evolve, but the strain in the film and defect densities change dramatically as well. In addition, the material near the GaAs-Si interface continues to rearrange even after being covered by the GaAs overlayer. These developments have important consequences for the generation of defects and the structural quality of thick films. This chapter follows the structural development of the films from nucleation to completion.

3.1 RHEED Development

We used RHEED to monitor successive stages of the growth. The patterns obtained during a typical two-step growth sequence are shown in Fig. 3-1. After the oxide is desorbed and the wafer is cooled to the growth temperature, a sharp, streaked Si RHEED pattern is obtained. On substrates misoriented 3.7° off-axis toward an <011> direction, the reconstruction is 2x1, but a 2x2 pattern, presumably a mixture of 2x1 and 1x2 domains, is obtained on 1.2° misoriented substrates. This will be discussed in more detail in Ch. V. After GaAs growth is begun, a spotted pattern, indicative of three-dimensional growth, is formed immediately and persists for several hundred Ångstroms. This is shown in Fig. 3-1a for 300Å of growth at 405°C. Islanding was also found by RHEED to occur in films grown at temperatures as low as 250°C. After 1000Å is grown at 405°C, the unreconstructed streak pattern shown in Fig. 3-1b is obtained, resulting from island
Fig. 3-1. RHEED patterns of GaAs/Si films: (a) \(300\text{Å}\) grown at \(405^\circ\text{C}\); (b) \(1000\text{Å}\) grown at \(405^\circ\text{C}\); (c) \(1000\text{Å}\) grown at \(405^\circ\text{C}\) and heated to \(575^\circ\text{C}\); (d) \(1000\text{Å}\) grown at \(405^\circ\text{C} + 2\text{µm overgrowth at } 575^\circ\text{C}\).

coalescence and surface morphology smoothing. When the film is then heated to \(575^\circ\text{C}\) for the overlayer growth, the surface reconstructs to form a 2x4 structure, as it does during GaAs homoepitaxial growth using these conditions. A sharp 2x4 pattern persists throughout the subsequent overgrowth. The [0\(\overline{1}\)1] azimuth before and after the overgrowth are shown in Figs. 3-1c and d, respectively.

3.2 Evolution of film structure

The film crystallinity also evolves during the growth. Fig. 3-2 shows the ion channeling yields of films of different thicknesses; the films were grown at \(405^\circ\text{C}\) except for the \(3000\text{Å}\) film, in which the growth temperatures were \(405^\circ\text{C}\) for the \(1000\text{Å}\) buffer layer and \(575^\circ\text{C}\) for the \(2000\text{Å}\) overlayer. Under the backscattering conditions we utilize,
the aligned yield from a perfect GaAs crystal is roughly 3% of the random yield. As indicated in the figure, the position of the peak corresponding to the 50Å sample is displaced slightly because a different geometry was used in the measurement in order to enhance the depth resolution.

As shown in the figure, the aligned yield from the 50Å film is roughly 90% of the random yield. Although some amount of this yield is due to backscattering from the atomic layers at and just below the surface, the high aligned yield indicates that the islands are quite disordered. (An alternate explanation is that the islands are tilted with respect to one another relative to the (100) plane, but this can be ruled out by the results discussed in Section 3.3.) While comparison between the peaks of the 50 and 300Å films is difficult because of surface backscattering, the high backscattering yield from the 300Å film
indicates that the crystallinity of this film is also rather poor. The fact that the backscattering yield from the 1000Å film is lower than that from the 300Å film is meaningful, however, and is indicative of improved crystallinity with increased coverage. In the spectrum of the 3000Å film, the large peak at lower energy (channel number) corresponds to backscattering from the 1000Å buffer layer. It is interesting to note that the aligned yield from this buffer region is less than the aligned yield from the 1000Å film which is not covered by an overlayer. This can be explained in the following way. In general, as an ion beam penetrates deeper into a homogeneous sample, the fraction of the beam that is dechanneled increases from interaction with defects; the aligned yield, therefore, will increase with depth. The fact that we observe a yield reduction in the buffer layer despite further overgrowth indicates that the crystallinity of the buffer layer improves substantially during the overgrowth.

In order to determine if the improvement in buffer layer crystallinity is due to the overgrowth or only the high temperature exposure, a comparison was made among films grown at 405°C and then heated at 575°C with and without further growth at this temperature. The film with the overlayer was heated at 575°C for a total of 35 minutes, including the overgrowth. Fig. 3-3 shows a comparison by ion channeling of the time dependence of the atomic rearrangements occurring during the 575°C anneal. It is evident that the aligned yield of the 1000Å film decreases considerably after a 15 minute anneal and is further reduced after a total of 35 minutes at 575°C. This reordering of atoms and annealing of defects apparently occurs throughout the entire epilayer, since the high and low energy sides of the peaks are affected. The 1000Å film annealed for 35 min can be compared with the 1000Å buffer layer buried under the 2000Å overlayer. The fraction of the beam which is dechanneled in the buffer layer is identical in the two samples, indicating comparable defect densities in the buffer layer. Since both layers were exposed to the high temperature for the same amount of time, it is apparent that the high temperature rather than the overgrowth process contributes to the reordering.
The preceding ion channeling results show that there is considerable disorder in 1000Å buffer layers grown at 405°C. High concentrations of point defects, dislocations and other structural defects are presumably present. This is confirmed by Fig. 3-4a, a cross-sectional TEM image of one such buffer layer. The film clearly contains large numbers of dislocations as well as stacking faults and/or twins. The threading of dislocations to the surface is also apparent. These features are representative of the film in general. This high defect density is expected from the 4.1% lattice mismatch between GaAs and Si; if all the mismatch were accommodated by a network of misfit dislocations with Burger's vectors parallel to the interface, the dislocation density would be roughly $10^{12}$/cm².
Fig. 3-4. Cross-sectional TEM images of GaAs/Si films: (a) 1000Å buffer layer grown at 405°C; (b) the structure in (a) covered by 2000Å overgrowth at 575°C.
Fortunately, the very dense dislocation network is confined to roughly the first 1000Å, as shown in Fig. 3-4b, the image of a film with a buffer layer grown at 405°C and a conventionally grown 2000Å overlayer. This change in defect density in the vicinity of the buffer layer-overlayer junction is consistent with the ion channeling finding of a sudden improvement in crystallinity in this region, as discussed below.

High resolution TEM images of the GaAs/Si interface show that it is quite disordered in addition to being punctuated by defects. Fig. 3-5 shows the GaAs/Si interfacial morphology of a film consisting of a 1000Å buffer layer grown at 405°C and a 2000Å overlayer grown at 575°C; the electron beam is incident in the <0.2° misoriented direction, such that the interface in the image is along the 3.7° misoriented <011> direction.

Fig. 3-5. High-resolution TEM image of the GaAs/Si interface for a film consisting of a 1000Å buffer layer grown at 405°C covered by 2000Å overgrowth at 575°C.
direction. Although the interface appears rather diffuse due to the projection of the steps along the beam direction, it is apparent that the interface is atomically rough, with a variety of step heights and terrace lengths occurring. Using the high angle tilting capability of the ARM, we imaged the same region of the interface along the perpendicular, non-misoriented \(<011>\) direction in the plane of the film; the interface along this direction is also quite rough. The interfacial structure is quite different from the regular array of \((200)\) steps which has been predicted [66,67], and also different from the flat terraces and step bands we have observed on very thin films, as will be discussed in Ch. 5. This roughness has also been seen by Heral et al. [68], who used a Si cleaning procedure quite different from the Shiraki method. Rather than a result of an uneven Si surface prior to growth, the interfacial roughness most likely is due to interdiffusion which occurs during the high temperature overlayer growth.

3.3 Strain relaxation

The changes in structural quality, particularly defect density, suggest that the strain in the film is also evolving as the growth proceeds. This section details the strain development as measured by ion channeling angular scans. This technique involves rocking the sample over a small angular range and measuring the backscattering yield as a function of angle. When the incident ion beam is most closely aligned with a given zone axis, there is a minimum in the backscattered yield. The angle between the minimums in the epilayer and substrate scans shows the relative positions of the zone axes in the two materials. If the epilayer is randomly oriented with respect to the substrate, zone axes normal and non-normal to the surface will be offset in angle with respect to the substrate. Our films, however, were found to be well-oriented from the scan using the \(<001>\) zone...
axis normal to the surface. Since random orientations of the GaAs can be ruled out, deviations between the positions of non-normal zone axes in the GaAs and Si are therefore indicative of strain in the plane of the film, which affects the non-normal but not the normal zone axes. The geometry of the measurement is shown schematically in Fig. 3-6. If GaAs planes normal to the surface are compressed, non-normal zone axes will be closer to the surface normal; in tension, the reverse is true. If there are a range of strains in the plane of the film, the curve will be broadened because the zone axes occur in a variety of positions.

![Diagram showing ion channeling scans](image)

**Fig. 3-6.** Geometry for angular ion channeling scans using non-normal zone axes.

Quantification of the strain from the data in the angular scans was done by Rosner [69]; for completeness, his procedure is reproduced here. Assuming negligible warpage of the substrate, one can model the film to be under biaxial stress in the plane of the film resulting in an isotropic planar strain $\varepsilon_p$. As the surface of the film is traction-free, there can be no stress in the direction of the surface normal. Solution of the matrix equation for the normal strain, $\varepsilon_n$, as a function of the elastic coefficients yields the relation
\[ e_n = -2C_{12}/(C_{11}+C_{12}) \cdot e_p. \]

The tetragonal distortion can be related to the angular misorientation by a simple geometric calculation, yielding

\[ e_p - e_n = \Delta \theta/\cos \theta \sin \theta, \]

where $\theta$ is the angle between the off-normal zone axis and the surface normal and $\Delta \theta$ is the misorientation between the GaAs and the Si obtained from the angular scan data. The planar strain is then given by

\[ e_p = 0.616 \cdot \Delta \theta/\cos \theta \sin \theta. \]

Two examples of angular scans appear in Fig. 3-7, which shows the results for films 300Å and 1000Å thick taken using <112> zone axes. Both films were grown at 405°C, but the thicker film was also annealed for 35 minutes at 575°C in situ. The zero angle corresponds roughly to the Si <112> zone axis with positive angle towards the surface normal. Comparison between the GaAs and Si minima positions shows that the thinner GaAs is strained in compression, while the thicker film is strained in tension. In addition, the angular width at half minimum for the GaAs is larger for the thinner film. This means that there are local variations in the strain in this film.
Fig. 3-7. MeV ion channeling angular scan profiles taken of <112> zone axes with projections into the surface perpendicular to the surface steps induced by the substrate misorientation. The films are (a) 300Å grown at 405°C, (b) 1000Å grown at 405°C with a 35 min, 575°C in situ anneal. The zero angle corresponds approximately to the Si <112> zone axis with positive angle towards the surface normal.

A summary of the evolution of the strain in the films at various stages of the growth is shown in Fig. 3-8. The measurements were done using pairs of non-normal zone axes of identical crystallographic type, such that the surface projection of each zone axis was either perpendicular or parallel to the direction of the Si surface steps induced by the substrate tilt. This serves to account for asymmetries in the strain caused by surface steps, as discussed in Ch. 5. The results in Fig. 3-8 show the average strain through the entire film, except for the 3000Å film, in which the yield is from the 1000Å buffer layer near the interface. A totally commensurate film would exhibit a planar compressive strain of approximately 4.1%, equal to the lattice mismatch between the GaAs and Si. Due to the difference in thermal coefficients of expansion, a completely relaxed film cooled from 405°C would be strained in tension 0.16%. The largest compressive strain determined for a 50Å film
grown at 405°C was only 1.5%, indicating that much of the mismatch has already been accommodated by misfit dislocations, even at this very early stage of growth. After 1000Å is grown at that temperature, the compressive strain is further reduced to 0.08%.

The effect of annealing at 575°C was studied by examining 1000Å films grown at 405°C and then heated to 575°C, in one case with no growth and, in the other, with 2000Å of overgrowth. After the higher temperature exposure, all the films examined were found to exhibit tensile strain equal to that expected from cooling a relaxed film from the growth temperature. Apparently, substantial atomic rearrangement occurs during the anneal,
resulting in the formation of networks of misfit dislocations that accommodate the lattice mismatch. In addition, the angular scan data shows that the strain in the thinner films is inhomogeneous in the plane of the film. As these films consist of islands, the inhomogeneity is most likely due to variations in the lattice spacing of different islands. This explanation is supported by the following observations. TEM images of the films show that the island size varies in a given film. Hull and Fischer-Colbrie have shown that the lateral dimensions of the islands in addition to the height determine the onset of misfit dislocation formation [70]. This means that different sized islands in the film are relaxed by different amounts. In contrast, there was negligible variation in the amount of lateral strain in a continuous film 1000Å thick, also grown at 405°C and annealed at 575°C.

These data show that the consequences of the two-step growth scheme on the properties of the films are due, in part, to the buffer layer anneal. The growth procedure we follow involves an abrupt transition between the two growth stages. After the buffer layer growth, the film is heated for 15 minutes at 575°C in order to wait for the Ga cell and substrate temperatures to stabilize for the overgrowth. During this time, the film relaxes, presumably by misfit dislocation formation. This means that further growth takes place on material that is substantially relaxed, so fewer new misfit dislocations are needed to form in the overlayer than would be necessary if the material had not been annealed. There should also be a significant change in defect density in the vicinity of the buffer layer-overlayer junction, which is confirmed by the TEM image in Fig. 3-4b. This suggests that the optimum two-step procedure would be to anneal the buffer layer until the lattice is completely relaxed before growing the overlayer, so that the dislocations would be confined to the buffer layer rather than thread up to the wafer surface. Subsequent work by Lee et al. [71] has shown reductions in the defect density by various high temperature exposures during and after the growth.
TABLE 3-1. Summary of thick film characterization results.

<table>
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<tr>
<th>ID</th>
<th>Tilt (011),deg</th>
<th>Buffer Layer T, Thickness, Thickness, X_min,</th>
<th>RBS %</th>
<th>X-Ray FWHM, arc-sec</th>
<th>Comments</th>
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<td>4.41</td>
<td>450</td>
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<td>470</td>
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<td>3.98</td>
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<td>1160</td>
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<tr>
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<td>2140</td>
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</tr>
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<td>350</td>
</tr>
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<td>2.0</td>
<td>3.72</td>
<td>350</td>
</tr>
</tbody>
</table>

Fig. 3-9. Plan view TEM image of dislocations in Sample #122, a 2.15\(\mu\)m GaAs/Si film.
3.4 Thick layer results

While the emphasis of this work was on nucleation and the initial stages of growth, a number of thick layers were grown as well. The purpose of the thick layer study was primarily to compare our layers with those grown by other groups, to ensure that our nucleation studies were relevant to work done elsewhere.

Table 3-1 summarizes the characterization results of a number of different films that were grown. The x-ray data are the FWHM of a (400) diffracted peak, as discussed in Ch. 2. All the wafers were grown using the two-step growth scheme except for samples #508 and #509; these two samples were grown without interruption by gradually increasing the buffer layer growth temperature and growth rate after the buffer layer was grown until the final overlayer parameters were reached.

The low values of $\chi_{\text{min}}$ indicate that the crystalline quality of the films is excellent, particularly in samples #508 and #509. Rosner [69] characterized films grown by two industrial groups; the results show that our films are indeed comparable with high-quality films grown for device purposes by other groups. Typical values of $\chi_{\text{min}}$ for 2 $\mu$m MBE films grown at Hewlett-Packard are 3.71 and 3.91; the $\chi_{\text{min}}$ is further improved to the range of 3.29-3.78 when a mid-growth anneal or a rapid thermal anneal is done on the samples. MOCVD films grown by Kopin Corporation of thicknesses ranging from 2.1-2.4 $\mu$m have $\chi_{\text{min}}$ values of 3.6-4.5 [69].

Our x-ray FWHM values are also comparable to those of the Hewlett-Packard and Kopin films [69]. The values for the 2 $\mu$m HP MBE films are 330 and 450 arc-secs. For the MOCVD films grown by Kopin, the FWHM values are 450 arc-secs for a 2.2 $\mu$m film and 300 arc-secs for a 2.4 $\mu$m film.

The surface morphology of our films is quite good as well; the films are shiny with a trace of cloudiness. A TEM image of one of our films, #122, is shown in Fig. 3-9. The dislocation density in this 2.15 $\mu$m film is approximately $2 \times 10^9$/cm$^2$. Films with
Fig. 3-10. RBS $\chi_{\text{min}}$ of several samples as a function of thickness.

Fig. 3-11. X-ray FWHM for several samples as a function of thickness.
dislocation densities as low as roughly $10^7$/cm$^2$ have been obtained by other groups by employing the procedures discussed below.

Another important factor for device applications is the minimum thickness necessary to grow high-quality material. The results of this chapter show that the quality of films of thicknesses up to 300Å is still rather poor. At this stage, the material is still far from suitable for the fabrication of any devices. Fortunately, the material greatly improves with further overlayer growth. Figs. 3-10 and 3-11, respectively, show the ion channeling minimum yield and x-ray results for the films as a function of thickness. While there is some variation in the growth procedure among these samples, the trend of improvement with thickness is clear. It is for this reason that thicker GaAs layers, typically 2-3 μm, need to be grown before devices can be fabricated using the material.

3.5 Discussion

Current device-related GaAs/Si materials research is focussed primarily on two areas: threading dislocation density reduction, and problems encountered when GaAs and Si devices are integrated on the same chip. Dislocations and strain in the epilayers is generally thought to be responsible for the low lifetimes reported for GaAs/Si lasers [33]. Ideally, a network of dislocations at the GaAs/Si interface is all that is required to accommodate the lattice mismatch. The problem lies in the formation of dislocations with Burger's vectors that are not parallel to the interface, and the tendency for the dislocations to propagate up through the epilayer up to the active device region.

Agreement on adequate techniques for counting dislocations has been a source of considerable controversy among GaAs/Si growers [33]. Plan view TEM is now considered the only accurate technique for this purpose. The general consensus is that the lowest reliable defect counts are in the $10^7$/cm$^2$ range. However, dislocation densities on
the order of $10^5$/cm$^2$ are needed for many GaAs/Si devices. Our results suggest that dislocation propagation can be controlled somewhat by annealing after the buffer layer growth. However, the work of Lee et al. [71] shows that various temperature treatments have only limited effect. Another technique employed is to grow strained-layer superlattices (SLSs) in the epilayer; the strain at the interfaces created by this structure serves to bend dislocations at the interface before they can thread up into the growing film. As with annealing, SLSs can reduce the dislocation density by one to two orders of magnitude from $10^9$/cm$^2$ but not to the extent needed. Clearly, new developments are necessary in order to achieve this goal.

Our results also show the significant improvement of crystallinity and defect density with thickness up to 2μm. Other studies of MBE films as thick as 3μm indicate that the material continues to improve with thickness up to 3μm [69]. Recent work on MOCVD films [72] shows that films 4μm thick have deep level densities, backscattering yields, and implant activation efficiencies comparable to bulk and homoepitaxial GaAs. There are, however, drawbacks in using films as thick as 4 microns. Wafer bowing and cracking commonly occur in thick films [73,74]. In addition, integration of thick GaAs device layers with Si devices on the same wafer creates high steps between the two materials; this makes the wafer difficult to process, as metallization and photolithography require relatively flat wafers. These problems can be solved by growing the GaAs in small wells etched into the Si surface. Groups at Stanford University [75] and Texas Instruments [76] are now working on this type of growth.
CHAPTER 4

GaAs ISLANDING AND THE
CONSEQUENCES FOR THICK FILM GROWTH

GaAs/Si growth was a formidable challenge to crystal growers in the 1970s, as discussed in Ch. 1. Successful growth was delayed for years until suitable procedures were developed for Si wafer cleaning and GaAs/Si nucleation. This demonstrates that the processes occurring at the onset of the epitaxy are critical to the growth of good material. The details of these early growth stages, and their subsequent effects on thick film growth, are the focus of this chapter.

For all types of epitaxy, several growth parameters need to be optimized in order to grow high-quality films. The substrate temperature, growth rate and the ratios of the incident beam fluxes are particularly critical parameters. For heteroepitaxy, there may be additional factors, such as lattice mismatch and antiphase domains, affecting the growth, so that the best procedure for growing a particular material may be considerably different from the one used in homoepitaxy. This is certainly true for the first step of GaAs/Si growth.

A less obvious, but nonetheless important, factor to consider is the growth mode of the epilayer; i.e., whether Volmer-Weber, Stranski-Krastanov or planar growth occurs. This chapter addresses the effects of GaAs island formation on the properties of thick films. We show that GaAs island formation can degrade the surface morphology of the films and may also be the source of some of the defects. In addition, we discuss the effects of the growth temperature, buffer layer thickness and other details of the growth procedure with regard to this nucleation mode.
Fig. 4-1. Nomarski photographs of 3000Å GaAs/Si films, where the 1000Å buffer layers were grown at: (a) 405°C, (b) 575°C.

4.1 Effect of buffer layer growth temperature on surface morphology

One of the most important developments for successful GaAs/Si growth was the two-step growth procedure, in which the buffer layer is grown at a low substrate temperature and growth rate. We have found that this procedure considerably improves the surface morphology. We examined the effect of the buffer layer growth temperature on a series of 3000Å films, each consisting of a 1000Å buffer layer and a 2000Å overlayer grown at 575°C. Visual inspection of the films shows that the morphology gradually degrades from a nearly mirror-like to very cloudy appearance as the buffer growth temperature is increased from 325°C to 575°C. Fig. 4-1 shows Nomarski photographs of two such films, in which the buffer layers were grown at 405°C and 575°C, respectively. It is apparent that the film grown entirely at the high temperature is the rougher of the two.

This degradation in surface morphology can be explained by the changes in island structure with temperature. Fig. 4-2 shows plan view images of 50Å films grown at 325°C and 405°C. The most obvious feature of these micrographs is the Moiré fringe contrast. The spatial period of the fringes represents the interference period between the (022) lattice
planar surfaces in the GaAs and the Si being used to form the image, the Moiré spacing being indicative of the mismatch between the Si and GaAs lattices in the thinned TEM sample. The regions of Moiré fringe contrast, therefore, show the GaAs islands on Si. The islands of the 325°C film are smaller and more numerous than those of the 405°C film, consistent with nucleation becoming more dominant over surface transport at the lower substrate temperature. In addition, the surface coverage of GaAs on the Si is lower in the higher temperature film, indicating that the aspect ratio (h/l) is greater for the islands in that film. The observed degradation of surface morphology with temperature can be explained by the increased surface mobility, which results in the nucleation of fewer, taller islands at the higher temperatures; this leads to rougher surfaces when the islands coalescence to form complete films. The dramatic improvement in surface morphology explains the success of the two-step growth procedure.
Another interesting feature to note in Fig. 4-2 is that the islands grown at 405°C are significantly elongated along one <022> direction relative to the orthogonal <022> direction. The islands grown at the lower temperature, however, are somewhat more rounded. This shape anisotropy will be shown in Ch. 5 to be due to nucleation and growth along Si surface steps which are intentionally created by the substrate misorientation.

4.2 Effect of buffer layer growth temperature on film crystallinity

We have shown that the use of a low buffer layer growth temperature improves the surface morphology. However, for epitaxial films in general, changes in the growth temperature significantly alters the epilayer crystallinity. Does the use of the two-step growth procedure degrade the crystalline quality of thick GaAs/Si films? To answer this question, we compared different buffer layer growth temperatures, using ion channeling, to examine the effect on the film crystallinity. Figs. 4-3a and b, respectively, show the aligned ion channeling spectra from two sets of samples: 1000Å buffer layers grown at different temperatures, and 1000Å layers grown at those same temperatures and then covered by a 2000Å overlayer grown at 575°C. From Fig. 4-3a, it is apparent that the aligned yield drops considerably with increasing growth temperature, indicative of significant improvements in the film quality. This finding reflects the fact that, at higher temperatures, the surface species have greater kinetic energy and therefore can diffuse longer distances on the surface in order to find correct lattice positions. In Fig. 4-3b, the important information comes from the slope of the spectra, which has the following significance. The signal level of the aligned spectra represents the fraction of the channeled ion beam that has been dechanneled by interaction with crystalline defects; thus, the slope of this curve is a measure of the dechanneling rate as a function of depth, which is directly
Fig. 4-3. Ion channeling spectra of films grown with different buffer layer temperatures. (a) 1000Å buffer layers; (b) buffer layers covered by 2000Å overlayer grown at 575°C.

proportional to the defect density. In the films grown with lower temperature buffer layers, there is an abrupt change in the slope of each spectrum at the position corresponding to the buffer/conventional layer interface. This implies a substantial change in defect density at this interface for a range of growth temperatures. Note also that there is no change when the buffer layer is grown at the same temperature as the conventional layer, confirming that this is predominantly a temperature effect as opposed to a growth rate or flux effect.
The information in Fig. 4-3 is summarized in Fig. 4-4, a plot of normalized ion channeling peak yield versus buffer layer growth temperature. Before the overgrowth, the crystallinity improves substantially with temperature. Upon subsequent heating at 575°C with overgrowth, however, the buffer layers reorder to roughly comparable levels. Most importantly, the surface aligned yields for all of the samples are in the range of 6.0 ± 1.0%. These data indicate that the crystallinity of the 2000Å overlayers, as determined by ion channeling, is independent of the initial growth temperature.

4.3 Buffer layer annealing and substrate coverage

Optimization of the buffer layer growth parameters is crucial for the growth of high-
quality thick films. One important consideration is the buffer layer thickness. Because the film quality is much better when it is grown at the higher temperature of the second growth step, buffer layers that are thin are preferable. We find that the nucleation of at least a certain thickness of low-temperature buffer layer is necessary, however, for good surface morphology. With this in mind, we examined island coalescence and the changes in the buffer layer that occur when the substrate temperature is raised to the overlayer growth temperature.

TEM images of films grown at 0.4μm/hr and 405°C show that the GaAs islands nucleate, grow, and coalesce, until an almost complete film is formed after 500Å of growth. Figs. 4-5a and 4-6a show plan-view TEM images of 30Å and 500Å films, respectively, on substrates misoriented 3.7° off-axis toward <011>. Irregularities in the Moiré fringes, due to defects and local strain variations in the films, are readily apparent.

The procedure we follow for thicker films involves growing a buffer layer, heating the wafer to 575°C, waiting 15 minutes for the Ga crucible and substrate temperatures to stabilize, and continuing the growth at 1 μm/hr at 575°C. Figs. 4-5b and 4-6b show the structural changes occurring in the buffer layer after the heat treatment before the second growth stage. From Fig. 4-5b, it is apparent that the islands have agglomerated, exposing more of the underlying substrate. Observations of various regions of the 500Å films, on the other hand, show that the heat treatment does not uncover more of the substrate. As Fig. 4-6b shows, the Moiré fringes become much more regular after the anneal, indicating a substantial improvement in film crystallinity. This correlates well with our ion channeling results which show a substantial decrease in the ion channeling yield when 1000Å buffer layers were heated to 575°C.

These results suggest that the optimal buffer layer thickness for our growth procedure is slightly thicker than 500Å, such that a complete film is formed. As discussed earlier in this chapter, we find that the surface morphology of thick films degrades due to the rough surface resulting from coalescing islands. Use of very thin, islanded buffer
Fig. 4-5. Plan view TEM images of a 30Å GaAs film on Si(100) tilted 4° toward <011>: (a) before and (b) after annealing in situ for 15 minutes at 575°C.

Fig. 4-6. Plan view TEM images of a 500Å GaAs film on Si(100) tilted 4° toward <011>: (a) before and (b) after annealing in situ for 15 minutes at 575°C. g = <220> parallel to the tilt axis.

layers will clearly lead to poor surface morphology, particularly because the anneal at 575°C further agglomerates the islands, leaving a more uneven film morphology.

The relationship between substrate coverage and film morphology can also explain why optimal MOCVD involves thinner buffer layers than MBE, typically 100-200Å [77,78]. Using TEM to observe MOCVD films grown by Kopin Corporation, Rosner [79] found that complete substrate coverage usually occurs before approximately 200Å is
grown, in contrast to MBE. In fact, for MOCVD, much thicker buffer layers result in poor overgrowth [77]. The reason is that the buffer layer is amorphous or polycrystalline, depending on the growth conditions, and it becomes difficult to recrystallize the layer if it is too thick. Apparently, the surface mobility of the reacting species is much lower in the case of MOCVD, so that single crystal GaAs formation is not accomplished.

4.4 Island coalescence

The threading dislocations which are such a problem for GaAs/Si devices are commonly attributed to the lattice mismatch and thermal expansion coefficient differences between GaAs and Si. We have evidence suggesting that island coalescence can also generate defects. Fig. 4-7 shows a plan view TEM image of a 300Å film grown at 405°C. It is apparent that many of the islands have coalesced, although the layer is not yet complete. In addition, there are many irregularities in the Moiré fringes which follow island-like boundaries. This suggests that the boundaries between coalescing islands are highly disordered. If two merging islands are of different size and therefore have different amounts of lattice relaxation, the lattice planes of the two islands will not line up correctly and defects such as dislocations may be generated. This explanation is supported by ion channeling measurements of strain in the films. As discussed in Ch. 3, the angular scan data show that the strain in the plane of the film is inhomogeneous, which suggests that the strain has relaxed to varying degrees in different islands.

Island coalescence can lead to threading dislocations in the following ways. In the same manner that dislocations are affected by SLSs, misfit dislocations in one island may be bent when they reach the different strain field in the other island, leading to threading dislocations in the epilayer. This, however, requires quite high stresses, which may not be present in the boundaries between most merging islands. Another source of threading
dislocations can be the rough surfaces arising from coalescing islands. Because of the high stresses acting on the film, there may be regions on the surface where the stress is especially high, and this could lead to defect generation. We do not know yet whether a particular type of defect is formed as a result of island coalescence, and also if the density or type of defect depends upon island size at the time of nucleation. Perhaps there would be fewer defects if all the islands were nucleated at the same time, and therefore are similar in size. Since the Si misorientation, growth temperature, and growth rate affect the structure and size of the islands, these growth parameters may also affect defect generation caused by islanding. This will be discussed in more detail in Ch. 5.
4.5 Results of attempts to grow island-free films

On several occasions, the growth of island-free films was attempted without success. This section summarizes the results of our efforts to grow three such wafers. At temperatures below roughly 200°C, the deposited GaAs was amorphous. Our comparison of 50Å thick films grown at different temperatures (Fig. 4-2) indicates that the surface coverage is on the order of 50% when the film is grown at 325°C and is somewhat lower for the 405°C film. It is quite likely, therefore, that complete amorphous layers formed at very thin GaAs coverages when the temperature is below 200°C.

The difficulty we encountered, however, is that the films were either so thin that they broke up into islands upon heating to higher temperatures, or so thick that they could not recrystallize. A 250Å layer grown at 175°C separated into islands when the temperature was raised. On the other hand, a 1000Å layer grown at 115°C could not be recrystallized upon heating to higher temperatures. On the third wafer, 250Å was grown at 175°C, and then the substrate temperature was gradually increased to 405°C while the growth continued, such that a total of 1000Å was grown. This wafer was amorphous after the growth, but a RHEED pattern of chevrons, indicating facetting, was obtained when it was heated to 575°C. Unfortunately, a 2μm overlayer grown on this buffer layer also showed a faceted RHEED pattern, and the surface morphology was extremely poor upon visual examination. Hopefully, the use of other procedures will lead to the growth of high-quality, island-free films.

4.6 Discussion

The preceding discussion indicates that island formation can lead to rough surfaces and higher defect densities in the film. Clearly, island formation is deleterious to the
growth of high-quality films. The best solution would be to avoid islanding altogether. However, there are no reports in the MBE literature which show that this has been achieved. If it is impossible to avoid islanding, then the crystal grower is faced with a dilemma: the nucleation of many islands will improve the surface morphology, but the nucleation of fewer islands may decrease the density of defects formed by coalescence. Defects can best be avoided by the nucleation of uniformly-sized islands, so that "lattice mismatches" between coalescing islands can be minimized. Currently, the best reliable reported dislocation densities are in the range of $10^7$/cm$^2$. The vast majority of the dislocations originate from the lattice and thermal expansion coefficient mismatches, so probably the increased defect levels due to island coalescence are insignificant. Therefore, the better strategy would be to improve the surface morphology by increasing the island density that is initially nucleated. One way of doing this is to use a low buffer layer growth temperature.

The surface mobility of the arsenic and Ga species can also be controlled with the shuttering of the arsenic and Ga beams. The deposition of a layer of Ga, or "Ga pre-layer", directly on the Si may increase the island density, as the photoemission work by Bringans et al. suggests [80]. This can be explained in the following way. Arsenic forms an extremely stable, fully coordinated passivating layer on Si, so that the Ga atoms that adsorb to this As pre-layer are probably quite mobile and diffuse long distances before bonding to the substrate [29]. As will be discussed in Ch. 5, GaAs nucleation occurs preferentially at steps on the Si surface. This suggests that the Ga atoms tend to diffuse on the As-passivated Si surface until it reaches the dangling bonds at a step, where it bonds. The use of a Ga pre-layer instead would probably lower the diffusion lengths of the surface species, and therefore increase the nucleation density. In addition, the work of Zinke-Allmang et al. indicates that high As/Ga flux ratios can also limit island size [81]. Their studies show that Ga is mobile and tends to cluster on As-terminated Si(111), but that the Ga atoms are immobilized by bonding to incoming As atoms. The more As atoms there are
impinging on the substrate, therefore, the less distance the Ga atoms will diffuse on the surface. Finally, as will be shown in Ch. 5, the Si cleaning procedure and heat treatments prior to the growth also affect the island structure and density and can be adjusted to improve the growth.

Because islands with large aspect ratios degrade the surface morphology, the growth of a buffer layer with a relatively smooth surface is essential. Our in situ annealing results show that the buffer layer should be an unbroken film; otherwise, island agglomeration occurs upon heating the wafer to the overlayer growth temperature, resulting in a much rougher thick film surface. If one employs the graded growth procedure, in which the Ga cell and substrate temperatures are ramped up while continuing the growth, the substrate temperature should be raised fairly slowly in order to avoid further uncovering of the substrate.

Our procedure of abruptly stopping the growth before growing the overlayer may give better control of defect propagation than the graded growth method. The ion channeling results discussed in this and the last chapter indicate that there is an abrupt improvement in the film crystallinity at the buffer layer/overlayer interface when the growth is initiated at low temperatures. In addition, the buffer layer relaxes at the overlayer temperature before the second stage of the growth. This may be beneficial in confining threading dislocations to the buffer layer and minimizing the formation of new misfit dislocations in the overlayer.
CHAPTER 5

Si SURFACE STEPS AND THEIR EFFECTS ON GaAs/Si NUCLEATION

Because antiphase domains (APDs) were such a problem in the early attempts to grow GaAs/Ge, GaP/Si, SiC/Si and other heteroepitaxial systems [82,83], a great deal of GaAs/Si research has been devoted to finding ways of avoiding these defects. As discussed in Chapter 1, APD formation depends on the types of steps that occur on the Si surface. The step density and type can, to some extent, be adjusted by using vicinal Si substrates, which are sliced several degrees away from the [100] surface normal. Shibahara et al. [83] have done a direct comparison by chemical etching of SiC grown on vicinal and well-oriented (100) substrates and found that use of the vicinal substrates eliminates APDs.

While APD suppression was the original goal of using vicinal Si substrates [31], thick GaAs/Si films are affected in other ways by the misorientation. Lee [84] and Fischer et al. [85] found that substrate tilt can improve the surface morphology. The Hall mobility and carrier concentration also vary with tilt [84]. From those results as well as the ones in Chapter 4, it is clear that the Si surface structure, GaAs nucleation processes, and thick film growth are interrelated. In this chapter, we investigate the way in which GaAs island nucleation is affected by the step type and density on the Si surface.

5.1 Background information

As discussed in Chapter 1, steps affect APD formation in the following way. Because of the tendency of As rather than Ga to bond to the Si surface, antiphase domains
form when GaAs islands nucleated at different sides of an odd atomic layer high step coalesce. APDs can be prevented, therefore, by using a Si surface consisting of a staircase of steps that are even multiples of $a_0/2$ high. Low energy electron diffraction (LEED) work by Henzler and Clabes [86] and Kaplan [87] shows that double steps tend to form on misoriented Si (100) surfaces prepared by sputter/annealing in vacuum. More recently, Sakamoto and Hashiguchi [88] have found by RHEED that annealing a two-domain, nominally on-axis Si (100) 2x1 surface at 1000°C for 20 minutes converts the surface to a single-domain 2x1 structure. This indicates that, within the resolution of the measurements, Si surface diffusion causes the odd atomic layer steps to disappear so that only even atomic layer steps remain.

Why does this reconstruction occur? $<011>$ steps tend to form on Si (100) surfaces, whether misoriented on not [89]. In the diamond cubic structure, [011] steps are distinguishable from [01$\bar{1}$] steps. They can be characterized by the relative orientations of the step direction and the Si dimer bonds on the upper terrace adjacent to the step. Using the notation of Kroemer [90], type A steps are parallel to the dimers, and type B are perpendicular to them. The different types of $<011>$ single and double steps are shown schematically in Fig. 5-1. Calculations by Chadi [67] and Aspnes and Ihm [91] show that there is an energetic preference for a staircase consisting of type A double steps rather than type B double steps or alternating type A and B single steps. They proposed different models for the geometry of the steps, and STM work by Wierenga et al. [92] confirmed Chadi's model.

The reasoning that a staircase of double steps is necessary for APD-free material has led to the common practice of heating the Si wafer to roughly 900°C or more prior to the epitaxy. Not only does this serve to desorb the surface oxide, but it also converts the surface to a single domain surface, assuming the appropriate tilt and anneal conditions are used. Recent work [76] has shown that this anneal does not appear to damage Si devices already existing on the substrate, so it is suitable for GaAs/Si monolithic integrated circuits.
Fig. 5-1. Schematic diagram of the different types of single and double steps on a Si(100) surface.

Although these results suggest that the lowest-energy Si (100) surface consists of an array of double steps of one particular type, in practice, this is not entirely accomplished. Even though a wafer may be cut off-axis toward [011], for example, there will be a small but finite slope in the [011] direction as well. This could conceivably create small sections of type B double steps in addition to the energetically favored type A. Nakayama et al. [93] proposed a way in which only type A double steps occur in either direction by having the terrace corners split into single steps. STM images by Wierenga et al. [92] show that there are kinks in type A double steps in which the step breaks into two single steps, so perhaps this is possible. However, such single steps could give rise to APDs.
It is also likely that, on step staircases in a <011> direction, there are a few remaining single steps on the surface. Some caution must be used in interpreting the step structures inferred from LEED and RHEED results, as these techniques sense only the major re-ordering on a surface and do not reveal any microscopic disorder which may be present. Inoue et al. [94] used Reflection Electron Microscopy (REM) to show that a Si (001) surface heated to 1000°C reconstructed largely to terraces of a single type of domain. However, some small regions of domain disorder still existed. These small regions would likely be undetectable by RHEED or LEED; thus the results are consistent with Sakamoto and Hashiguchi [88]. It is extremely likely that this occurs in all cases, as a perfectly reconstructed surface with all double steps would add a small configurational entropy term to the net free energy for the surface. Therefore, what appear to be APD-free GaAs epilayers may actually contain APDs that are too small to be detected by RHEED or chemical etching. It is also conceivable that certain domains are overgrown or never formed in the first place. In order for single-domain growth to occur, it is necessary for islands nucleated at type A double steps to overgrow those formed at other types of steps, or for nucleation on type B or single steps to be suppressed.

The geometry is somewhat different when the direction of the substrate tilt is not a <011> direction. In contrast to the single staircase of steps induced by tilts toward a <011> direction, there are two perpendicular staircases of <011> steps when the tilt is toward <001> [90]. In this case, there are equal lengths of [011] and [01\bar{1}] double steps; probably they are two perpendicular staircases of type A double steps offset by a single step from one another. This is shown schematically in Fig. 5-2. Kinks and other irregularities will alter this structure somewhat. Because of the surface symmetry, tilts toward a <001> direction antiphase domains will not prevent APD formation. This was confirmed experimentally by Akiyama [95]. However, he also found that an offset angle of less than 0.2 degrees away from [011] toward [001] would ensure single-domain growth. Sakai [96] suggests that there is competition between the nuclei forming on the
Fig. 5-2. Schematic diagram of the staircases of steps induced on Si(100) surfaces by tilts toward (a) <011> and (b) <001>.

perpendicular staircases; in order to prevent APDs, one type of nuclei need to overgrow the other type. Clearly a great deal more needs to be learned about the energetics and kinetics of bonding at the steps as well as the mechanism of overgrowth of one island by another.

Although the work of Akiyama [95] and Shibahara [83] show that the substrate tilt does affect APD formation, the exact role of the substrate is still controversial. As will be discussed in Ch. 6, the work of several groups indicates that a single-domain Si surface is not necessary for the growth of single-domain GaAs/Si.
5.2 Si surface reconstructions and step bands

Using RHEED, we find that the conversion of the Si surface to a two-domain structure depends on the misorientation. After heating a Shiraki-cleaned Si substrate to 880°C for 10 minutes in an arsenic ambient of 10⁻⁷ torr, the surface oxide desorbs and a clean, streaked RHEED pattern is obtained. On tilts of 1.2° or less toward <011>, a 2x2 pattern, presumably a mixture of 1x2 and 2x1 domains, is observed. On wafers tilted 3.7° or more off-axis, the pattern is 2x2 immediately after oxide removal, but it converts to 2x1 with further heating. This result can be explained as follows. The transformation of a Si surface from a two-domain to a single-domain structure occurs by Si atoms diffusing on the surface, causing some steps to disappear and others to form. The distance between steps is shorter on the more highly misoriented wafers, which means that Si atoms have less distance to diffuse on the surface in order to find a step. If the degree of tilt and/or the anneal temperature is sufficiently high that the terrace length is small compared to the Si surface diffusion length, the surface will convert to the single-domain structure.

This also explains the results of Shibahara et al. [83] discussed above. On tilted substrates it is easier to convert the substrate to the energetically preferred step structure, presumably a staircase primarily of double steps. Since there should be fewer single steps on the more highly misoriented substrates, APD formation should be less likely when vicinal rather than well-oriented (100) substrates are used.

Rather than the staircase of double steps that is expected from the theoretical and LEED results, however, cross-sectional TEM shows that a variety of Si step heights are found. In fact, we find that the steps tend to agglomerate to form high steps, which we will refer to as "step bands". This is shown in Fig. 5-3, cross-sectional TEM images of a 10Å GaAs film grown on a substrate misoriented 3.7° off-axis toward <011>; the electron beam is perpendicular to the tilt axis in these images. (In discussing GaAs consisting of islands rather than complete layers, the thickness given is the thickness that the epilayer
Fig. 5-3. Cross-sectional TEM images of a 10Å GaAs film grown on a substrate misoriented 3.7° off-axis toward <011>.

would be if it were a complete film. The individual islands, therefore, are higher than this designated thickness.) It can be seen that the GaAs islands have nucleated on the Si surface steps, which are much higher than $a_0/2$. The large terrace areas appear to be uncovered by GaAs. (Recently, however, photoemission and Auger results of Bringans et al. [97] and Biegelsen et al. [98], respectively, indicate that there may be a very thin GaAs layer between the islands. Such Stranski-Krastanov growth would not be detectable in these XTEM images). Fig. 5-4 shows an enlarged view of one of the islands in cross-section. The details of interfacial structure is difficult to interpret, but the substrate is clearly higher on one side of the island compared to the other, indicating that the island has nucleated on a large surface step.
Another feature of Fig. 5-4 is the roughly hemispherical shape of the island, typical of the islands we have seen. Biegelsen et al. [99] found that the islands grown at temperatures of 500°C or more are rounded, but those grown at lower temperatures show more evidence of facetting. In contrast, islands grown by MOCVD are distinctly pyramidal, having sidewalls consisting of (111) facets [100,101]. Calculations by Choi et al. [102] show that the equilibrium form of a GaAs island on (100) Si is that observed in the MOCVD films. The effects of adsorbates and the differences in growth temperature are the most likely explanations for these shape differences.

Although step bands appear on the Shiraki-cleaned surfaces without any heat treatment, they are significantly enhanced by the substrate heat treatment time. In Fig. 5-5, we compare the step bands on wafers tilted 3.7° toward <011> after being heated in situ for different lengths of time at 880°C in an As ambient of 10^{-7} torr. The left-hand ordinate is the average step band height, h, in units of (200) monolayers, and the right-hand ordinate is the percentage of (200) surface steps, S, included in these step bands. The total number of double steps was determined geometrically from the tilt and the lattice constant of Si. The solid dots and the arrows indicate the values of h and S, respectively. For
Fig. 5-5. A comparison of the step bands on wafers tilted 3.7° toward <011> after being heated for different lengths of time at 880°C in an As ambient of 10⁻⁷ torr. The data is taken from cross-sectional TEM images. The left-hand ordinate is the average step band height, h, in units of (200) monolayers, and the right-hand ordinate is the percentage of (200) surface steps, S, included in these step bands. The solid dots and the arrows indicate the values of h and S, respectively. The point marked by a cross refers to a 2x2 surface, and the triangle just below it is the corresponding value of S. The points marked at t=10 seconds actually correspond to t=0 seconds (the Shiraki-cleaned surface without anneal). All other points correspond to samples on which a very thin GaAs film has been grown.

In comparison, the point at 10 seconds anneal time refers to a Shiraki-cleaned wafer having no heat treatment afterward. It is apparent that both the average step band height and percentage of steps within step bands increase with anneal time. All of these samples had a 2x1 surface reconstruction after the anneal, as expected for this tilt. Also shown on the graph is a single point obtained from a sample of the same tilt but with an anomalous 2x2 reconstruction after a 20 minute anneal. Both h and S are unusually high for this sample.
The most likely explanation for the 2x2 reconstruction is that there was a great deal of surface contamination on the substrate, which interfered with the Si surface diffusion needed to convert the surface from double domain to single domain. We find that the occurrence of step bands also is promoted by increasing the degree of tilt toward <011>. It is apparent, therefore, that step band formation is affected by the anneal time, degree of misorientation and the amount of contamination on the surface.

While we consistently observe step bands, they have not been seen by other groups using similar growth procedures but quite different cleaning methods from the Shiraki method [89,98,103,104]. Fischer-Colbrie [103,104] prepared wafers in the following manner: the native surface oxide was stripped with HF in a flowing N2 ambient prior to transfer to the MBE system, and the wafer was then heated to 730°C for 30 minutes. Biegelsen et al. [98] used an ozone cleaning procedure followed by oxide desorption at elevated temperatures. The fact that step bands were not observed suggests that they result from the Ishizaka-type substrate preparation process. The most conclusive evidence for this is the STM work of Griffith et al. [89]. They found that that the surface steps tend to agglomerate when a Si cleaning procedure similar to the Shiraki clean was used, but not, however, on sputter/annealed samples.

There are several mechanisms that could account for step band formation. Robbins et al. [105] investigated and reviewed structural changes occurring during Si oxide desorption and high temperature annealing, some of which may be the source of step bands. Non-uniformities in the surface oxide can lead to preferential desorption at some areas of the surface, causing pinholes to form in the oxide [106]. Si atoms required to form the volatile SiO from SiO$_{1+x}$ can be supplied via step motion toward the pinholes, causing step agglomeration, as shown schematically in Fig. 5-6a. Perhaps this non-uniform desorption is especially pronounced for the oxide produced by the Shiraki clean. Another possibility, shown in Fig. 5-6b, is that impurity particles on the Si surface hinder step motion, causing the steps to pile up next to the impurity [107]. Auger studies by Krusor et al. [108] show
that the ozone cleaning procedure they use leaves less carbon on the surface than the Ishizaka clean; perhaps this is the reason they do not observe step bands on their wafers.

Fig. 5-6. Schematic diagrams of two possible methods of step band formation during the pre-growth anneal of the Si at 880°C. (a) Step agglomeration when Si atoms required to form the volatile SiO from SiO$_{1+x}$ are supplied by step motion toward the pinholes in the oxide; (b) step pile-up when impurity particles on the Si surface hinder step motion.
Fig. 5-7. Plan view TEM images of 30Å GaAs/Si films grown on Si wafers with varying degrees of misorientation toward <011>: (a)1.2°, (b)3.7°, (c)5.6°.
5.3 The Effects of Steps on GaAs/Si Nucleation

5.3.1 Island shape

We have examined the effects of different substrate misorientations on GaAs/Si nucleation. Fig. 5-7 shows plan view TEM images of 30Å GaAs/Si films grown on Si wafers with varying degrees of misorientation toward (011). The GaAs islands appear as Moiré fringes formed from interference from the <022> planes perpendicular to the steps. In all three cases the GaAs islands are greatly elongated parallel to the steps. It is apparent that the structure of the islands is affected by the degree of Si misorientation. Comparison is most meaningful, however, between the films on the 3.7° and 5.6° vicinal surfaces, because the Si surface reconstruction was 2x1 prior to the growths, while it was 2x2 for the wafer tilted 1.2° off-axis; these reconstructions are typically observed for the respective misorientations. The islands on the 5.6° off-axis substrate appear as long strings along the step direction. In contrast, those grown on the 3.7° off-axis wafer are more numerous and less anisotropically shaped. On the lowest tilt, there are some very long islands interspersed with regions of small islands.

Rough determinations of the mean nucleus spacing in these films was made by counting the number of islands intersecting a calibrated scale on the micrographs. The results of many of these measurements is shown in Fig. 5-8. The ordinate is the mean nucleus spacing in the direction of the tilt, and the abscissa is the spacing between double steps on the theoretically predicted Si surface. In all three films, the spacing between the islands in the direction of the tilt is roughly an order of magnitude greater than the distance between steps on a staircase of double steps; this spacing is consistent with the observations of nucleation at step bands.
Fig. 5-8. GaAs nuclei density as a function of Si tilt. The ordinate is the mean nucleus spacing in the direction of the tilt, and the abscissa is the spacing between double steps on the theoretically predicted Si surface.

Fig. 5-9. Plan view TEM images of approximately 50Å of GaAs on nominally on-axis Si(100). (a) g = [022], (b) g = [004].
The parallel island chains are not observed if the substrate is nominally on-axis (100) or tilted toward <001>. The former is illustrated in Fig. 5-9, where the different images were formed using different diffraction conditions. The majority of the islands appear to be randomly shaped. A few are slightly elongated in <011> type directions, probably because there are steps at those locations; STM images of on-axis Si(100) [89] show that there are indeed such steps on the surface.

Fig. 5-10 shows 30Å GaAs on Si tilted 4° toward <001>. In this case, the staircase of steps presumably consists of [011] and [011] sections [90]. Correspondingly, some of the islands are elongated in these two directions, although more irregularly shaped islands occur as well. The island structures in all these images apparently reflect the underlying substrate step arrangement.

Fig. 5-10. Plan view TEM image of 30Å GaAs film grown on Si tilted 4° toward <001>.
While STM is needed to determine the step structure underlying these islands, there are a number of possible explanations for the differences in island structure with the degree of tilt. One is that the islands preferentially nucleate at kinks in the steps, and that the average kink density in the steps depends on the degree of tilt. By cross-sectional TEM, we found that the average step band height is higher on a 4° tilt toward <011> than a 2° tilt, reflecting the fact that the steps need to travel shorter distances on the higher tilt before encountering another step. Step bands of different height probably have different energies, and therefore different kink densities. In addition, calculations by Pearson et al. [109] for Si(111) surfaces and Choi et al. [110] for GaAs(100) surfaces indicate interactions among ledges occur for separation distances as much as 50Å. If the same is true for Si(100), the step and terrace energies on different tilts will be different due to such interactions, and this will affect the kink density as well. Long-range interactions can also affect the relative tendencies of step versus terrace nucleation. Because the step energies may vary with height or the spacing between them, the density of nucleation sites will vary with misorientation.

In addition, GaAs nucleation should also occur preferentially at the types of steps high in energy due to dangling bonds. Double domain Si surfaces have odd atomic layer high steps, while those on single domain Si are predominantly even atomic layers high. The presence of different types of steps on the single and double domain Si surfaces, therefore, can affect the location and density of nucleation sites on the two surfaces. The different island shapes on the 1.2° off-axis wafer, therefore, may be due to nucleation at different types of steps.
Fig. 5-11. Asymmetry of strain for GaAs/Si films grown at 405°C on wafers misoriented 3.7° toward <011>. The data was obtained from ion channeling angular scans using <111> type zone axes.

5.3.2 Strain in the islands

Our plan view TEM results show that the shape of the islands on Si tilted toward <011> is anisotropic because of the Si steps. In addition, strain measurements using Rutherford backscattering angular scans show that the strain is anisotropic as well. Fig. 5-11 shows the results obtained using <111> type zone axes for the in-plane strain in films of thicknesses of 50, 300 and 1000Å, all grown on Si misoriented 3.7° toward <011>. These results as well as those in Ch. 3 indicate that the film relaxes with increasing coverage,
although there is still some residual strain after 1000Å is grown. In addition, strain anisotropy is observed in the 50Å and 300Å films, where the Si coverage by GaAs islands is not yet complete, but not in the 1000Å thick film, where there is complete coalescence. The compressive strain in the plane of the two thinner films is greater in the direction parallel to the steps than perpendicular to them; alternatively, the GaAs planes perpendicular to the steps are more compressively strained than those parallel to the steps. Hull and Fischer-Colbrie [70] found experimentally that the critical thickness for the commensurate/incommensurate growth transition depends on the lateral dimensions of the islands. The strain anisotropy we observe, however, is opposite to that expected from those findings. This is presumably a consequence of the stronger bonds between GaAs and Si step atoms compared to the terrace atoms; as a result, the GaAs planes perpendicular to the steps are "pinned" somewhat by the Si step atoms. The film apparently grows both vertically from the substrate and horizontally from the step edge; thus, the steps serve as a template for the growth.

This strain anisotropy is confirmed by the Moiré fringe spacing in the plan-view TEM images, which decreases as the GaAs relaxes. Fig. 5-12 shows the 30Å film on the 5.6° that appears in Fig. 5-7, where the difference between Fig. 5-12a and b is the diffraction condition. The fringe period is smaller in Fig. 5-12b, where the planes parallel to the steps were used to form the image, than in Fig. 5-12a, where the diffracting planes are perpendicular to the steps. This shows, once again, that the strain in the plane of the film is greater in the direction parallel to the steps.

In addition, Rosner [69] examined this strain anisotropy as a function of tilt on 250Å films grown by Fischer-Colbrie, whose procedures are described in Refs. 103 and 104. Although the strain parallel to the steps is roughly the same on tilts of 1.2° and 5.6° toward <011>, the strain perpendicular to the steps is significantly different on the two tilts. The anisotropy is much more pronounced on the higher tilt, in which the step density is greater.
Fig. 5-12. Plan-view TEM images of a 30Å GaAs film grown at 405°C on a Si wafer tilted 5.6° toward <011>. The operating g-vectors as shown are (a) parallel and (b) perpendicular to the steps on the surface.

This strain anisotropy also suggests that the dislocation structure is different in the directions parallel and perpendicular to the steps. XTEM work by Otsuka et al. [111] and subsequently by Lo et al. [112] suggests that the misfit dislocation type is affected by the presence of steps. They find that two types of misfit dislocations occur at the GaAs/Si interface: type I dislocations, in which the Burger's vector is parallel to the interface (1/2[011]), and type II dislocations, in which the Burger's vector is inclined 45° away from the interface in <110> directions. Clearly type I dislocations are the more effective in accommodating the lattice mismatch. In addition, type II dislocations are the source of threading dislocations and stacking faults. TEM examination by both groups suggests that steps assist the formation of type I dislocations, although further work is necessary to establish this conclusively.
5.4 Discussion

The occurrence of step bands can have important consequences for the quality of GaAs/Si films because the structure of the GaAs islands is greatly affected by them. Increased step agglomeration can lead to rougher GaAs surfaces for two reasons. First, the substrate surface roughness due to step bands provides a rough template for the epitaxy. Secondly, the reduced nucleation density means that the islands with high aspect ratio are formed, causing a rough GaAs film surface when the islands coalesce. Mars and Rosner [113] found that, after heating substrates above 1000°C, both the substrates and GaAs films grown on them have rough surface morphologies.

Step band formation could also explain why a number of groups [84,114] have reported that the surface morphology is a function of the substrate tilt. As the misorientation increases, there are more steps and the distance between them is smaller. It would therefore take less time at a given temperature to form step bands on highly tilted wafers. This would mean that there are more and higher step bands on wafers cut further off-axis when the same pre-growth heat treatment is used, as we have observed. Lee [84] found that the surface morphology degraded when the tilt was increased from 3° toward <011>. Although Lee did not use a Shiraki clean (the last cleaning step was an oxidation in nitric acid, followed by heating to 1000°C in the load chamber and then to 700°C in growth chamber), it is possible that step bands formed on the wafers. Both Fischer [114] and Lee [84] found that a certain amount of tilt was necessary for good morphology. The reason could be the suppression of antiphase domains, but Uppal and Kroemer found that the relationship between morphology and antiphase domains is unclear [115].

This suggests that the optimal pre-growth heat treatment depends on the substrate misorientation. Ideally, the anneal should desorb the surface oxide and convert the surface
to a single-domain structure without forming many step bands. A temperature and time combination suitable for low tilts may be too severe for higher tilts, particularly if the cause of step bands is the pile-up of mobile steps at surface impurities. One should use the shortest possible Si heat treatment before the growth, and tailor the anneal conditions for the particular misorientation used, so that step band formation is minimized. In addition, substrate cleaning procedures which do not lead to step band formation should be employed.

Another factor to consider is the different island structures on wafers of different tilts. The results of the last chapter indicate that island coalescence can be the source of additional defects, especially if the coalescing islands are of different size, and therefore are strained to different extents. Ideally, all the islands should be the same size. From Fig. 5-7a, it is apparent that the islands grown on the 1.2° tilt have a wide variety of sizes. Because the films on the higher tilts have more uniformly-sized islands, they are better for thick films as far as defects are concerned. On the other hand, because the density of the islands decreases with tilt, relatively small tilts are needed to get good surface morphology. Taking both these issues into account, the optimal tilt appears to be the 3.7° tilt.

Considering tilts toward directions other than <011> type, antiphase domains form when the tilt is toward <001> [78], so this tilt should be avoided. With tilt directions between <001> and <011>, there are two perpendicular staircases, but the lengths of the steps is different on the two surfaces. Since the GaAs forms island chains along the steps, that means that the perpendicular chains will be of different size. Probably the tilts towards <011> would give the preferable, more uniformly-sized islands than tilts between <001> and <011>.
CHAPTER 6

SUMMARY AND SUGGESTIONS FOR FUTURE WORK

6.1 Dissertation Summary

The aim of the work described in this dissertation is an understanding of the initial stages of GaAs/Si growth and their effects on the quality of GaAs layers. Our approach has been quite different from the majority of the GaAs/Si researchers, who have focussed on device fabrication. Progress on device work has been hampered by materials issues, necessitating an investigation of the growth processes. We have endeavored to improve the GaAs/Si growth conditions for device applications as well as to gain a better understanding of heteroepitaxy in general.

During the first phase of our work, we followed the growth from the very initial stages to the growth of thick films, using RHEED, TEM and ion channeling. We found that GaAs first forms islands on the Si that are compressively strained in the plane of the film due to the lattice mismatch. As the growth proceeds, these islands gradually coalesce and form a complete film. While this occurs, substantial atomic rearrangement occurs and the film crystallinity, as determined by ion channeling, improves considerably. The strain in the film also relaxes as more and more misfit dislocations are nucleated. When the low-temperature buffer layer is heated to 575°C for the overlayer growth, the film relaxes completely and there is a considerable improvement in crystallinity. Both ion channeling and XTEM show a marked change in the defect density in the region of the buffer layer/overlayer interface. For this reason, the two-step growth method may be more effective than the graded growth procedure in confining dislocations and other defects to the region near the GaAs-Si interface. As the film continues to grow, the dislocation
density drops, but there still are numerous threading dislocations in 2μm thick films. Characterization of these thick films by TEM, ion channeling, and x-ray diffraction shows that film quality is excellent, comparable to that grown by other laboratories for device purposes.

After examining this evolution of film structure, we focussed on GaAs island formation and the effects of this on thicker films. We found that the surface morphology of thick films degrades with increasing buffer layer temperature. This can be explained by the higher aspect ratios of islands grown at higher temperatures, creating a rough film surface upon coalescence. Although the buffer layer temperature affects the surface morphology, the crystallinity of the overlayer is independent of the buffer layer temperature. It is advantageous, therefore, to grow the buffer layer at low temperatures in order to improve the surface morphology of thick films.

In addition to surface morphology degradation, island formation can also lead to additional defect formation. We found that the planar compressive strain in thin, islanded films is inhomogeneous, apparently because different islands are relaxed to varying degrees. TEM images show crystalline irregularities at the boundaries between merging islands, where defects appear to be generated.

Using a growth rate of 0.4μm/hr and a substrate temperature of 405°C, a nearly continuous film is obtained after 500Å of growth. In situ annealing of this film at 575°C for 15 minutes does not expose more of the substrate and significantly improves the film crystallinity. In contrast, heating a 30Å film in the same way causes the islands to agglomerate, uncovering the substrate. This suggests that a buffer layer slightly thicker than 500Å is most suitable for the growth of thicker layers.

A third focus of our work has been on the role of Si surface steps in GaAs/Si nucleation. TEM images show that steps on vicinal Si(100) surfaces cleaned by a Shiraki-type procedure tend to cluster together to form step bands. Although the mechanism of step band formation is not known, it is probably related to one or both of the following.
mechanisms: the desorption of the chemical oxide formed by the Shiraki clean, or the pile-up of mobile steps at surface impurities during the pre-growth Si anneal. The average step band height and percentage of steps within step bands increase with anneal time and degree of tilt toward an <011> direction.

The vast majority of the GaAs islands nucleate at these step bands and grow along them. The island shape depends on the degree and direction of the misorientation from the [100] surface normal, reflecting the underlying step arrangement. The planar compressive strain within the islands is affected by the steps as well; the strain is greater in the direction parallel to the steps than perpendicular to them. Because the island structure is so sensitive to the Si surface steps, the surface morphology and defects in GaAs/Si films depend on the degree and direction of the substrate tilt.

6.2 Suggestions for Future Work

6.2.1 Island-free growth

Clearly, island-free GaAs/Si epitaxy would be optimal for the growth of thick films, improving both the surface morphology and defect density. Although we attempted a few such growths, island-free growth remains an elusive goal. As discussed in Ch. 4, the best strategy to achieve this is to increase the nucleation density by decreasing the surface mobility of the atoms on the growing film. From our work on the variation of buffer layer structure with temperature it is clear that very low buffer layer temperatures are necessary for island-free growth. In addition, step band formation causes the island density to decrease because the islands tend to nucleate at the step bands. It would be preferable instead to have a staircase of double-high steps so that there would be many more nucleation sites. Our work and that of Griffith et al. [89] show that step bands form
after Shiraki-type preparation procedures, which suggests that other cleaning methods are preferable for GaAs/Si growth; this is clearly a fruitful area for continued work. As discussed in Ch. 4, the passivating As layer on Si is probably responsible for high mobility of the adsorbing Ga atoms [29]. The use of a Ga pre-layer instead would probably lower the diffusion lengths of the surface species. The use of high As/Ga ratios may also do the same [81,116].

6.2.2 STM Research

Our work on steps and nucleation raises interesting questions that can best be addressed by using STM in combination with other methods. Our findings that the GaAs island structure varies greatly with the misorientation suggests that the step structures and energies are quite different on the different surfaces. This will affect the following surface characteristics: 1) the kink density on a given step; 2) the relative energies of the different steps; 3) the ratio of the step energies to the terrace energy. All of these influence the GaAs nucleation. In addition, the structure of the steps may be significantly altered when the As pre-layer is deposited, as the RHEED findings of Pukite et al. [117] suggest.

It would be interesting to compare, therefore, the step structure and energy on different Si misorientation. This can be studied in the following ways. STM can be used to determine the step structure, as was done for an on-axis and a vicinal Si(100) surface by Griffith et al. [89]. The overall surface symmetry can be examined by LEED. Theoretical work, such as that done by Choi et al. [110] and Pearson et al. [109] can determine if the Si surface steps tend to attract or repel, and the effective interaction distances.
6.2.3 *Mechanisms for antiphase domain suppression*

Although APD-free growth has been achieved, the mechanism for this is still unknown. Assuming that the substrate step structure alone determines whether APDs will form, there are a number of possible scenarios for APD suppression. The islands may preferentially nucleate at only certain types of steps, so that antiphase domains do not form. On the other hand, different islands may compete with one another, such that islands on one domain overgrow the others. A third possibility is that the antiphase domain boundaries meet and annihilate so that the material above contains fewer antiphase domains, as Uppal and Kroemer [115] have suggested.

Another controversy which is especially interesting is whether the GaAs growth procedure or the substrate structure prior to the growth is responsible for eliminating the APDs. It is certainly true that a surface consisting only of double steps will lead to APD-free growth. However, the work of several groups suggests that this is not a necessary condition, and that in fact the growth conditions play an important role. Wang [21] used nominally on-axis (100) wafers having 2x2 RHEED patterns and found that the reconstruction of the GaAs MBE epilayer could be changed from 2x4 to 4x4 (presumably a superposition of 2x4 and 4x2) by varying the initial growth temperature. Similarly, etching studies by Fischer et al. [85] show that there is a temperature window outside of which APD-free material can be grown. Nishi et al. [118] and Pukite and Cohen [117] also found that GaAs with a 2x4 RHEED pattern could be grown on a 2x2 Si(100) substrate by MOCVD and MBE, respectively. In addition, the RHEED results of Pukite and Cohen suggest that As adsorption changes the Si step structure from single steps to alternate single and triple steps on wafers misoriented 2.5° toward <011>. GaAs growth on such a surface, they find, is still single-domain. This is clearly a rich area for further investigation.
6.2.4 Threading dislocation suppression

Threading dislocations and other electrically active defects remain the most important problems impeding further GaAs/Si progress. While there have been a variety of attempts to reduce the dislocation density by using superlattices, anneals, and various nucleation schemes, none of these has been more than marginally successful. The use of these methods can reduce the dislocation density from roughly $10^9$/cm$^2$ in an untreated GaAs/Si film to $10^7$/cm$^2$; however, a density of $10^4$/cm$^2$ is the desired goal. Success in this final dislocation reduction appears far more difficult than at the higher dislocation densities. New ideas in the understanding of dislocation propagation and generation are required if GaAs/Si technology is to progress beyond its current state. One important question is why all the threading dislocations are not blocked by the superlattices and anneals. It is still not known whether these remaining dislocations are different from the others, or whether the density of dislocations is the factor determining the effectiveness of these methods. Further work needs to be done to determine which dislocation types tend to thread through the film.

The mechanism of dislocation generation is another important issue that needs to be addressed. Clearly, a high density of dislocations is required near the GaAs/Si interface to take up the lattice mismatch, but there is no fundamental need for threading dislocations. Perhaps the threading dislocations are caused by the tensile stresses developed in the film during the cool-down from the growth temperature. Island coalescence may also be another cause of threading dislocations. In addition, steps on the Si surface have been shown to effect the type of dislocation nucleated, but their exact role is not understood. The location of dislocation nucleation, whether at the film surface or at the GaAs-Si interface, is also unclear. In order to devise effective ways of reducing threading
dislocation densities, these questions need to be examined more fully. In fact, the solution of these problems will greatly impact the future success of GaAs/Si technology.
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