LOW FREQUENCY NOISE AS A CHARACTERIZATION AND
RELIABILITY TOOL FOR THE EVALUATION OF ADVANCED
MOSFETS

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF SCIENTIFIC
COMPUTING AND COMPUTATIONAL MATHEMATICS
AND THE COMMITTEE ON GRADUATE STUDIES
OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

Paul Lim
September 2009
UMI Number: 3382777

INFORMATION TO USERS

The quality of this reproduction is dependent upon the quality of the copy submitted. Broken or indistinct print, colored or poor quality illustrations and photographs, print bleed-through, substandard margins, and improper alignment can adversely affect reproduction. In the unlikely event that the author did not send a complete manuscript and there are missing pages, these will be noted. Also, if unauthorized copyright material had to be removed, a note will indicate the deletion.

UMI

UMI Microform 3382777
Copyright 2009 by ProQuest LLC
All rights reserved. This microform edition is protected against unauthorized copying under Title 17, United States Code.

ProQuest LLC
789 East Eisenhower Parkway
P.O. Box 1346
Ann Arbor, MI 48106-1346
I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

James S. Harris, Jr.  Principal Adviser

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

(H.-S. Philip Wong)

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Robert W. Dutton

Approved for the University Committee on Graduate Studies.

Peter J. Swart
Abstract

The continued scaling of MOSFET feature sizes, including the gate area, has been the major approach of the integrated circuits industry to achieve increases in speed and density for the past 40 years. This reduction in the gate area leads to several very challenging problems and even potential roadblocks, due to the fundamental limits imposed by the unbreakable laws of physics. One of these is the inevitable increase in device noise levels, which has significant impact on the device performance.

Due to the limitations of continued scaling, research has started to focus on alternative materials to the Si-SiO₂ combination in conventional MOSFETs. These alternative materials combinations must meet two fundamental requirements in order to be seriously considered as potential replacements for conventional silicon technology. The first is that the alternative material devices must exceed several operating benchmarks of conventional silicon devices, and the second is that it must also maintain these advantages throughout their commercially useful lifetime.

In this thesis, noise in these advanced MOSFETs is characterized, and used for evaluating alternative technologies on both of these fundamental requirements. For the first requirement, noise characterization offers a powerful yet simple way to evaluate the passivity of the new semiconductor-dielectric interface. Noise behavior subject to various bias and gate scaling reveals device transport mechanisms that are otherwise unseen in measured I-V curves. For the second requirement, the noise behavior of the candidate devices under stress tests often manifest damage earlier than detectable by more conventional methods, and the manner of noise degradation adds evidence to the suspected transport mechanisms.

Advanced MOSFET devices that were characterized in this work covered various
types, and include one where silicon was still used as the channel material, but with a hi-κ dielectric (Si-SiHfON), another where germanium was used as the channel material coupled with a hi-κ dielectric (Ge-HfO₂), and a third where 1-D carrier transport was utilized with carbon nanotubes as the channel material (CNTFETs).

The advanced bulk MOSFETs (Si-HfSiON and Ge-HfO₂) were shown in this work to have higher magnitudes of 1/f noise than conventional Si-SiO₂ MOSFETs in agreement with expectations due to higher interface trap densities. It was also shown that these advanced bulk devices have similar bias and scaling dependence of the noise to that of conventional Si-SiO₂ MOSFETs, giving evidence that the mechanisms for noise are similar. Under hot-carrier stress, it was found that the noise degradation of these devices eventually saturated, while the threshold voltage degradation did not for the period of time tested, giving evidence that the main contribution to the voltage shifts in these devices is due to mobile charge migration in the oxide, in agreement with the observed hysteresis and threshold voltage instabilities.

For CNTFETs, it was shown that despite the transport advantages of 1-D CNTs, these devices have much higher noise levels and hot-carrier stress led to degradation comparable to conventional Si-SiO₂ MOSFETs, giving evidence that a source of 1/f noise in CNTFETs is the underlying oxide. These results emphasized that reliability studies of CNTFETs must not be ignored, if the technology is to continue as a viable alternative for conventional CMOS.
Acknowledgements

First on the list is my adviser, Prof. James Harris, fondly known as "Coach" within the research group. Aside from being mentally very sharp, Coach has a zest for life and adventure that inspires us all, in academic terms and in real life. No doubt that was his secret to remaining young and active. I was a stray cat in my PhD research and Coach gave me a home.

Next in line are the professors who have served as my mentors throughout the years. Professors Philip Wong, Robert Dutton and Yoshio Nishi not only served as members of my defense committee but gave me numerous assistance when I encountered difficulties in my research. Prof. Andrew Stuart served as an early adviser when I was absorbed in the interesting field of nonlinear dynamics. Prof. Gautam Iyer served as chair of my defense committee and was a frequent badminton friend as well.

Not to be forgotten are the research associates who have been part of my research at one point or another. Dr. Yang Liu was, and still is, a collaborator in my study of 1/f noise. Dr. Zhiping Yu taught me the basics of semiconductor device simulation. Gail Chun-Creech is simply the best admin ever, attending not only to Coach's needs but to everyone else.

My superiors at National Semiconductor, Prasad Chaparrala, Richard Taylor, Samuel Martin, Amjad Obeidat and Jeff Babcock taught me the fine arts of device parameter extractions, reliability tests, and noise measurements, without which I would not have been able to master the skills needed for my research work.

The members of the Harris group at Stanford throughout the years have provided some great company. I have forged great friendships with Mark Wistey (who is like
a brother to me), Tomas Sarmiento (Ola!), Tom O’Sullivan (Milkshake!), Hopil Bae (Hopil-a!), Donghun Choi (Donghun-a!), Junxian Fu, Xiaojun Yu, Angie Lin (thanks for laughing at my misfortunes), Larkhoon Leem, Altamash Janjua, Ke Wang, Luigi Scaccabarozzi, Yu-Hsuan Kuo, Tom Lee (my one and only collaboration within the group), Li Gao, Jun Pan, Evan Pickett, Barden Shimbo, Xiao Hann Lim, Mathilde Gobet, Evan Thrush, Yiwen Rong, Seth Bank, Homan Yuen, Lynford Goddard, Rekha Rajaram, Meredith Lee, Yangsi Ge, David Jackrel, Rafael Aldaz, Yijie Huo, Wonil Ha, Chien-Chung Lin, Xian Liu, Kai Ma, Vincenzo Lordi, Dan Grupp, Qiang Tang, Alireza Khalili, Hyunsoo Yang, Zhihong Rao, Hai Lin, Robert Chen, Ed Fei, Lele Wang, Sonny Vo, Anjia Gu, Dong Liang, Shuang Li and many others.

Outside of academics, friends have given me lots of chances to enjoy life. The members of the Indonesian society at Stanford Willy Wiyatno, Yuniarto Widjaja, Alvin Barlian, Freddy Samad, Tira Hendrata and many more along with several members of the Filipino, Korean, Chinese, and Taiwanese groups have provided me with lots of fun. When it came time for parties and out-of-town trips, I’ve been fortunate to have the company of the Santa Cruz beach crew: gang leader Linda Huynh ("boss", "the wall"), and her slaves Gerardo Silva, Bryan Mai and Mark Miranda. Wayne Lum allowed me free us of his badminton facility and was my frequent partner for delicious meals that made me gain much weight, and was also my fellow Netflix devil. Kiam Tey coached me for a time in badminton and was a big help on getting me started on using Microsoft Excel as an automation tool for my research.

And finally, the many years of PhD study would have been too much if not for the support of my family. My dad, Avelino Lim, passed away before I came to graduate school but nevertheless remained with me in spirit. My mom, Suy Eng Lim, made sure I’m always well-fed and in good health. My uncle Florencio Lim was like a second dad to me. My sisters, Billie Ngotiaco and Kevin Lim, have always been there in times of difficulties. My two nephews Timothy and Joshua Ngotiaco always found time to play with me whenever I visited them, and their dad and my brother-in-law Ferdinand Ngotiaoco always made me feel welcome.
Dedication

To Woody, Axel, and Jazmin, fellow stray cats saved by the awesome Coach.
Errata

This page reserved for future corrections.
# Contents

Abstract iv  
Acknowledgements vi  
Dedication viii  
Errata ix  

## 1 Introduction to Noise in Semiconductors  
1.1 Motivation and Thesis Outline 1  
1.2 Noise 3  
1.3 Major Types of Noise in Semiconductors 3  
1.3.1 Johnson Noise 3  
1.3.2 Shot Noise 4  
1.3.3 Generation-Recombination (G-R) Noise 5  
1.3.4 Flicker (1/f) Noise 6  
1.4 Theories of 1/f Noise 8  
1.4.1 Number Fluctuation Model 8  
1.4.2 Mobility Fluctuation Model 10  
1.4.3 Dominant 1/f Noise Mechanism in MOSFETs 12  
1.5 Application of Noise to Semiconductor Device Reliability 12  

## 2 1/f Noise in MOSFETs  
2.1 Motivation for Studying 1/f Noise in MOSFETs 13
2.2 MOSFET fundamentals ........................................... 14
  2.2.1 Carrier Mobility ............................................. 15
  2.2.2 Current-Voltage Relationships ............................. 17
  2.2.3 Effect of Substrate Bias ................................... 21
2.3 MOSFET Interface Traps and Characterization Techniques .... 22
  2.3.1 Capacitance-Voltage curves (Low frequency quasi-static) methods 22
  2.3.2 Charge Pumping ............................................ 23
  2.3.3 Other Methods .............................................. 23
2.4 1/f Noise in MOSFETs .......................................... 24
  2.4.1 MOSFET Noise Model ...................................... 24
  2.4.2 Sources of 1/f Noise in MOSFETs: Number Fluctuation vs Mobility Fluctuation .............................................. 26
  2.4.3 Impact of Substrate Voltage on 1/f Noise .................. 31
  2.4.4 Input Referred Noise ...................................... 31
  2.4.5 Summary .................................................. 32

3 Motivation to Go Beyond Si-SiO\textsubscript{2} ................. 33
  3.1 Advantages of Scaling ....................................... 33
  3.2 Disadvantages of Scaling .................................... 35
  3.3 Short Channel Effects ........................................ 36
  3.4 Impact of Scaling on Low-frequency Noise .................... 37
  3.5 Alternative Materials ....................................... 38
    3.5.1 Alternative Bulk Channel Materials ...................... 38
    3.5.2 Low-dimensional Carbon-based Channel Materials ....... 40
    3.5.3 Alternative Dielectrics ................................ 47

4 Noise Characterization of MOSFETs ............................. 49
  4.1 Noise Measurement Setup ..................................... 49
    4.1.1 External Sources of Extraneous Noise .................. 50
    4.1.2 Internal Sources of Extraneous Noise .................. 52
    4.1.3 Noise Equipment Setup ................................ 52
  4.2 Silicon-Silicon Dioxide (Si-SiO\textsubscript{2}) MOSFETs ........ 54
<table>
<thead>
<tr>
<th>Chapter</th>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.2</td>
<td>4.2.1</td>
<td>Bias Dependence</td>
<td>54</td>
</tr>
<tr>
<td>4.2</td>
<td>4.2.2</td>
<td>Temperature Dependence</td>
<td>58</td>
</tr>
<tr>
<td>4.2</td>
<td>4.2.3</td>
<td>Gate Area Dependence and Scaling</td>
<td>59</td>
</tr>
<tr>
<td>4.3</td>
<td>4.3.1</td>
<td>Device Fabrication</td>
<td>62</td>
</tr>
<tr>
<td>4.3</td>
<td>4.3.2</td>
<td>1/f Noise Characteristics</td>
<td>63</td>
</tr>
<tr>
<td>4.3</td>
<td>4.3.3</td>
<td>Summary of 1/f Noise Behavior of Si-HfSiON MOSFETs</td>
<td>66</td>
</tr>
<tr>
<td>4.4</td>
<td>4.4.1</td>
<td>Ge-MOSFETs</td>
<td>67</td>
</tr>
<tr>
<td>4.4</td>
<td>4.4.2</td>
<td>Device Fabrication</td>
<td>69</td>
</tr>
<tr>
<td>4.4</td>
<td>4.4.3</td>
<td>1/f Noise Characteristics</td>
<td>69</td>
</tr>
<tr>
<td>4.4</td>
<td>4.4.4</td>
<td>Summary of 1/f Noise in Ge-HfO₂ pMOSFETs</td>
<td>73</td>
</tr>
<tr>
<td>4.5</td>
<td>4.5.1</td>
<td>Role of Oxide Traps in CNTFET 1/f Noise</td>
<td>75</td>
</tr>
<tr>
<td>4.5</td>
<td>4.5.2</td>
<td>Summary of 1/f Noise in CNTFETs</td>
<td>76</td>
</tr>
<tr>
<td>5</td>
<td>5.1</td>
<td>Introduction to Device Reliability</td>
<td>81</td>
</tr>
<tr>
<td>5</td>
<td>5.1.1</td>
<td>Device Lifetimes</td>
<td>82</td>
</tr>
<tr>
<td>5</td>
<td>5.1.2</td>
<td>Hot-Carrier Effects</td>
<td>82</td>
</tr>
<tr>
<td>5</td>
<td>5.1.3</td>
<td>Negative Bias Temperature Instability</td>
<td>85</td>
</tr>
<tr>
<td>5</td>
<td>5.2</td>
<td>Silicon-Silicon Dioxide (Si-SiO₂) MOSFETs</td>
<td>88</td>
</tr>
<tr>
<td>5</td>
<td>5.3</td>
<td>Silicon-HfSiON MOSFETs</td>
<td>91</td>
</tr>
<tr>
<td>5</td>
<td>5.3.1</td>
<td>Hot Carrier Stress</td>
<td>91</td>
</tr>
<tr>
<td>5</td>
<td>5.3.2</td>
<td>Recovery</td>
<td>92</td>
</tr>
<tr>
<td>5</td>
<td>5.3.3</td>
<td>Summary</td>
<td>93</td>
</tr>
<tr>
<td>5</td>
<td>5.4</td>
<td>Germanium-HfO₂ MOSFETs</td>
<td>94</td>
</tr>
<tr>
<td>5</td>
<td>5.4.1</td>
<td>Temperature Dependence</td>
<td>96</td>
</tr>
<tr>
<td>5</td>
<td>5.4.2</td>
<td>Hot-Carrier Stress</td>
<td>97</td>
</tr>
<tr>
<td>5</td>
<td>5.4.3</td>
<td>Summary</td>
<td>99</td>
</tr>
<tr>
<td>5</td>
<td>5.5</td>
<td>Carbon Nanotube MOSFETs</td>
<td>100</td>
</tr>
</tbody>
</table>
5.5.1 Device Fabrication and Characteristics ........................ 100
5.5.2 Device Reliability under Hot-Carrier Stress ................ 100
5.5.3 Summary of CNTFET Noise and Reliability under Hot-Carrier Stress ........................................ 102

6 Summary and Future Work ........................................ 105
   6.1 Summary ...................................................... 105
   6.2 Future Work .................................................. 107

A Noise Measurement Automation Code ........................... 108
List of Tables

3.1 Semiconductor Mobilities ........................................ 39
3.2 Dielectric Properties ........................................... 48
# List of Figures

1.1 MOSFET Noise Types .............................................. 4  
1.2 Lorentzian .......................................................... 6  
1.3 GR Noise ........................................................... 7  
1.4 Sum of Lorentzians ............................................... 9  
1.5 McWhorter traps .................................................. 10  

2.1 MOSFET schematic diagram ...................................... 14  
2.2 Carrier mobility .................................................. 17  
2.3 MOSFET band diagram .......................................... 18  
2.4 MOSFET $I_d-V_d$ .................................................. 20  
2.5 MOSFET $I_d-V_g$ .................................................. 21  
2.6 MOSFET Noise Model ............................................ 25  
2.7 MOSFET Carrier Number Fluctuation .......................... 27  

3.1 MOSFET scaling .................................................... 34  
3.2 Carbon Nanotube from Graphene ............................... 41  
3.3 Carbon Nanotube Chirality ..................................... 42  
3.4 Carbon Nanotube FET ............................................ 43  
3.5 CNT Schottky Barrier ............................................ 44  
3.6 CNTFET vs Si FET ................................................. 45  
3.7 Dielectric band alignment ...................................... 48  

4.1 Noise Measurement Setup ....................................... 53  
4.2 NMOS noise gate bias dependence in linear region ......... 55
<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.3</td>
<td>NMOS noise gate bias dependence in saturation region</td>
<td>56</td>
</tr>
<tr>
<td>4.4</td>
<td>PMOS noise gate bias dependence in linear region</td>
<td>57</td>
</tr>
<tr>
<td>4.5</td>
<td>NMOS noise gate bias dependence in saturation region</td>
<td>58</td>
</tr>
<tr>
<td>4.6</td>
<td>PMOS noise temperature dependence</td>
<td>59</td>
</tr>
<tr>
<td>4.7</td>
<td>NMOS noise temperature dependence</td>
<td>60</td>
</tr>
<tr>
<td>4.8</td>
<td>Gate leakage noise</td>
<td>61</td>
</tr>
<tr>
<td>4.9</td>
<td>Si-HfSiON gate stack structure</td>
<td>63</td>
</tr>
<tr>
<td>4.10</td>
<td>Si-HfSiON MOSFET $I_d-V_g$ curves</td>
<td>64</td>
</tr>
<tr>
<td>4.11</td>
<td>Si-HfSiON MOSFET drain current noise vs gate bias</td>
<td>65</td>
</tr>
<tr>
<td>4.12</td>
<td>Si-HfSiON MOSFET drain current noise vs drain current</td>
<td>65</td>
</tr>
<tr>
<td>4.13</td>
<td>Si-HfSiON MOSFET normalized transconductance vs drain current</td>
<td>66</td>
</tr>
<tr>
<td>4.14</td>
<td>Si-HfSiON MOSFET $I_d-V_g$ curves under various substrate biases</td>
<td>67</td>
</tr>
<tr>
<td>4.15</td>
<td>Si-HfSiON MOSFET drain current noise vs gate overdrive with substrate bias</td>
<td>67</td>
</tr>
<tr>
<td>4.16</td>
<td>Ge PMOS gate structure</td>
<td>68</td>
</tr>
<tr>
<td>4.17</td>
<td>Ge PMOS $I_d-V_g$</td>
<td>70</td>
</tr>
<tr>
<td>4.18</td>
<td>Ge FET Noise</td>
<td>71</td>
</tr>
<tr>
<td>4.19</td>
<td>Ge FET Noise vs Drain Bias</td>
<td>72</td>
</tr>
<tr>
<td>4.20</td>
<td>Ge FET Noise vs Gate Bias</td>
<td>73</td>
</tr>
<tr>
<td>4.21</td>
<td>Ge FET Noise vs Gate Length</td>
<td>74</td>
</tr>
<tr>
<td>4.22</td>
<td>Ge FET Noise vs Gate Width</td>
<td>75</td>
</tr>
<tr>
<td>4.23</td>
<td>CNT noise</td>
<td>76</td>
</tr>
<tr>
<td>4.24</td>
<td>CNTFET noise</td>
<td>77</td>
</tr>
<tr>
<td>4.25</td>
<td>Noise of annealed CNT</td>
<td>78</td>
</tr>
<tr>
<td>4.26</td>
<td>Suspended CNT</td>
<td>79</td>
</tr>
<tr>
<td>4.27</td>
<td>Noise of suspended CNT</td>
<td>80</td>
</tr>
<tr>
<td>5.1</td>
<td>MOSFET Hot Carriers</td>
<td>83</td>
</tr>
<tr>
<td>5.2</td>
<td>NBTI $V_{th}$ Degradation</td>
<td>85</td>
</tr>
<tr>
<td>5.3</td>
<td>NBTI $g_m$ Degradation</td>
<td>86</td>
</tr>
<tr>
<td>5.4</td>
<td>MOSFET interface traps</td>
<td>87</td>
</tr>
<tr>
<td>Section</td>
<td>Topic</td>
<td>Page</td>
</tr>
<tr>
<td>---------</td>
<td>-------</td>
<td>------</td>
</tr>
<tr>
<td>5.5</td>
<td>Hot Carrier $I_d - V_g$ Degradation</td>
<td>89</td>
</tr>
<tr>
<td>5.6</td>
<td>Hot Carrier Trap Density Increase</td>
<td>90</td>
</tr>
<tr>
<td>5.7</td>
<td>Hot Carrier 1/f Noise Degradation</td>
<td>91</td>
</tr>
<tr>
<td>5.8</td>
<td>Si-HfSiON MOSFET $I_d-V_g$ curves under hot carrier stress</td>
<td>92</td>
</tr>
<tr>
<td>5.9</td>
<td>Si-HfSiON MOSFET $V_{th}$ shifts under hot carrier stress</td>
<td>93</td>
</tr>
<tr>
<td>5.10</td>
<td>Si-HfSiON MOSFET 1/f noise degradation under hot carrier stress</td>
<td>94</td>
</tr>
<tr>
<td>5.11</td>
<td>Si-HfSiON MOSFET $V_{th}$ recovery under reverse stress</td>
<td>95</td>
</tr>
<tr>
<td>5.12</td>
<td>Si-HfSiON MOSFET noise recovery under reverse stress</td>
<td>95</td>
</tr>
<tr>
<td>5.13</td>
<td>Ge FET Noise Temperature Dependence</td>
<td>96</td>
</tr>
<tr>
<td>5.14</td>
<td>Ge FET $I_d - V_g$ Hysteresis Temperature Dependence</td>
<td>97</td>
</tr>
<tr>
<td>5.15</td>
<td>Ge-FET $I_d-V_g$ Degradation</td>
<td>98</td>
</tr>
<tr>
<td>5.16</td>
<td>Ge-FET $V_{th}$ Degradation</td>
<td>98</td>
</tr>
<tr>
<td>5.17</td>
<td>Ge-FET Noise Degradation</td>
<td>99</td>
</tr>
<tr>
<td>5.18</td>
<td>CNTFET $I_d-V_d$</td>
<td>101</td>
</tr>
<tr>
<td>5.19</td>
<td>CNTFET $I_d-V_d$</td>
<td>101</td>
</tr>
<tr>
<td>5.20</td>
<td>CNTFET Noise</td>
<td>102</td>
</tr>
<tr>
<td>5.21</td>
<td>CNTFET $I_d - V_g$ Degradation</td>
<td>103</td>
</tr>
<tr>
<td>5.22</td>
<td>CNTFET $V_{th}$ Degradation</td>
<td>103</td>
</tr>
<tr>
<td>5.23</td>
<td>CNTFET Noise Degradation</td>
<td>104</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction to Noise in Semiconductors

1.1 Motivation and Thesis Outline

Every year, the continued scaling of MOSFET feature sizes, including the gate area, has been the major approach of the integrated circuits industry to achieve increases in speed and density. In 2015, the International Technology Roadmap for Semiconductors predicts that 25nm node technology will be reached [1]. This reduction in the gate area leads to several very challenging problems and even potential roadblocks, including higher noise levels, as will be discussed in the next chapters. Even though it may appear that noise is more relevant to analog circuits than digital circuits, in very small devices, the noise may start to affect the high and low levels of digital circuits [2], increasing logic error rates to potentially unacceptable levels.

Due to the limitations of continued scaling, research has started to focus on alternative materials to the Si-SiO₂ combination in conventional MOSFETs. These alternative material combinations must meet two fundamental requirements in order to be seriously considered as potential replacements for conventional silicon technology. The first is that the alternative material devices must exceed several operating benchmarks of conventional silicon devices, and the second is that it must also maintain these advantages throughout their commercially useful lifetime.
In this thesis, noise is used for evaluating the alternative technologies on both of these fundamental requirements. For the first requirement, noise characterization offers a powerful yet simple way to evaluate the passivity of the new semiconductor-dielectric interface. Noise behavior subject to various bias and gate scaling reveals device transport mechanisms that are otherwise unseen in measured I-V curves. For the second requirement, in many cases noise behavior of the candidate devices under stress tests manifest damage earlier than detectable by more conventional methods. In some cases, the manner of noise degradation under stress adds evidence to the suspected transport mechanisms.

Chapter 1 introduces the basics of noise in semiconductors, focusing on flicker (1/f) noise, and some of its mechanisms are discussed.

Chapter 2 starts with a brief review on basic MOSFET operation, carrier transport, and basic current-voltage relationships. 1/f noise in MOSFETs is then discussed, where noise-bias relationships are derived subject to the various noise mechanisms.

Chapter 3 covers the problems of continued scaling for Si-SiO\textsubscript{2} MOSFETs, device and material limitations, and outlines the motivation to look for alternative materials to replace conventional silicon technology. The virtues of various channel materials and dielectrics are then considered.

Chapter 4 starts with a discussion of the noise measurement setup, followed by results of noise characterization on conventional Si-SiO\textsubscript{2} MOSFETs which are used as benchmarks to compare alternative devices against. The remainder of the chapter discusses the noise characterization of various alternative devices, exploring their strengths and weaknesses, transport properties, and semiconductor-dielectric interface quality.

Chapter 5 introduces noise as a reliability tool for MOSFETs, starting with Si-SiO\textsubscript{2} MOSFETs again to set benchmark behavior under hot-carrier stress. The same alternative MOSFETs characterized in Chapter 4, are then also subjected to hot-carrier stress, and their noise behavior under stress is studied for clues to transport and noise mechanisms.

Chapter 6 summarizes the results the noise characterization and reliability studies, and suggest future direction of research.
1.2 Noise

Noise is generally defined to be the part of the signal that is a deviation from the steady state response of a system. These are typically random and uncorrelated fluctuations of the signal [3, 4]. Fluctuations in electronic devices can be caused by external sources, like AC power lines, mechanical vibrations, electromagnetic transmissions, etc., or they can arise from fundamental internal sources that affect the carrier transport like the discrete nature of the carriers, lattice defects, oxide traps, phonon scattering, and other physical processes.

1.3 Major Types of Noise in Semiconductors

As shown in Figure 1.1, there are several noise mechanisms that are typically observed in semiconductor devices over various frequency ranges. The total noise is thus a sum of these various noise components, like Johnson thermal noise, shot noise, generation-recombination noise, and flicker (or 1/f) noise [3, 5]. Any type of noise that is flat across the entire spectrum is commonly classified as "white" noise, in analogy to "white" light, which consists of all the visible colors (frequencies) vs noise sources with a frequency dependence, such as 1/f noise.

1.3.1 Johnson Noise

Johnson or thermal noise arises from the thermodynamic fluctuations of electron density in a material at any finite temperature. The voltage power spectral density of Johnson noise is expressed as [3]:

\[ S_V = 4k_BTR; S_I = \frac{4k_BT}{R} \]  

(1.1)

where \( k_B \) is the Boltzmann constant, \( T \) is the absolute temperature in Kelvin, and \( R \) is the resistance of the material. It has no dependence on frequency and so is flat across the entire spectrum, hence it is a common example of white noise. However, it is not expected thermal noise to be constant up to indefinitely high frequencies, as
CHAPTER 1. INTRODUCTION TO NOISE IN SEMICONDUCTORS

4

Figure 1.1: Diagram showing examples of various types of noise and their addition to produce the total noise observed [5].

this would imply an infinite noise power, which is physically impossible.

As every electronic device has non-zero resistance, thermal noise is therefore unavoidable, but it can be minimized through good device design.

1.3.2 Shot Noise

Shot noise comes from the fluctuations arising from carriers independently and randomly surmounting or crossing a barrier [3]. The name comes from the notion that when listened to on a speaker, the noise source sounds similar to the volley of shots coming from a fired shot gun. It is typically dominant in devices like diodes and bipolar junction transistors, where current is produced by driving carriers over a barrier. Shot noise is described by the following current power spectral density
where $q$ is the fundamental charge and $I$ is the current through the device.

The fundamental process behind shot noise is the discrete nature of the electronic charge for each electron. The current across the barrier is determined by the number of carriers, each carrying the charge $q$, flowing at a particular rate. Shot noise results from the fluctuation in this flow due to the individual electrons crossing the barrier independently and randomly.

### 1.3.3 Generation-Recombination (G-R) Noise

Generation-Recombination noise in semiconductors originates from traps or defects that randomly capture and release carriers, thus causing fluctuations in the number of carriers available for current transport in the material. Trapped charges in turn, may affect the other free carriers, thus possibly inducing secondary fluctuations. The power spectral density for Generation-Recombination noise is described by [3]:

$$S_N = 4\Delta N^2 \frac{\tau}{1 + (2\pi f)^2 \tau^2}$$  \hspace{1cm} (1.3)

where $\Delta N^2$ is the variance of the number of carriers $N$, and $\tau$ is the carrier lifetime.

If $N \gg N_T$ where $N_T$ is the number of traps, the current power spectral density for Generation-Recombination noise can be converted to the form [5]:

$$S_I = I^2 \frac{N_T}{N^2} \frac{\tau}{1 + (2\pi f)^2 \tau^2}$$  \hspace{1cm} (1.4)

The shape described by Equation (1.4) is commonly called a Lorentzian (Figure 1.2), and it can be derived by taking the Fourier transform of a telegraphic signal representing trapped and released states in the time domain (Figure 1.3).

For a distribution of time constants, the power spectral density will sum up into an expression proportional to $1/f$, as will be described in Section 1.3.4.
1.3.4 Flicker (1/f) Noise

Flicker noise is also called 1/f noise because of its inverse dependence on the frequency of its power spectral density. Most conductors with flowing current exhibit some type of 1/f noise, which as of now has not yet been fully understood. The near ubiquity of this type of noise in conducting solids suggests a fundamental source, and it is independent of the type of material. Indeed 1/f noise has been observed in metals, semiconductors and semimetals. The effective dimension space of the device is also not a factor in its occurrence.

The power spectral density is of the form

\[ S(f) \propto f^{-n} \]  \hspace{1cm} (1.5)
where $0.8 < n < 1.4$ over a frequency range of several orders of magnitude. The integral of such a power spectra over all frequencies would diverge. At low frequencies, the divergence is of the form $n = 1$ or higher, but there is a lower limit in frequency in practice, so this is usually not a problem. Such limits can be from breakdown of the system for extremely long times for instance. For high frequencies, the divergence is for $n = 1$ or lower, but measurement rolloffs and cutoffs put an upper limit on the frequency range.

The next section describes the various theories and models that are currently being considered for the occurrence of $1/f$ noise in semiconductors. These theories are often competing and have given rise to many disagreements among physicists in this field. However, there are a few features of $1/f$ noise that are commonly agreed upon. These include the observation that resistance fluctuations are present, even in the absence of driving current. The appearance of $1/f$ noise in a material in equilibrium alludes to
the existence of local noise sources. It is also agreed that the spectral density scales inversely with system size.

1.4 Theories of 1/f Noise

There are two competing theories as to the dominant source of 1/f noise, with each having its own fervent supporters. The first is the number fluctuation model, and the second is the mobility fluctuation model. Each is described in the two following sections.

1.4.1 Number Fluctuation Model

Theory

The number fluctuation model proposes that the dominant source of 1/f noise is charge number fluctuation mechanisms in the material. Such processes have a Lorentzian spectral distribution [6]:

\[ S(f) \propto \frac{f_c}{f^2 + f_c^2} \]  

(1.6)

where \( f_c \) is the corner frequency. The 1/f spectra is created from a collection of such Lorentzians with a distribution of corner frequencies, as shown in Figure 1.4. McWhorter in 1957 proposed [7] that in germanium MOSFETs, the charge fluctuations occur at the semiconductor-oxide interface where there are electron traps distributed in the oxide, and the trapping and detrapping processes are at work. These processes can be a result of quantum tunneling from the bulk or fast interface states. The distribution of the corner frequencies are then a result directly associated with the distance of the traps to the interface (see Figure 1.5). As a result of this paper, the number fluctuation model is sometimes called the McWhorter model, especially when discussed in the context of 1/f noise in MOSFETs.

It can be inferred from Fermi statistics that only states with energies near the Fermi level have much fluctuation in their occupancy. The relative independence of
1/f noise on temperature then necessarily implies that the trapping states not only have a range of positions, but must also have a range of energies.

**Dutta-Horn Extension**

It was observed that there was some temperature dependence of the noise in metals [8]. Extending the number fluctuation model to account for this temperature dependence, Dutta and Horn [9] generalized the source of 1/f noise by including all processes that have activation energies with an Arrhenius form $f_0 \exp(-E/kT)$. 

![Figure 1.4: The sum of Lorentzians, each with slope proportional to $1/f^2$, is a curve with a slope proportional to $1/f$ [5].](image-url)
Critical discussion

The biggest weakness of the number fluctuation model is that despite its physical plausibility, only a few cases are explained by it, most of them involving interfaces between two different materials [5]. Nevertheless, it is currently accepted that there is very strong evidence that in semiconductors, trapping-detrapping processes are the main sources of 1/f noise [5]. This is easily shown by varying the number of traps and the resulting proportionality of the magnitude of 1/f noise. Similarly, it has also been shown [7] that 1/f noise in semiconductors is sensitive to surface treatment.

1.4.2 Mobility Fluctuation Model

Theory

The mobility fluctuation model was originally introduced in 1969 by Hooge [10] (hence sometimes referred to as the Hooge model), and postulated an empirical formula for 1/f noise as
\[
\frac{S_R(f)}{R^2} = \frac{\alpha_H}{N f} \quad (1.7)
\]

where \(\alpha_H\) is the so-called Hooge constant, \(N\) is the number of charge carriers in a homogenous sample, \(R\) is the resistance, and \(S_R(f)\) is the power spectral density of the resistance fluctuations at frequency \(f\).

The original data fitting Equation (1.7) was taken from Au films doped with impurities, and was based on the assumption that the fluctuations are due to phonon scattering [10]. Using other materials (e.g. semiconductors), it was found that corrections needed to be applied on \(\alpha_H\) to account for non-phonon scattering. Several additional corrections followed until finally it was proposed that \(\alpha_H\) be made an adjustable parameter that is dependent on the material type and quality [5, 11].

**Role of Material Defects in Mobility Fluctuations and 1/f Noise**

By using crystals of poor quality (compared to Si or GaAs) like HgCdTe, it was demonstrated [5, 12] that defects and other deviations from crystal symmetry lead to higher 1/f noise magnitudes attributable to larger mobility fluctuation. Consistent with this notion, relatively high noise levels have been observed in amorphous silicon [13]. The currently most widely accepted notion is that the mobility fluctuation component of the 1/f spectrum has a strong correlation with the degree of disorder of the material [14, 15].

**Critical discussion**

The main weakness of the Hooge model is that it is purely empirical and has no fundamental connection to physical properties of the materials and devices. Even though a large number of descriptions have been developed in attempt to support the Hooge formula [16, 17], it still suffers from the fact that it does not give an accurate physical picture of the data [18]. The most glaring flaw is exposed by the descriptions that try to explain the presence of \(N\) in the formula, which suggests that some independent fluctuations are occurring on each of the mobile carriers. This however, is inconsistent with the 1/f spectrum itself, since any fluctuation tied to individual
mobile carriers cannot persist for times longer than the time that the carrier remains in the sample. This can be verified by checking the transit and diffusion times of carriers, which are typically at most in the millisecond range. This would have required the flattening out of the spectrum at a lower limit of the frequency, which is not observed.

1.4.3 Dominant 1/f Noise Mechanism in MOSFETs

In MOSFETs, due to the presence of traps in the gate oxide and the oxide interface, the drain current is subject to fluctuations caused by the trapping and de-trapping of carriers in the oxide and interface. This would tend to support that the number fluctuation is the dominant low frequency noise mechanism in MOSFETs. However, there is evidence that mobility fluctuations may be the main mechanism for some pMOSFET devices [5, 19, 20]. Up to the present, there is still much debate as to which mechanism actually dominates the low frequency noise in MOSFETs. These mechanisms will be discussed in detail in the next chapter.

1.5 Application of Noise to Semiconductor Device Reliability

As noise in general is a natural process of scattering of discrete carriers in a discrete lattice structure, it is unavoidable and ubiquitous. As discussed earlier, Johnson noise is present in all conductors. Shot noise is present whenever there are discrete carriers going over a potential barrier. Flicker noise however, can be considered as "excess" noise, in that based on the discussion of the theories of its mechanisms in the previous section, its existence relies on interface or material defects. It does not necessarily have to be absolutely present in any material. This is what makes using 1/f noise as a diagnostic tool so powerful, that its significant presence signals the existence of defects, whether in the material or an interface. It is thus not surprising that in the past decade, suggestions have been made that noise (particularly the 1/f component) be used as a diagnostic or reliability tool [21, 22]. In the next chapters, this use for 1/f noise is applied specifically on MOSFETs.
Chapter 2

1/f Noise in MOSFETs

2.1 Motivation for Studying 1/f Noise in MOSFETs

In the previous chapter, the basic theory on mechanisms of 1/f noise in semiconductors was introduced. This chapter gives a basic introduction on the fundamentals of MOSFET physics and operation, followed by the MOSFET noise model and finally a discussion of the mechanism of 1/f noise in general MOSFETs.

As described at the end of the previous chapter, the study of 1/f noise in semiconductor devices gives insight as to the quality of the material or an interface. A MOSFET device will have a channel material where the carrier transport is affected by defects and impurities. It will also have an interface with interfacial and oxide traps in close proximity to the carriers in the channel. These mechanisms contribute to make 1/f noise the dominant noise process in MOSFETs.

The study of 1/f noise in MOSFETs is thus motivated by several reasons. First, being the dominant noise process, it is the easiest to measure. Second, being sensitive to defects in either the material or the interface, it is a good diagnostic tool for the overall quality of the device. Third, again its sensitivity to defects also makes it a powerful reliability tool in studying the damage progression or "aging" of devices during operation.
Owing to the second reason, the study of 1/f noise in MOSFETs with material combinations other than Si-SiO₂ offers a chance to evaluate the interface of the new material combinations. Because different insulators will have different trap levels, they will have different noise properties, thus providing a useful tool to investigate their stability. The third reason allows the evaluation of these material combinations for commercial viability in terms of lifetimes and reliability.

2.2 MOSFET fundamentals

A MOSFET is a four-terminal device labeled as the gate, source, drain, and substrate terminals as shown in Figure 2.1 [23–26]. In normal operation, the drain and source terminals will have a voltage difference so as to make current flow between them possible. Voltage applied on the gate terminal is used to control the current flow. The substrate terminal is usually grounded, but may also be biased to achieve certain body effects which adjust the threshold voltage at which the device "turns on".

![MOSFET schematic diagram](image)

Figure 2.1: A MOSFET schematic diagram showing the four terminals, the terminal voltages and currents and some device parameters [5].
CHAPTER 2. 1/F NOISE IN MOSFETS

The source and drain are heavily doped compared to the rest of the body, and with dopants that are of the opposite conductivity type compared to the body doping type. The gate electrode, which is usually metal or poly-silicon, is separated from the body by a gate dielectric, which was SiO$_2$ for most of the past 50 years but today may be a thin insulating material of some oxide compound other than SiO$_2$.

2.2.1 Carrier Mobility

Carrier transport in semiconductors is facilitated by two mechanisms. The first is the drift of the carriers due to an applied electric field, and the second is the diffusion of carriers due to a concentration gradient, which is of growing importance with the extremely short channel length devices utilized today. The drift mechanism is dominant in MOSFETs under the bias conditions for typical operation and for the noise measurements in this thesis and will be discussed here.

When an electric field is applied, the charged carriers are accelerated by the induced force and they develop an average drift velocity, $v_d$, on top of the random thermal velocity. This carrier velocity however, does not accelerate indefinitely under the electric field because of frequent scattering from material dopants and other impurities, lattice defects and vibrations (phonons), oxide and interface traps, and carrier collisions. Each scattering event results in the involved carriers losing their momentum in the direction of the electric field, so the average drift velocity is relatively constant for a constant applied field. At a low electric field, $E$, the drift velocity is proportional to the field strength

$$v_d = \mu E$$  \hspace{1cm} (2.1)

where the constant of proportionality $\mu$ is defined as the mobility. Another relationship for mobility and drift velocity can be derived by considering that in the time between scattering events, the applied electric field $E$ will accelerate the carriers with a force of $qE$. Assuming the effective mass of the carriers is $m^*$, then the acceleration is given by $qE/m^*$ and the average drift velocity that the carriers gain during a mean
free time $\tau$ between scattering events is

$$v_d = \frac{qE\tau}{m^*} \quad (2.2)$$

Thus, mobility can also be defined as [2, 23]

$$\mu = \frac{q\tau}{m^*} \quad (2.3)$$

At high electric fields, the increase in the average carrier energy is offset by the increasing energy loss due to optical-phonon emission. This results in a decrease in the carrier mobility as the electric field increases, and the drift velocity saturates at a limiting value, $v_{sat}$, called the saturation velocity. For most semiconductors, $v_{sat}$ is of the order $10^7$ cm/s. This applies to carrier transport in bulk semiconductors.

The effective carrier mobility in the inversion channel of a MOSFET is lower than in the bulk because of its confinement in a narrow region and proximity to the oxide interface, exposing it to additional scattering mechanisms due to surface roughness and surface phonons, in addition to the interface and oxide traps and defects. At high gate voltages, there is further degradation in the effective channel mobility due to the increase in the electric field normal to the carrier flow in the channel, pressing the carriers more closely to the oxide interface.

Assuming that the different scattering mechanisms (Figure 2.2) are independent of each other, the effective channel mobility can be approximated using Mathiessen's rule [27]

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_C} + \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} + ... \quad (2.4)$$

where $\mu_C$ is the mobility from Coulomb scattering due to ionized dopants and impurities, and charged traps in the oxide or interface, $\mu_b$ is the mobility due to bulk phonon scattering, $\mu_{ac}$ is the mobility due to surface acoustic phonon scattering, and $\mu_{sr}$ is the mobility due to surface roughness scattering.
2.2.2 Current-Voltage Relationships

When a MOSFET has a gate bias higher than a particular level called the threshold voltage, the increase in surface potential will invert the conductivity type of the substrate near its interface with the gate dielectric, and a channel of carriers of opposite type to that of the substrate will form in this region (Figure 2.3) [2, 23]. This channel allows current to flow between the source and the drain, and the device is considered to be in strong inversion and switched on. A MOSFET with a p-type substrate will form an n-type channel under operation and will be referred to as NMOS or NMOSFET and one with an n-type substrate will form a p-type channel and will be referred to as PMOS or PMOSFET.
The threshold voltage $V_T$ is approximated by [24–26]

$$V_T = V_{fb} \pm 2\psi_B \pm \frac{\sqrt{4\epsilon q N_{sub} \psi_B}}{C_{ox}}$$  \hspace{1cm} (2.5)

where $V_{fb}$ is the flatband voltage, $\psi_B$ is the energy difference between the Fermi level $E_F$ and the intrinsic level $E_i$, $\epsilon$ is the semiconductor permittivity, $N_{sub}$ is the substrate doping density, and $C_{ox} = \epsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area. The plus signs correspond to NMOS and the minus signs to PMOS. The flat-band voltage (literally, the applied voltage where the MOSFET bands are completely flat) depends on the workfunction difference between the gate metal and the substrate material $\phi_{ms}$ and the charge trap density $Q_{ox}$ at the interface of the oxide and semiconductor [24–26]:

$$V_{fb} = \phi_{ms} - Q_{ox}/C_{ox}$$  \hspace{1cm} (2.6)

The threshold voltage is defined as the voltage required to produce an inversion carrier density equal to the bulk doping value, hence the surface potential of $\Psi_S = 2\Psi_B$. The inversion charge density is approximated as

$$Q_i(V) = C_{ox}(V_{GS} - V_T - mV)$$  \hspace{1cm} (2.7)
where \( V \) is the potential along the channel, and \( m = 1 + C_d/C_{ox} \), typically between the values 1 to 1.4, is the body effect coefficient which is used as a correction factor. \( C_d = \sqrt{\varepsilon qN_{sub}/4\psi_B} \) is the bulk depletion capacitance. The body effect will be discussed further in the next section.

As can be seen in Equation 2.7, the gate voltage controls the charge density in the channel region, thus modulating the conductivity between the source and drain. Through this modulation, the drain current can be controlled by the gate bias, given the drain-source voltage. In the region \( V_{DS} < V_{DS,sat} \), commonly referred to as the linear region, the drain current is described in long-channel devices by

\[
I_D = \frac{W}{L} \mu C_{ox} [(V_{GS} - V_T) V_{DS} - m V_{DS}^2/2] \tag{2.8}
\]

where \( \mu \) is the effective carrier mobility in the channel. The drain current increases with drain voltage until it typically reaches a saturation point at \( V_{DS,sat} = (V_{GS} - V_T)/m \) due to the channel disappearing at the drain end commonly called channel pinch-off (Figure 2.4). At saturation, the drain current for long-channel devices thus remains essentially constant at

\[
I_{D,sat} = \frac{W}{L} \mu C_{ox} \frac{(V_{GS} - V_T)^2}{2m} \tag{2.9}
\]

With continued increase of the drain voltage beyond \( V_{DS,sat} \), this pinch-off point where the channel disappears moves toward the source side, decreasing the effective channel length of the device. In long channel devices, this so called channel length modulation can be neglected. In short channel devices however, the modulated length becomes a significant proportion of the entire device length and the effect on the drain current is far more noticeable. In this case, the short channel effect leads to the drain current continuing to weakly increase with \( V_D > V_{D,sat} \) without saturating.

At the subthreshold region where \( V_{GS} \) is below the threshold voltage \( V_T \), there is a small diffusion current (Figure 2.5)

\[
I_D = \frac{W}{L} \mu C_{ox} (m - 1) \left( \frac{kT}{q} \right)^2 e^{q(V_{GS} - V_T)/m kT} (1 - e^{-q V_{DS}/kT}). \tag{2.10}
\]
This current is limited by emission over a barrier, and those carriers that are emitted may be traveling at $v_{sat}$ with enough drain bias.

The subthreshold slope ($SS$) describes the ability to turn off a MOSFET where [25]

$$SS = \left[ \frac{d(\log_{10}I_D)}{dV_{GS}} \right]^{-1} \approx 2.3 \frac{mk_BT}{q} = 2.3 \frac{k_B T}{q} \left[ 1 + \frac{C_d}{C_{ox}} \right]. \quad (2.11)$$

It is desired that the subthreshold slope be as low as possible since this means that the current drop is steeper for decreasing gate voltage and therefore turn the MOSFET on or off faster which leads to a lower threshold voltage, higher on current, and lower relative subthreshold off current.
Figure 2.5: MOSFET $I_D - V_G$ curve under a fixed Drain voltage shown in logarithmic scale on the left and linear scale on the right [5].

### 2.2.3 Effect of Substrate Bias

This section covers the effect of an applied substrate bias $V_{BS}$ on the device parameters, called the body effect. The effect of $V_{BS}$ to the depletion charge is described by the equation [25]

$$Q_d = \sqrt{2eQ_{sub}(2\psi_B + V_{BS})}$$

(2.12)

The depletion region in the substrate is thus increased when the substrate is reversed biased, and decreased when the substrate is forward biased. Thus a reverse substrate bias leads to an increase in the effective electric field which then decreases the effective mobility. On the other hand, a forward substrate bias leads to the opposite effect.

As the dependence of the depletion charge on the substrate bias is a square-root relationship, it is not anticipated to have a significant effect on the noise of the device.
2.3 MOSFET Interface Traps and Characterization Techniques

A properly working MOSFET cannot have a semiconductor-dielectric interface trap density, \( N_T \), that is too high, or Fermi-level pinning may force the gate bias to go much higher before achieving strong inversion in the channel. Interface traps are attributed to dangling bonds at the semiconductor-dielectric interface, and interact electrically with carriers in the semiconductor channel. A good Si-SiC MOSFET typically has an interface trap density on the order of \( 10^{10} \) cm\(^{-2}\)eV\(^{-1} \) \cite{28}. In this section, a summary of common electrical interface trap density measurement techniques are discussed.

2.3.1 Capacitance-Voltage curves (Low frequency quasi-static) methods

This method utilizes the capacitance-voltage (C-V) curves measured from using the MOSFET gate as one terminal and tying the MOSFET drain, source, and substrate together to form the other terminal, and then sweeping the gate voltage from accumulation to deep inversion. As the voltage is swept across the range, the interface states change from being empty to being occupied by electrons, and this change of charge in response to the change in gate voltage has the effect of a capacitor in parallel with the MOSFET \cite{2}.

The measurement of interface states density is essentially performed by comparison to a case where either there are no interface states, or the interface states are rendered inactive \cite{28}. Typically, a C-V measurement at high frequency is performed so that the interface traps cannot follow the ac probe frequency, and do not contribute to the capacitance. The result is then used as a reference. A low frequency C-V measurement is next performed and compared to the reference, and from the shifts in the curves, the interface states density is calculated.
The main advantage of this method is that it is easy to measure, while the disadvantages are that it is difficult to measure the density of interface traps when the gate area is small or the gate leakage is significant [28], so it is impractical for small-area gate MOSFETs.

2.3.2 Charge Pumping

In this method, the MOSFET source and drain are tied together slightly reverse biased [28]. A time varying (or pulsed) gate voltage sufficient to drive the device alternatively to accumulation and inversion is then applied. The charge-pumping current is then measured at the substrate.

This method relies on the fact that during the shift from accumulation to inversion and then back, interface traps change states from being empty to filled, and vice versa, these states also interact with the electrons and holes alternately present in the channel and the trapping and detrapping processes end up producing the charge-pumping current. The interface trap density is derived from this measured current.

The main advantage of the charge-pumping method is that measurements can be done on relatively small-area gate MOSFET structures. Its main disadvantages are that the measurement is very sensitive to gate leakage current, measurements on semiconductor-on-insulator devices are difficult, and measurements may be pulse-frequency dependent.

2.3.3 Other Methods

There are other electrical measurement methods used to estimate interface charge density like subthreshold current, DC-IV and DLTS methods [28], but their details will not be discussed here. The subthreshold current method relies on calculating the interface trap density from the subthreshold slope, $SS$, and is better for measuring changes in the interface trap density (for instance when under stress) rather than the interface trap density itself. The DC-IV method is quite similar to the charge-pumping method, except that only DC biases are used, and for interface trap density
CHAPTER 2. 1/F NOISE IN MOSFETS

extraction, requires accurate knowledge of the capture cross-sections and surface recombination velocities, which may be difficult to obtain. The deep-level transient spectroscopy (DLTS) method uses temperature dependent transient analysis and is often too complicated to setup.

In the next section, 1/f noise in MOSFETs is discussed and will be used in Chapters 4 and 5 for semiconductor-dielectric interface studies.

2.4 1/f Noise in MOSFETs

Advances in CMOS technology have seen the development of smaller and faster transistors following the rate predicted by Moore's law. For analog applications, the reduction of noise in transistors is important to reduce the corruption in the output signal. In digital circuits with extremely small transistors, the noise may be enough to obscure the high and low signal levels.

On another issue, the search for alternative material combinations to Si-SiO₂ requires the quick evaluation of these new MOSFET devices. Unlike the 50 years of history with Si-SiO₂ MOSFETs, the new MOSFETs don’t have a reliability track record behind them. The approach to fundamental limits on continued scaling of Si-SiO₂ MOSFETs however, has put tremendous pressure to find in a matter of a few years, a suitable alternative material combination that can be quickly evaluated for CMOS suitability.

To both ends, the research on noise in MOSFETs has grown in importance. To study how noise affects the device parameters, the next section reviews some MOSFET noise models. Since the interest is mainly in 1/f noise, the descriptions are limited to models tailored for low frequency noise sources.

2.4.1 MOSFET Noise Model

The MOSFET low frequency noise equivalent circuit is described in Figure 2.6 [5, 26].

The MOSFET output drain current noise is a contribution from the various MOSFET component noise. The noise from the source resistance can be seen as the
superposition of thermal noise and 1/f noise

\[ S_{I_{th}} = \frac{cI_D^2}{f} + 4k_BT/R_S \]  

(2.13)

where \( c \) is some constant, and similarly the noise from the drain resistance is

\[ S_{I_{RD}} = \frac{cI_D^2}{f} + 4k_BT/R_D \]  

(2.14)

since device symmetry is assumed with respect to the source and drain regions. The inversion channel is approximately resistive and so the channel noise is

\[ S_{I_{Dch}} = 4k_BTg_{ch} \]  

(2.15)

where \( g_{ch} \) is the channel conductance.

For a general MOSFET operating circuit with a load \( R_L \), the contributions of the
noise of these components to the output drain current noise is

\[
S_{I_D} = \frac{S_{I_{D, ch}} + g_{ch}^2 R_{D}^2 S_{I_{RD}} + R_{S}^2 (g_{m} + g_{ch})^2 S_{I_{RS}} + S_{I_{RL}} [1 + g_{m} R_{S} + g_{ch} (R_{S} + R_{D} + R)]^2}{[1 + g_{m} R_{S} + g_{ch} (R_{S} + R_{D} + R)]^2}
\]  

(2.16)

2.4.2 Sources of 1/f Noise in MOSFETs: Number Fluctuation vs Mobility Fluctuation

As discussed in Section 1.4.3, there is an ongoing debate as to whether 1/f noise in MOSFETs is attributable to carrier number fluctuation or to carrier mobility fluctuation. As there is evidence for both sides, both theories are discussed as applied to MOSFETs. In addition, the possibility that the mobility fluctuation may have arisen from the Coulomb scattering caused by the trapped carriers associated with the number fluctuation theory is also discussed. This extension is called the number-correlated mobility fluctuation theory.

1/f Noise due to Number Fluctuations

As mentioned in Section 1.4.1, 1/f noise in MOSFETs due to fluctuations in the number of channel carriers was first presented by McWorther in 1957 [7]. The physical mechanism for this process is described by the trapping and detrapping of individual carriers into oxide or interface traps, as previously described. The resulting change in the surface potential gives rise to the fluctuations in the inversion charge density, which is translated into fluctuations in the flowing drain current (Figure 2.7).

An expression can be derived for the noise power spectral density under the assumption that the noise mechanism is purely due to the tunneling transitions of carriers into and out of traps in the gate oxide. For a single trap, the generation-recombination noise can be described by [5]

\[
S_{Q_{ox}} = \frac{4q^2}{W^2 L^2} \frac{\Delta N_{ox}^2}{\Delta z} \frac{\tau}{1 + (2\pi f \tau)^2}. \tag{2.17}
\]

where the variance in the number of oxide charges \(\Delta N_{ox}^2\) is calculated using the
Figure 2.7: Electrons in the channel of the MOSFET move in and out of traps, causing a change in the inversion charge density which in turn affects the drain current. This trapping and detrapping process also affects the mobility of the free carriers in the channel through Coulomb scattering, and this effect is called number-correlated mobility fluctuations [5].

Fermi-Dirac distribution function $f(E)$ as

$$
\Delta \overline{N_{ox}^2} = f(E)(1 - f(E))
$$

(2.18)

Considering all traps, it is noted that only those that are at or near the quasi-Fermi level will contribute to 1/f noise, since all others are either permanently filled or empty. Assuming that the trap density, $N_t$, is constant over the gate area, then integrating over all the relevant traps, gives [5]:

$$
S_{Q_{ox}} = \frac{4q^2k_B T}{WL} \int_0^{\tau_{ox}} N_t \frac{\tau}{1 + (2\pi f \tau)^2} dz.
$$

(2.19)

Although an energy dependent trap activation process is possible, and will give 1/f
noise spectra if the time constants depend exponentially on energy, it is assumed that the tunneling process in traps is dominant. In this case, the trapping time constant is described by $\tau = \tau_0(E) \exp(z/\lambda)$ where $\lambda$ is the tunneling attenuation length calculated by WKB approximation. The integral can then be evaluated and in terms of flat-band voltage noise [5],

$$S_{V_{fs}} = S_{Q_{ox}}/C_{ox}^2 = \frac{q^2k_BT\lambda N_t}{WLC_{ox}^2} \frac{1}{f}.$$  \hspace{1cm} (2.20)

Translating to drain current noise, this gives

$$S_{I_D} = S_{V_{fs}}g_m^2 = \frac{q^2k_BT\lambda N_t}{WLC_{ox}^2} \frac{I_D^2}{(V_{GS} - V_T)^2} \frac{1}{f}.$$  \hspace{1cm} (2.21)

Normalizing to the square of the drain current finally gives

$$\frac{S_{I_D}}{I_D^2} = \frac{(q^2k_BT\lambda N_t)(V_{GS} - V_T)^2}{WLC_{ox}^2} \frac{1}{f}.$$  \hspace{1cm} (2.22)

Mobility Fluctuations

As mentioned in 1.4.2, in 1969 and the years following, Hooge proposed [10, 11, 16] that 1/f noise in solids is a bulk effect and this process attributed to carrier mobility fluctuations was extended to the drain current fluctuations in MOSFETs. Hooge's theory states that in any conductor, the resistance fluctuations can be described by the empirical formula [10]

$$\frac{S_R}{R^2} = \frac{\alpha_H}{N} \frac{1}{f}.$$  \hspace{1cm} (2.23)

where $R$ is the resistance of the sample, $N$ is the number of carriers, and $\alpha_H$ is the Hooge constant. It is recalled from 1.4.2 that this "constant" is not really fixed but due to various scattering mechanisms that may be involved under different bias conditions, so it is actually bias-dependent. For MOSFETs, the number of carriers in the channel can be calculated as

$$N = \frac{1}{q}WLQ_t,$$  \hspace{1cm} (2.24)
which gives the normalized drain current fluctuation

\[
\frac{S_{I_D}}{I_D^2} = \frac{\alpha_H q}{WLQ_i f}. \tag{2.25}
\]

At higher drain biases, the carrier density \(Q_i\) is not uniform along the length of the channel so the integration of the contribution of infinitesimal segments along the channel must be performed to achieve a result valid over a range of drain bias conditions [5]:

\[
\frac{S_{I_D}}{I_D^2} = \frac{\alpha_H \mu_{eff} q V_{DS}}{L^2 I_D} \frac{1}{f}. \tag{2.26}
\]

To complete the discussion of mobility fluctuations, the effect of having multiple scattering processes involved in causing the fluctuations must be considered. Assuming the scattering processes and their respective fluctuations are independent of each other, Mathiessen's rule can then be used to calculate the effective mobility \(\mu_{eff}\)

\[
\frac{1}{\mu_{eff}} = \sum_j \frac{1}{\mu_j} \tag{2.27}
\]

and so the fluctuation in the effective mobility would be

\[
\frac{\Delta \mu_{eff}}{\mu_{eff}^2} = \sum_j \frac{\Delta \mu_j}{\mu_j^2} \tag{2.28}
\]

Now,

\[
\frac{S_{\mu_{eff}}}{\mu_{eff}^2} = \sum_j \frac{\mu_{eff}^2}{\mu_j^2} S_{\mu_j} \tag{2.29}
\]

and for each scattering process

\[
\frac{S_{\mu_j}}{\mu_j^2} = \frac{\alpha_{Hj} q}{WLQ_i f} \tag{2.30}
\]

so [5]

\[
\frac{S_{I_D}}{I_D^2} = \frac{S_{\mu_{eff}}}{\mu_{eff}^2} = \frac{q}{WLQ_i f} \sum_j \frac{\mu_{eff}^2}{\mu_j^2} \alpha_{Hj} \tag{2.31}
\]
Thus, the effective Hooge constant \( \alpha_{Heff} \) for a particular bias condition is

\[
\alpha_{Heff} = \sum_j \frac{\mu_{eff}^2}{\mu_j^2} \alpha_{Hj} = \mu_{eff} \sum_j \frac{\alpha_{Hj}}{\mu_j^2}.
\] (2.32)

### Number-Correlated Mobility Fluctuations

There are arguments presented by some \([29, 30]\) that the mobility fluctuation of the carriers may be caused by Coulomb scattering due to the trapped carriers in the oxide. The change in the oxide charge density \( \Delta Q_{ox} \) due to the trapping and detrapping of carriers leads to a change to the flat-band voltage \( \Delta V_{fb} \)

\[
\Delta V_{fb} = -\Delta Q_{ox}/C_{ox}
\] (2.33)

This then leads to a change in the drain current \( \Delta I_D \)

\[
\Delta I_D = \frac{\partial I_D}{\partial V_{fb}} \Delta V_{fb} + \frac{\partial I_D}{\partial \mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \Delta Q_{ox}
\] (2.34)

which simplifies to

\[
\Delta I_D = -g_m \Delta V_{fb} + \frac{\partial I_D}{\partial \mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}} \Delta Q_{ox}
\] (2.35)

since \( \frac{\partial I_D}{\partial V_{fb}} = \frac{\partial I_D}{\partial V_{GS}} = -g_m \). Defining a coupling constant

\[
\alpha = \frac{1}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial Q_{ox}}
\] (2.36)

gives

\[
\Delta I_D = -g_m \Delta V_{fb} + \alpha I_D \mu_{eff} \Delta Q_{ox}.
\] (2.37)

In terms of purely the change in flat-band voltage, \( \Delta V_{fb} \), the change in the drain current is

\[
\Delta I_D = -g_m \Delta V_{fb} - \alpha I_D \mu_{eff} C_{ox} \Delta V_{fb} = -(g_m + \alpha I_D \mu_{eff} C_{ox}) \Delta V_{fb}.
\] (2.38)
The drain current noise power spectral density thus follows [5]:

\[ S_{lD} = [g_m^2 + (\alpha I_D \mu_{eff} C_{ox})^2] S_{Vfb} \]  

(2.39)

where the first term inside the brackets represents the contribution of the carrier number fluctuation, and the second term is the contribution due to the number-correlated mobility fluctuation.

### 2.4.3 Impact of Substrate Voltage on 1/f Noise

In many cases, it has been observed in PMOS devices that when a substrate bias, \( V_{BS} \), is applied to the substrate which forward biases the substrate-source junction, there is a decrease in 1/f noise [31, 32]. The reverse is true when the substrate-source junction is reverse biased. The substrate effect on the 1/f noise in NMOS devices appears to be insignificant, except in weak inversion [33, 34].

This may be explained by the change in the depletion capacitance, \( C_d \), as a function of the substrate voltage, increasing when forward biased and decreasing when reverse biased. This effects the 1/f noise as can be seen from Eq (3-23) [5]. Another explanation is that the substrate bias effects the distance between the oxide charges and channel carriers, thus varying the Coulombic interaction.

### 2.4.4 Input Referred Noise

The discussion of 1/f noise in MOSFETs in the preceding sections has mostly centered on that of the drain current. In some cases, it is more convenient to refer this information to the input noise seen at the gate. As the gate voltage itself, being fixed, does not generate this noise, this drain current noise that is referred to the input gate voltage is called the input referred gate noise. It is calculated from the drain noise as

\[ S_{V_G} = \frac{S_{lD}}{g_m^2} \]  

(2.40)
The equivalent gate voltage noise due to number fluctuation is thus

\[ S_{VG} = \frac{q^2k_BT\lambda N_t}{WLC_{ox}^2} \left[ 1 + \frac{\alpha\mu_{eff}C_{ox}I_D}{g_m} \right]^{2} \frac{1}{f} \]  

and the equivalent gate voltage noise due to mobility fluctuation is

\[ S_{VG} = \frac{q\alpha\mu_{HL}}{WLC_{ox}} \frac{1}{f}. \]

**2.4.5 Summary**

The MOSFET noise equations discussed in the previous sections will be useful in verifying the scaling trends and bias dependences in advanced MOSFETs. Although originally derived for Si-SiO₂ MOSFETs, the equations are expected to still work with the simple substitution of the appropriate material parameters of the alternative materials. In addition, after measured noise data is available, the difference in the gate bias dependence of the noise in the number fluctuation and mobility fluctuation models will give helpful hints as to which mechanisms are dominant in the various advanced MOSFETs studied in this thesis.
Chapter 3

Motivation to Go Beyond Si-SiO₂

During the first half-century since the Si-SiO₂ MOSFET was invented by Labate, Kahng and Atalla at Bell Labs, the trend has been almost entirely focused on scaling down its size. From gate lengths of several micrometers, the MOSFET currently has shrunk to only a few tens of nanometers in feature size.

3.1 Advantages of Scaling

The scaling of MOSFETs is driven by several advantages. A smaller MOSFET allows far more transistors to be packed into a single chip, thus increasing processing power within the same area, or maintaining the same functionality with a smaller chip area. The reduced chip size allows more chips to be packed onto a single semiconductor wafer. Since production costs for a wafer are relatively fixed, this results in more chips produced at the same cost, thus lowering the cost per chip.

Over the past three decades, the number of transistors per chip has doubled every two to three years once a new technology node is introduced (Figure 3.1. As an example, the number of MOSFETs in a microprocessor fabricated in a 45 nm technology is twice as many as that in a 65 nm technology chip. This doubling of the transistor count is commonly referred to as Moore’s Law, in honor of Gordon Moore who first observed this in 1965 and predicted its continued trend [35].

Another advantage of smaller transistors is the increase in the switching speed and
increase in frequency for amplifiers. This is attributable to the smaller dimensions so carriers don’t have to move as far, and second, to the resulting reduction in the gate capacitance. This latter result can be illustrated by noting that typically constant scaling is assumed to occur in all dimensions, so the gate length, width, and oxide thickness are reduced in the same proportion. This retains the same gate resistance, but the gate capacitance is governed by the equation

\[ C_{gate} = \varepsilon_{ox} \frac{A_{gate}}{t_{ox}} \]  

(3.1)

and is thus reduced by the size scaling in the same proportion. Hence, the RC delay of the transistor is also scaled by the same dimensional scaling factor.
3.2 Disadvantages of Scaling

At the level of scaling that is used today, it turns out that a decrease in device switching is undermined by the delay in the interconnects, so the continued overall increase in chip speed has virtually disappeared. Furthermore, as the devices approach atomic and quantum levels in size, normal operation of the MOSFETs starts to be hindered by physical limits and quantum effects, such as tunneling.

Scaled devices start to experience short-channel effects, which essentially result from the shorter channel length, and include channel length modulation, carrier velocity saturation, ballistic transport, and similar effects that lead to undesirable secondary effects, like hot-carrier effects that negatively impact device reliability and operation [25, 26]. Another consequence of shorter channel lengths is drain induced barrier lowering or DIBL, where the proximity of the drain contact to the gate contact gives the drain voltage significant control of the potential in the channel. Short-channel effects are discussed further in the next section.

In order to combat drain-induced barrier lowering, the MOSFET junctions have become more complex, including using higher doping levels, making the junction regions shallower, using "halo" doping and others. In order to keep these features in the finished device, annealing has to be reduced or there is risk of these added features being reduced or completely eliminated by impurity diffusion. The annealing process originally used to heal lattice damage and defects will thus not be able to complete it’s intended job, leading to MOSFETs with higher levels of material and interface defects.

The gain of a MOSFET depends on its transconductance, which in turn depends on carrier mobility. As the channel length is decreased, the increase in the electric field along the channel and the increase in the doping levels both lead to lower mobility. Hence the device gain is effectively reduced.

The scaling of the gate oxide thickness leads to the dielectric layer being very thin, on the order of one nanometer. At this thickness, quantum mechanical tunneling of the carriers through the dielectric barrier is significant. This leads to increased gate leakage, which then leads to increased power consumption.
In addition, the thin oxides are subject to reliability degradation, and as a result, the operating gate voltage has to be reduced to avoid dielectric breakdown. In order to maintain the performance of the device, the threshold voltage of the MOSFET has to be reduced as well, leading to a reduction in the voltage swing between complete device turn-off and complete device turn-on. Typical circuit designs result in a compromise between the saturation current in the on-state and the low junction leakage current in the off-state. This results in subthreshold leakage that is quite significant, which leads to further increased power consumption.

All these increases in power consumption by ever smaller devices, in conjunction with the higher density of having more of them packed into the same space, inevitably leads to substantial localized heat generation. In general, higher temperatures not only negatively impact device and circuit performance, but more importantly, result in reduced device reliability and lifetimes.

The smaller devices also lead to significant process challenges, as the total number of atoms that contribute to the operation of the MOSFET is reduced. This means that any process variation in the manufacture of the device may lead to variations in the physical device parameters. These variations not only affect the device dimensions like channel length, device width, junction depth, oxide thickness, etc, but also the number of dopants and their locations. Since there are a fewer number of atoms involved, the statistical variations become a bigger percentage of the physical device parameters. This larger uncertainty forces circuit designs which accommodate a wider range of individual MOSFET device parameters, but simultaneously produces a smaller range of operating parameters, such as supply voltage, on/off current, etc.

3.3 Short Channel Effects

For short-channel MOSFETs in the saturation region, the $I_D - V_D$ characteristics are no longer parallel to the horizontal axis, but exhibit a positive slope (i.e. there is no true saturation current). This slope increases as the channel is shortened through channel length modulation as explained in Section 2.2. The so-called Drain-Induced-Barrier-Lowering (DIBL) effect resulting from the proximity of the drain contact to
the gate contact gives the drain voltage a significant proportion of control of the channel. This reduces the threshold voltage and increases the off-current if a high drain bias is applied [25, 26].

During operation, short-channel MOSFETs may experience higher levels of degradation processes like hot-carrier effects. This will be discussed in detail in Chapter 5 on device reliability.

Techniques employed to combat short-channel effects include: decreased source/drain junction depth, increased channel doping, decreased oxide thickness, decreased supply voltage, etc. The amount of increase or decrease in these device parameters is governed by scaling rules involving a common multiplicative factor, effectively maintaining a constant electric field.

These techniques however, have several undesired side effects. At higher doping concentration for instance, there is mobility degradation due to higher fields and more impurity scattering. Decrease in junction depth leads to higher source/drain resistances, when it is actually desired to reduce them.

3.4 Impact of Scaling on Low-frequency Noise

The impact of scaling on low-frequency noise is quite significant. The normalized drain current noise power spectral density is inversely proportional to the gate area, so scaling leads to higher 1/f noise. This is intuitive as in a channel with a fewer number of total carriers, any fluctuation of the carriers will be a larger fractional proportion of the total.

Dimensionally considered, thinner oxides have the opposite effect, resulting in better noise performance. However, when the decreased trap population is put into play, the standard deviation in the number of traps among an ensemble of devices will adversely effect it. A trapless oxide may lower 1/f noise initially, but trap generation during operation due to hot carriers for instance, may raise it during its use.

In ultrashort devices, ballistic transport of the carriers may occur, which means a reduction in carrier scattering, thus in theory offering the possibility of reduced 1/f noise. However, the energy attained by these carriers when they reach the drain side
may become quite large, and damage to the drain region is caused when collisions with the lattice or oxide occur, leading to higher noise after some period of operation.

### 3.5 Alternative Materials

Si-SiO\textsubscript{2} has been used almost exclusively as a near-perfect semiconductor-dielectric combination for MOSFETs over the past three decades. This is largely due to SiO\textsubscript{2}'s great passivation properties with the silicon interface, however the limits on these devices imposed by short-channel effects has led researches to investigate other materials for the bulk semiconductor channel and new dielectric materials for MOSFETs. For instance, the higher hole mobility of germanium has placed it as a leading candidate for future PMOS transistors. Insulating materials with dielectric constants higher than silicon dioxide, like hafnium oxide, provide a thicker barrier against tunneling while maintaining the same capacitance. Carbon nanotubes offer the possibility of ballistic carrier transport with much lower kinetic energy and lower oxide damage from hot carriers.

These various materials, and their combinations, will have different properties, resulting in 1/f noise performance that differ from those observed in Si-SiO\textsubscript{2} based devices. The 1/f noise behavior under hot-carrier stress in these devices may prove particularly useful in providing efficient predictions about device reliability.

#### 3.5.1 Alternative Bulk Channel Materials

Germanium and III-V semiconductors are attractive as alternative bulk materials, largely because of their superior carrier mobilities, in particular that of holes ($\mu_h$) for Ge and that of electrons ($\mu_e$) for the III-V semiconductors. Table 3.1 shows the electron and hole mobilities for various semiconductors doped at $10^{15}$ cm$^{-3}$.

**Germanium**

Germanium has long been considered an excellent semiconductor bulk material for MOSFETs due to its high carrier mobilities, but has been limited mainly by lack of
CHAPTER 3. MOTIVATION TO GO BEYOND SI-SIO₂

Material | $\mu_e$ (cm²V⁻¹s⁻¹) | $\mu_h$ (cm²V⁻¹s⁻¹)
--- | --- | ---
Si | 1500 | 450
Ge | 3900 | 1900
GaAs | 8500 | 400
InAs | 30000 | 480
InP | 5000 | 180

Table 3.1: Electron and hole mobilities for various semiconductors doped at $10^{15}$ cm⁻³ [36].

A suitable dielectric material (GeO₂ being water soluble) that would result in a low semiconductor-dielectric interface trap density for proper MOSFET operation. In recent years, the search for a semiconductor bulk material alternative to silicon has brought germanium back into the limelight.

Although there are Ge PMOSFETs that have been able to take advantage of the higher Ge hole mobility [37, 38], Ge NMOSFETs have encountered some obstacles. The problem arises from poor dopant incorporation in Ge which results in large source/drain (S/D) resistance. Using metal to reduce this resistance has also encountered difficulties due to strong surface Fermi level pinning. Recently, Kobayashi et al [39] were able to achieve Fermi level depinning by using a thin SiN layer, so Ge NMOSFETs utilizing its superior electron mobility are expected to be produced soon.

Current research is also focusing on finding a suitable dielectric material to be paired with the germanium bulk substrate. Potential candidates include hafnium oxide (HfO₂) and native germanium dioxide (GeO₂) with a Al₂O₃ cap to protect it from the environment [37, 38].

III-V Compound Semiconductors

III-V semiconductors have long been commonplace in optoelectronic applications like lasers and lighting, and mobile applications, such as power amplifiers in cell phones. Recently, similar to the case with germanium, several III-V compound semiconductors are being considered as alternatives to silicon mainly because of their superior electron mobilities, particularly for use as the channel material in NMOSFETs. High electron mobility transistors (HEMTs) have been successfully grown and demonstrate
significant performance enhancement in analog applications [40]. However, beyond performance demonstration purposes, the nonplanar design and Schottky gate electrodes of HEMT structures with limited forward bias operation are impractical for low power digital circuits due to limited scalability and large leakage currents.

GaAs substrate MOSFETs with GdGaO/Ga$_2$O$_3$ gate dielectric stacks and In$_{0.3}$Ga$_{0.7}$As channel layers have been successfully fabricated and show I-V characteristics superior to those of silicon [41, 42]. However, the success of the GaAs-Ga$_2$O$_3$ interface (including Fermi-level unpinning) may not be sufficiently stable over long periods and this passivation may not necessarily extend to high indium-containing channels. Further studies on this matter are ongoing, in addition to continued searches for suitable dielectric materials. Similar techniques to those for Ge NMOSFET Fermi-level depinning of the source/drain metal contacts are currently being explored for III-V devices as well.

Challenges to the success of III-V MOSFETs in replacing silicon-based MOSFETs include the commercial non-practicality of using molecular beam epitaxy (MBE) to grow these devices, and the difficulty of integrating III-V channels onto silicon substrates for full CMOS integration.

The non-availability of III-V channel MOSFETs to this research work at this time unfortunately excludes these devices from the 1/f noise characterization work in this thesis, and only a speculation can be made regarding the noise behavior of these devices. Due to the compound composition of these materials, other scattering mechanisms, like alloy and particularly polar optical phonon scattering come into play [27, 36]. This will likely result in III-V channel MOSFETs showing the dominance of the mobility fluctuation mechanism in the 1/f noise behavior.

3.5.2 Low-dimensional Carbon-based Channel Materials

In an effort to reduce short channel and oxide interface scattering effects, there has been an explosion of research into devices utilizing low-dimensional carbon-based channel materials like carbon nanotubes (CNTs) and graphene. Graphene is essentially a two-dimensional (2-D) single atomic layer carbon graphite sheet of sp$^2$-bonded
Carbon atoms that are densely packed in a honeycomb crystal lattice. Carbon nanotubes are graphene sheets rolled up into one-dimensional (1-D) tubes (Figure 3.2) [43].

![Figure 3.2: A 2-D graphene rolls up into a 1-D nanotube [44].](image)

**Carbon Nanotubes**

Depending on the chirality of its structure, a carbon nanotube can be either metallic or semiconducting (Figure 3.3). For semiconducting nanotubes, the bandgap is determined by the diameter of the tubes [43]. The chirality of a carbon nanotube is basically the spiral configuration or "twist" along the axis of the rolled-up tube and is described by the chiral vectors \(m\) and \(n\), defined by

\[
R = ma_1 + na_2
\]  

(3.2)

where \(m, n\) are integers.

The main advantage of using carbon nanotubes is their 1-D structure. In a 1-D material, charge transport is enhanced because carriers can only scatter forward or
Figure 3.3: The chirality of carbon nanotubes determine whether the material is metallic or semiconducting. The chiral vectors $m$ and $n$ define the chirality of the material.

backward, thus precluding much more likely low angle scattering that limit the mobility and transport in 2-D and 3-D materials. Ballistic transport is thus far more probable in 1-D wires than in 2-D quantum wells or 3-D bulk systems. This investigation of carrier transport was first observed and discussed by Sakaki [45] in 1980 using GaAs/AlGaAs quantum wire structures. Growing 1-D structures using traditional semiconductor materials however, requires using molecular beam epitaxy (MBE), followed by several very costly and time-intensive etching and regrowth processes which make mass-producing such structures commercially impractical.

Carbon nanotubes, on the other hand, are grown using much simpler methods, such as arc-discharge [46] and chemical vapor deposition (CVD) [47]. CVD in particular, is much more commercially viable and compatible with the silicon processing [48]. This, together with the theoretical advantages of 1-D transport properites, make
carbon nanotubes attractive as a channel material for a FET device alternative to silicon.

To construct such a CNTFET device, the simplest configuration is to have a single carbon nanotube placed on top of a Si-O₂ layer grown on top of a doped silicon layer, which acts as a back gate. Metal contacts are added to form the source and drain contacts of the device [49]. The choice of palladium (Pd) as the metal contact is currently popular due to the desire to have as ideal a Schottky barrier as possible to the carbon nanotube [50] (Figure 3.4). Carrier injection into the channel then occurs by tunneling through the Schottky barrier (Figure 3.5).

![Diagram of CNT-FET structure]

Figure 3.4: A simple CNT-FET structure [51].

A carbon nanotube field effect transistor (CNTFET) holds several advantages over a conventional Si-SiO₂ FET. As mentioned above, carrier transport in CNTs is one-dimensional, allowing for a higher probability of ballistic transport. On the process side, chemical synthesis of CNTs provides atomic precision of key device dimensions,
CHAPTER 3. MOTIVATION TO GO BEYOND SI-SIO$_2$

Figure 3.5: These figures show the qualitative response of the nanotube conduction and valence bands on the gate voltage, one at the on-state and the other at the off-state. The drain-source voltage is fixed at a negative value. Carrier injection into the channel occurs by tunneling through the Schottky barrier [52].

thus better control of resulting device electrical parameters. All bonds in the material are stable, satisfied and covalent, thus lowering the presence of defects. A CNTFET also has a symmetric band structure, which allows for identical electron and hole transport properties, resulting in balanced NMOS and PMOS devices, a very significant circuit advantage where PMOS devices are approximately four times larger than NMOS devices in order to have equal on currents and on/off switching characteristics in today's silicon-based CMOS logic gates (Figure 3.6), and also advantages in the fabrication process where uniformity greatly simplifies the process flow.

As glowing as the advantages of CNT are over silicon as a MOSFET channel material, there are several challenges that must still be addressed in terms of commercial viability. In general, making CNTs of uniform diameters, chirality, and lengths are
Figure 3.6: The figure shows a comparison between a CNTFET and a conventional Si-SiO2 FET. To allow for a better comparison, the drain currents are normalized by gate capacitance [53].

still beyond perfection. Also, due to the sensitivity to defects of the 1-D transport of carriers in carbon nanotubes, the noise behavior is expected to be quite high, as will be discussed in Chapter 4, which may not only disqualify their use as a channel material for analog applications, but limit their viability as digital MOSFETs as well.

Graphene

As described above, graphene is a planar single atomic layer thick sheet of sp2-bonded carbon atoms that are densely packed in a honeycomb crystal lattice. Several layers of graphene form the well-known carbon graphite. As such graphene is commonly referred to as "monolayer graphite".

Intrinsic graphene is classified as a semi-metal (or alternatively, a zero-gap semiconductor). The E-k relation was found to be linear for low energies near the six
corners of the two-dimensional hexagonal Brillouin zone, leading to zero effective mass for electrons and holes [54]. Interestingly, due to this linear dispersion relation at low energies, electrons and holes near these six points behave like relativistic particles described by the Dirac equation for spin 1/2 particles, which may lead to useful condensed matter physics experiments.

Han et al. [55] in 2007 investigated the electronic transport in lithographically patterned graphene ribbon structures where the lateral confinement of charge carriers creates an energy gap near the charge neutrality point. Individual graphene layers are contacted with metal electrodes and patterned into ribbons of varying widths and different crystallographic orientations. It was found that the energy gap scales inversely with the ribbon width, thus demonstrating the ability to engineer the band gap of graphene nanostructures by lithographic processes.

Experimental results show that graphene has a high electron mobility at room temperature, with reported values in excess of $15,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [56]. The symmetry of the experimentally measured conductance indicates that the mobilities for holes and electrons should be nearly the same [54]. This makes graphene an extremely attractive alternative channel material for both NMOSFETs and PMOSFETs. Novoselov et al. [57] in 2004 were able to demonstrate a working graphene PMOSFET, albeit with a poor on/off ratio of 30. Recently in 2009, Wang et al. [58] at Stanford University were able to produce working graphene NMOSFETs.

A huge challenge to the commercial viability of graphene MOSFETs is the practicality of the graphene synthesis itself. For example, the most common technique used by researchers is the so-called "mechanical exfoliation" from graphite, a fancy name for the method of "Scotch-tape-peeling" famously used by Novoselov et al. [57]. Recently, chemical vapor deposition (CVD) synthesis of graphene was achieved by Reina et al [59] and Kim et al [60] which may prove more practical.

Another challenge is the sensitivity of the material bandgap to the graphene dimensions. A viable CMOS technology must allow for scaling, and it is not yet clear that there exists a suitable solution to this.

Noise in graphene is found to be lower in general than that of carbon nanotubes, most likely owing to the extra degree of freedom in dimensionality, and comparable
Graphene was found not to be immune to the problems of increased noise with the scaling down of dimensions inherent in all other bulk semiconductors, but Lin et al. from IBM were able to suppress 1/f noise in graphene devices by using a bilayer channel structures.

3.5.3 Alternative Dielectrics

As discussed above, the scaling of the gate oxide thickness leads to the dielectric layer being very thin, such that quantum mechanical tunneling of the carriers through the dielectric barrier is significant. This leads to increased gate leakage, which then leads to increased power consumption. This motivates the search for insulating materials with dielectric constants higher than silicon dioxide, so as to provide a thicker barrier against tunneling while maintaining the same capacitance. Typically, the dielectric materials are grown on the semiconductors by atomic layer deposition (ALD). In this section, a short discussion will focus mainly on dielectrics suitable for MOSFETs with silicon channels.

Wilk et al. [63] summarize that the required properties of alternative gate dielectrics must consider (a) permittivity, bandgap, and band alignment to silicon, (b) thermodynamic stability, (c) film morphology, (d) interface quality, (e) compatibility with the current or expected materials to be used in processing for CMOS devices, (f) process compatibility, and (g) reliability. Many dielectrics appear favorable with respect to some of these criteria, but very few materials are promising with respect to all of these considerations. Table 3.2 shows the dielectric constants and bandgaps of some of the materials being considered, and Figure 3.7 shows the band alignments for various dielectric materials.

Currently, hafnium silicate (HfSiON) and hafnium oxide (HfO₂) are the most widely used among the alternative dielectric materials, having satisfied the widest range of dielectric property requirements enumerated above. The main trade-off between these two materials is that hafnium oxide has the higher dielectric constant, but hafnium silicate has the lower interface trap density [63], which reduces Fermi-level pinning and may result in lower 1/f noise. The noise properties of MOSFETs using
CHAPTER 3. MOTIVATION TO GO BEYOND Si-SiO₂

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric constant $\kappa$</th>
<th>Bandgap (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>3.9</td>
<td>8.9</td>
</tr>
<tr>
<td>Si₃N₄</td>
<td>7</td>
<td>5.1</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>9</td>
<td>8.7</td>
</tr>
<tr>
<td>TiO₂</td>
<td>80</td>
<td>3.5</td>
</tr>
<tr>
<td>HfSiON</td>
<td>13-20</td>
<td>5.6-6</td>
</tr>
<tr>
<td>HfO₂</td>
<td>25</td>
<td>5.7</td>
</tr>
<tr>
<td>ZrO₂</td>
<td>25</td>
<td>7.8</td>
</tr>
</tbody>
</table>

Table 3.2: Comparison of relevant properties for high-$\kappa$ candidates [63].

Figure 3.7: Band alignments with respect to silicon of various high-$\kappa$ dielectric materials [63].

both of these dielectric materials are described in Chapters 4 and 5.
Chapter 4

Noise Characterization of MOSFETs

4.1 Noise Measurement Setup

The measurement of noise is a very complex and sensitive process and considerable care and precaution must be taken to ensure that the measured noise is the targeted one and not contributed from sources external or spurious to the device. Compared to the DC bias currents applied to the device, the noise current is very small, typically a few picoamperes compared to the milliamperes of bias current (nine orders of magnitude smaller). As such, it may not only be overwhelmed by the DC response of the device, but also by external noise sources from electronic equipment and the environment, as well as internal noise sources from the device itself.

In desiring accuracy for any measurement of signals that are stochastic in nature, the average of multiple measurements must be taken. For low frequency noise measurements, each bias condition may thus require several minutes to complete, and in this time period, many extraneous noise disturbances may occur. The idea that any of these spurious disturbances will eventually be averaged out is incorrect, as noise power is effectively a sum of squares (hence all positive values), and therefore the situation where a positive disturbance may be compensated by a negative one by the law of averages of a large number of samples will never occur. As a consequence,
one must ensure as much as possible that the occurrence of any such disturbance be detected and the current set of measurements be invalidated and repeated. As easy as this may sound to simply physically observe a single set of measurements at a particular bias point for the entire run, it becomes increasingly difficult for measurements requiring multiple bias points where the process is automated and the entire run lasts for hours. Analysis of the numerical and graphical data by eyeballing or using computer programs may sometimes catch these incidents but the prevention or minimization of these occurrences is the most efficient way to handle them.

In setting up a noise measurement system, one must be aware that any extraneous noise at the input end of an amplifier has the most damaging effect on the targeted noise signal and so must be minimized. Most of these are due to external noise sources, which in many cases are easy to reduce. At the output of the amplifier, the noise signal will be strong enough so as not to be appreciably affected by external noise sources.

4.1.1 External Sources of Extraneous Noise

In most cases, the noise measurement equipment is located in a room where there are numerous noise-producing sources, like other electronic equipment, lighting, people walking around, etc. The next few sections cover the most common sources of these disturbances and ways to minimize or eliminate them.

Power supply

The power supply provides the DC biases for the device and therefore fluctuations in the supply voltage must be reduced as much as possible. To this end, using batteries for device biasing is the best solution. The drawback is that for measurements that require multiple biases, automation is extremely difficult. To make automation possible, electronic voltage sources may be used as long as they are very well filtered to reduce power line disturbances.
CHAPTER 4. NOISE CHARACTERIZATION OF MOSFETS

Electronic Equipment

Room lighting, especially fluorescent lamps, are strong sources of 60 Hz noise as are other electronic equipment in the room. The 60 Hz noise and its harmonics have a particularly strong presence as it is ubiquitous in the electrical system of the room and the entire building. Cellular phones, radio transmitters, and other similar equipment typically emit disturbances at much higher frequencies, but due to mixing in non-linear elements in the measurement circuits, they may be down-converted and effect the lower frequencies in the range of measurements of interest for this thesis as well.

The ideal situation is to have only the equipment needed for the noise measurements present in the entire room but this is not usually practical in most settings due to space, budget and other user restrictions.

Appropriate shielding is important as a first line of defense against these noise sources. Ideally, a metallic Faraday cage should enclose the whole system to electronically isolate it from the rest of the room. The device-under-test (DUT) should also be placed in a metal-shielded probe station. The amplifier should be situated as close as possible to the device and shielded as well.

Cables connecting equipment boxes to each other act as antenna, which pick up extraneous noise signals. To reduce this problem, the shortest possible lengths of cables should be chosen. One must also take care in not bending the cables, as capacitance variations that result from the physical distortions may affect the measurements.

Mechanical Vibrations

Through the floor, the probe station table, the probe station, and lastly the probes, mechanical vibrations coming from people walking, equipment being moved, pumps and HVAC systems running, etc. are transmitted to the probe contacts, which often result in disturbances in the physical contact with the device pads. This in turn results in disturbing the electrical biases to the device, which ends up as extraneous noise. In addition, vibrations felt by the cables connecting the equipment boxes may result in capacitance fluctuations.
A common way to minimize this is to use a vibration-isolation table for the probe station. It is also recommended to do the measurements at night or other less active hours of the day as the case may be, in order to avoid the situations mentioned above, in addition to reducing electrical disturbances from the turning on or off of electronic or electrical (particularly large motors associated with a clean room) equipment in the room or elsewhere in the building.

4.1.2 Internal Sources of Extraneous Noise

Even though internal noise sources are less obvious, it is no less imperative that they be minimized, especially those that come before the first amplifier stage. To reduce internal noise sources from the electronics, one must use metal film or wire-wound resistors in the circuits involved in the noise measurements. These types of resistors have very little low frequency noise and contribute almost entirely only thermal noise. Needless to say, the amplifier itself should have the lowest possible noise rating. In the case where probes are used to contact the device pads rather than bonding, care should be taken that the contacts are not poor due to damaged probes or insufficient drive-in pressure.

4.1.3 Noise Equipment Setup

The setup used for the noise measurements in this thesis is described here (Figure 4.1). The device is placed inside a Cascade 12K probe station. The biases are supplied by an Agilent 4156C Parameter Analyzer through triax cables. The drain current is then amplified by either a Stanford Research SR560 Voltage Preamplifier or a Stanford Research SR570 Current Preamplifier. The amplifiers have internal filters, which are set to be configured as a bandpass filter with the high frequency point at 10 kHz and the low frequency point at 0.03 Hz (to remove the DC signal). The output of the amplifier is then fed into an Agilent 35670 Spectrum Analyzer, which measures and analyzes the noise signal in the frequency domain, from a range of 0-100 kHz. For the purpose of reducing the signal broadening in the Fast Fourier Transform (FFT) analysis of the spectrum analyzer due to the non-periodicity of the
signal, the Hanning window filter function is used for better frequency resolution. The averaging of the noise measurements is set to at least 25.

The Hanning (not to be confused with Hamming) window is named after Julius von Hann and is a filter of the form

\[
w(n) = 0.5 \left[ 1 - \cos\left(\frac{2\pi n}{N-1}\right) \right]
\]

where \( N \) represents the width, in samples (typically a power of 2), \( n \) is an integer with values \( 0 \leq n \leq N \) [64]. This window function is useful for low frequncy noise measurements where better frequency resolution than some of the other windows is desired but moderate side lobes do not present a problem [5].

For multiple biases, a total run may take several hours, so controlling the Agilent 4156 Parameter Analyzer and the Agilent 35670 Spectrum Analyzer every few minutes can get very tedious and time-consuming. For the measurements in this thesis, a software program written in Microsoft EXCEL Visual Basic was developed to control the Agilent 4156 and Agilent 35670, and run via a computer linked to these two.
equipment boxes through GPIB cables. The program runs through a list of bias conditions, and controls the settings accordingly. The program also manages the data collection from the Agilent 35670 Spectrum Analyzer. The main part of the program is listed in Appendix A.

4.2 Silicon-Silicon Dioxide (Si-SiO$_2$) MOSFETs

Having the material combination with the most extensive research and development, it is not surprising that Si-SiO$_2$ MOSFETs also have the largest number of varieties. Coupled with the uncertainty of the sources of 1/f noise, one would assume that these normally lead to huge variations in the noise behavior also, depending on the features present or not in the devices. As shown by Chang et al [65] however, the major noise characteristics remain roughly the same for a very wide range of Si-SiO$_2$ MOSFETs, allowing one to make generalizations about the noise behavior in these devices.

4.2.1 Bias Dependence

Chang et al [65] tried a variety of bias conditions, with the gate voltage varying from subthreshold to strong inversion, and the drain voltage varying from linear to saturation regions of operation. A summary of the results from their work is discussed below.

NMOSFETs

In their paper [65], it was shown that the NMOSFET noise spectra change very little as the gate bias is varied (Figures 4.2 and 4.3, for a representative 12 x 3 $\mu$m$^2$ NMOSFET). Considering the margin of error to be approximately 10 percent, no consistent gate bias dependence parameters can be extracted from the data.

This independence with gate bias voltage is observed across all types of NMOSFET devices, and suggests that 1/f noise in these devices is due to carrier number fluctuation as opposed to mobility fluctuation. Assuming the device is biased in the linear region of operation, it is shown [65] that the input referred noise is
Figure 4.2: Input referred noise spectra for a representative 12 x 3 μm² NMOSFET in the linear region of operation [65].

\[
S_{V_g}(f) = \left(\frac{q}{C_{ox}}\right)^2 \frac{1}{WLf} \frac{N_T(E_F)}{\gamma}
\]

(4.2)

where \(N_T(E_F)\) is the interface state density per unit energy at the Fermi energy level, and \(\gamma \approx 10^8 \text{cm}^{-1}\) is McWhorter's tunneling parameter. If the trap density is not spatially uniform in the gate oxide, the frequency \(f\) is raised to some power other than 1 which can range from about 0.7 to 1.2.

**PMOSFETs**

PMOSFETs on the other hand, show a very different behavior, and exhibit strong gate voltage dependence in both the linear and saturation regions of operation [65].
Figure 4.3: Input referred noise spectra for a representative 12 x 3 μm² NMOSFET in the saturation region of operation [65].

(Figures 4.4 and 4.5, for a representative 12 x 3 μm² PMOSFET).

This dependence with gate bias voltage is observed across all types of PMOSFET devices, and suggests that 1/f noise in these devices is due to mobility fluctuation, and can be expressed as [65]

\[ S_{V_G}(f) = \left( \frac{q}{C_{ox}} \right) \alpha_H \frac{\alpha_H}{WL} (V_{GS} - V_T). \]  

(4.3)

Comparing the figures for the NMOSFET and PMOSFET devices (Figures 4.2 - 4.5), where both devices are from the same process, it is noted that at certain biases, PMOSFET devices have noise spectra that is 2 or 3 orders of magnitude lower than that of the NMOSFET devices. This difference in noise behavior between
NMOSFET and PMOSFET devices was originally explained by the fact that it is common for PMOSFET devices to be ion-implanted, so they have buried channel conduction, where the mobility fluctuation mechanism dominates [66, 67]. However, this theory was debunked when PMOSFET devices without ion implantations showed similar much lower noise with gate bias dependence as the other PMOSFET devices, and ion-implanted buried channel NMOSFET devices still showed the expected gate-bias-indifferent behavior [65].

When measured under subthreshold gate biases, the noise spectra behavior remained the same for the NMOSFET devices (gate-bias-independent), and for the PMOSFET devices (gate-bias-dependent) [65]. This again supports the theory that the NMOS and PMOS noise mechanisms are completely different.
4.2.2 Temperature Dependence

At low temperatures, electron and hole mobilities, leakage current, and interconnection conductivity improve significantly. Based on these, it was generally believed that the noise would also decrease at lower temperatures, and operation of MOSFETs at low temperatures has been suggested as a way improving the noise performance [65].

To test this, Chang et al [65] also performed low temperature studies of the noise behavior of these devices. It is shown that the NMOSFET noise spectra still had no gate bias dependence at all tested temperatures, and contrary to popular belief, low temperature did not result in a significant decrease of the 1/f noise (Figure 4.6). This supports the McWhorter tunneling model in the carrier number fluctuation theory of noise, which is roughly temperature independent [65].

On the other hand, the PMOSFET devices showed strong gate bias dependence
at all tested temperatures, and the noise behavior varied significantly at low temperatures (Figure 4.7). For the particular device shown in Figure 4.7, the noise starts to display a generation-recombination type of behavior at 20K. This generation-recombination noise is likely caused by the frozen out boron implant, and the peak appears to have moved to lower frequencies at 5K. The significant changes in the noise behavior with respect to temperature of the PMOS devices again support the mobility fluctuation mechanism [65].

### 4.2.3 Gate Area Dependence and Scaling

As shown by Equations (4.2) and (4.3), the 1/f noise performance should be inversely proportional to the gate area. In general, this leads to increased 1/f noise as devices
are scaled down. However, as discussed in Section 3.4, when the oxide thickness is also downscaled, lower noise is expected. At scaling beyond the 65nm node, the SiO₂ layer has become too thin and the gate leakage is significant. The resulting gate leakage current noise adds to the total drain current noise, increasing the total noise of the device. Contaret at al [68] suggested that the influence of the gate leakage current on the total noise could be described by the equation [68]

\[
\frac{S_{I_{D,\text{tot}}}}{I_{D}^2} = \frac{S_{I_{D}}}{I_{D}^2} + \alpha_{D}^2 \times \frac{S_{I_{G}}}{I_{D}^2}.
\]

Their work isolated the effect of the extraneous gate noise on the total noise in a 10 x 10 μm² NMOS with a 1.2nm SiO₂ gate oxide layer (Figure 4.8).
Figure 4.8: Contribution of extraneous gate leakage noise on the total noise in a 10 x 10 \( \mu \text{m}^2 \) NMOS with a 1.2nm SiO\(_2\) gate oxide layer with \( V_d = 50 \text{mV} \) [68].
4.3 Silicon-HfSiON MOSFETs

As discussed in Section 3.5.3, the continued scaling of Si-SiO₂ MOSFETs has led to thinner and thinner SiO₂ thicknesses, which results in unacceptably large gate leakage currents. Current efforts have focused on a search for suitable dielectric replacements with a higher dielectric constant, \( \kappa \), than that of SiO₂ (\( \kappa = 3.9 \)), so the gate capacitance is maintained with thicker dielectrics, thus reducing gate leakage due to tunneling.

Hafnium oxide (HfO₂), with a dielectric constant of 20-25, is one of the materials being studied. However, the high trap density associated with using HfO₂ as a silicon MOSFET dielectric results in about three orders of magnitude higher 1/f noise ([69]). An alternative material is hafnium silicate (HfSiON), which has lower defect densities than HfO₂ [69-71], but unfortunately, has a smaller dielectric constant of 10-14. Estimates of Si-HfSiON interface trap densities range from \( 10^{11} \) to \( 10^{11} \) cm\(^{-2}\)eV\(^{-1}\) compared to \( 10^{10} \) cm\(^{-2}\)eV\(^{-1}\) for a good Si-SiO₂ interface [63, 71].

Si-HfSiON MOSFETs exhibit threshold voltage instability due to charging and discharging of traps in the material through tunneling [72]. Characterizations have also been conducted on the 1/f noise behavior of these devices, which have critical implications in analog performance and at the same time provide important interface information [70]. A numerical noise model was suggested by Liu et al [73] showing the impact of high-\( \kappa \) dielectrics on the 1/f noise in MOSFETs and the scaling implications.

4.3.1 Device Fabrication

The Si-HfSiON MOSFETs studied in this work were fabricated at SEMATECH Corp, Texas, and have gate widths of 10 microns with gate lengths that range from 0.1 to 1 \( \mu m \) [74]. The MOSFET channels were doped at a density of \( 10^{18} \) cm\(^{-3}\) with a halo structure. Starting with the Si(100) substrate, the 2nm HfSiON gate stack is deposited via atomic layer deposition (ALD). The interfacial SiO\(_2\) layer thickness was found to be 1.0 nm. A TiN layer was then deposited by ALD and followed by a poly-Si CVD capping layer on top. The subsequent fabrication steps followed those in a standard CMOS gate first flow, which incorporated a 1050 °C spike anneal.
[74]. Figure 4.9 shows the gate stack structure. The devices are designed for a supply voltage of about 1V.

<table>
<thead>
<tr>
<th>Poly-Si cap</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiN</td>
</tr>
<tr>
<td>2 nm HfSiON</td>
</tr>
<tr>
<td>~ 1 nm SiO$_x$</td>
</tr>
<tr>
<td>Si (100)</td>
</tr>
</tbody>
</table>

Figure 4.9: Si-HfSiON gate stack structure [74].

4.3.2 1/f Noise Characteristics

Due to the threshold voltage instability, extra care needed to be taken when performing the noise measurements. Since the measurements took at least several minutes to complete, the devices were allowed to settle after applying the biases, and before the noise measurements were commenced. To maintain consistency, the range of devices with various gate lengths was chosen from a single die. Due to the limits imposed by the threshold voltage instability on noise measurements at low gate biases, and because for comparison purposes it is sufficient to use above-threshold gate biases, the measurements focused on the bias region above threshold. For better characterization results, the drain bias was kept low at 0.1V.
Figure 4.10 shows the measured $I_d-V_g$ curves for the NMOS and PMOS devices with various gate lengths plotted against the applied gate biases with drain voltage at 0.1V. Figure 4.11 shows the normalized measured drain current $1/f$ noise characteristics of Si-HfSiON NMOS and PMOS devices with various gate lengths plotted against the gate overdrive bias ($V_g - V_t$), with the drain voltage fixed at 0.1V. Compared with conventional Si-SiO2 NMOS devices, the noise level is about 2 orders of magnitude higher [75].

Figure 4.10: Si-HfSiON MOSFET $I_d-V_g$ vs $L_g$ with $V_d$ at 0.1 V for a) NMOS and b) PMOS devices, showing inverse dependence on gate length.

Figure 4.12 shows the measured drain current noise versus drain current plot for the various gate length devices. Both Figures 4.11 and 4.12 show that the measured noise level is inversely proportional to the gate length, and also to the applied gate biases. This is the expected behavior in the unified number and mobility fluctuation model [70]. Figure 4.13 shows the measured $g_{m}^2/I_d^2$ vs $I_d$ plot for the devices. It can be observed in Figures 4.12 and 4.13 that both $S_{I_d}/I_d^2$ vs $I_d$ and $g_{m}^2/I_d^2$ vs $I_d$ plots show an inverse dependence to $I_d$, again consistent with the unified flicker noise model [75]. It can be further noted that the $S_{I_d}/I_d^2$ vs $I_d$ data follow the $g_{m}^2/I_d^2$ vs $I_d$ data here, once again as expected [75].
Figure 4.11: Si-HfSiON MOSFET $S_{i_d}/I_d^2$ vs overdrive gate bias $V_{g-V_t}$ for a) NMOS and b) PMOS devices at $V_d = 0.1$, showing inverse dependence on gate bias.

Figure 4.12: Si-HfSiON MOSFET $S_{i_d}/I_d^2$ vs $I_d$ for a) NMOS and b) PMOS devices showing inverse dependence on the drain current, consistent with the unified flicker noise model.

Substrate Bias Dependence

Figure 4.14 shows the $I_d$-$V_g$ curves for typical NMOS and PMOS 10$\mu$m $\times$ 0.4$\mu$m devices with varying substrate biases, and Figure 4.15 shows their measured 1/f noise
Figure 4.13: Si-HfSiON MOSFET $\frac{g_m^2}{I_d^2}$ vs $I_d$ for a) NMOS and b) PMOS devices showing inverse dependence on the drain current, consistent with the unified flicker noise model. It is also noted that the $S_{I_d}/I_d^2$ vs $I_d$ data follow the $g_m^2/I_d^2$ vs $I_d$ data characteristics under these substrate biases. For both NMOS and PMOS devices, the effect of the substrate bias on 1/f noise if any, is quite small, which is consistent with conventional Si-SiO$_2$ devices [33].

### 4.3.3 Summary of 1/f Noise Behavior of Si-HfSiON MOSFETs

The consistency of the noise behavior of Si-HfSiON MOSFETs to that of Si-SiO$_2$ MOSFETs is not surprising, given that they still share the same channel material and there likely is a very thin SiO$_2$ layer at the interface. As expected, the noise level of Si-HfSiON MOSFETs is higher than that of Si-SiO$_2$ MOSFETs due to the higher trap density at the Si-HfSiON interface, but the bias dependence behavior is similar.
CHAPTER 4. NOISE CHARACTERIZATION OF MOSFETS

Figure 4.14: Si-HfSiON MOSFET $I_D-V_G$ curves with substrate bias $V_b$ for a) NMOS 10$\mu$m x 0.4$\mu$m and b) PMOS 10$\mu$m x 0.4$\mu$m devices.

Figure 4.15: Si-HfSiON MOSFET - effects of substrate bias on $S_{I_D/I_D^2}$ vs $V_G-V_t$ with a) no impact on the 10$\mu$m x 0.4$\mu$m NMOS device, and b) minimal impact 10$\mu$m x 0.4$\mu$m PMOS.

4.4 Germanium-Hafnium Oxide (Ge-HfO$_2$) MOSFETs

In this section, the low frequency noise of germanium pMOSFETs with hafnium oxide gate dielectric and P+ poly-Si gate electrodes is investigated. So far, all the
experimental data of Ge MOSFETs has focused on the mobility improvement over Si MOSFETs and the properties of the gate dielectric [37, 77, 78]. There has been no experimental data on the 1/f noise properties of Ge MOSFETs until the research work in this thesis. In this section, the characterization of Ge MOSFET noise is discussed, along with its bias-, and scaling-dependence. Temperature-dependence, due to the nature of the device behavior, will be discussed in Section 5.4.
### 4.4.1 Ge-MOSFETs

Germanium MOSFETs have recently shown great promise as a potential device technology for CMOS logic [37, 77–79]. Very large enhancement of the DC current drive and mobility has been reported [37, 78]. The higher mobility and larger transconductance potentially leads to a higher $f_T$ for improved RF/mixed-signal applications. The larger current drive of Ge MOSFET improves the amplification (gain) performance, and the higher $f_T$ increases the bandwidth. However, the noise figure is crucial for low noise amplifiers, and 1/f noise is a key factor in determining the phase noise of voltage controlled oscillators (VCOs). As one of the most sensitive probes of the semiconductor-dielectric interface is the measurement of the 1/f noise spectra of the device, study of the 1/f noise properties will provide insights into the interface properties (interface and bulk traps) of the high-k/Ge interface. Estimates of Ge-HfO$_2$ interface trap densities range from $10^{11}$ to $10^{11}$ cm$^{-2}$eV$^{-1}$ compared to $10^{10}$ cm$^{-2}$eV$^{-1}$ for a good Si-SiO$_2$ interface [80]. In this section, initial experimental measurements of 1/f noise of Ge pMOSFETs with an HfO$_2$ gate dielectric and P+ poly-Si gate electrode will be discussed.

### 4.4.2 Device Fabrication

Device fabrication followed a process described in Shang et al. [37]. Ge pMOSFETs were fabricated starting with SOI or SGOI wafers whereupon a STI process is performed to form SGOI active regions. A strained-germanium (s-Ge) channel layer is then created by high temperature oxidation. Conventional CMOS processes are then used for the gate stack formation, S/D implants, and metal contacts. For the devices measured, the HfO$_2$ thickness is 6.5 nm (Figure 4.16).

### 4.4.3 1/f Noise Characteristics

Ge pMOSFETs of gate lengths $L_g = 0.4, 0.7, 1, 2, 5, 10 \, \mu m$ and gate widths of $W_g = 0.4, 1, 10, 20, 50, 100 \, \mu m$ were measured for this study. The device IV characteristics show that there is very small gate leakage (Figure 4.17). Drain current noise was
measured in a shielded temperature controlled probe station using the standard noise measurement setup as discussed in Section 4.1.

![Graph](image)

Figure 4.17: $I_d$ vs $V_g$ curve for a 10µm gate width by 5µm gate length Ge pMOSFET at $V_d=50$mV, showing hysteresis.

The measured noise spectrum for a 10µm \times 1µm is shown in Figure 4.18. The normalized drain current noise spectral density $S_N = S_{d}^2/I_d^2$ at 10 Hz is used for the scaling-, bias-, and temperature-dependence analyses. The Ge MOSFETs were found to have $S_N$ values that are about two orders of magnitude larger than conventional Si-SiO$_2$ MOSFET devices. The larger 1/f noise for Ge MOSFET is probably due to two contributions, the first is the germanium crystal defects coming from the fact that the germanium channel is strained by the lattice mismatch, and the second is higher trap density at the Ge-HfO$_2$ gate dielectric interface, given that HfO$_2$ is not a native oxide to Ge, as the case is with Si-HfO$_2$. In Si-HfO$_2$ and other silicon-hi-$\kappa$ dielectric pairings, this high density of interface traps has led to Fermi-level pinning at the gate.
and has led to higher 1/f noise in MOSFETs of such material combinations, as discussed in Section 4.3. Here, it is suggested that given the absence of further interface studies of Ge-HfO₂, the higher 1/f noise in the Ge-HfO₂ MOSFETs, is evidence of the higher density of interface traps. In cases such as this, 1/f noise characterization provides a convenient tool for early analysis of material interfaces. As for the Fermi-level pinning at the gate, it is fortunate that because of the valence band offset, the Ge channel allows the \( V_{th} \) of HfO₂/poly Si PMOSFETs to be lowered to the appropriate \( V_{th} \) for high performance CMOS technology [37].

Figure 4.18: 1/f noise spectral density for a 10\( \mu \)m x 1\( \mu \)m Ge-HfO₂ pMOSFET.

Bias-Dependence

Noise measurements were done at various gate and drain voltage biases with one set holding the gate voltage constant (\( V_g = -1.5 \)) and varying the drain voltage and in a second set holding the drain voltage constant (\( V_d = -0.1 \)) and varying the gate voltage. In the constant gate voltage case, Figure 4.19 shows that there is no 1/f
noise dependence on drain bias for the Ge-HfO₂ MOSFETs, consistent with silicon MOSFETs (Section 2.4). In the constant drain voltage case, Figure 4.20 shows the general trend of the inverse relationship of $S_N$ to the gate voltage. Again, this behavior is consistent with that of silicon MOSFETs (Section 2.4).

![Figure 4.19: Normalized noise spectral density at 10Hz as function of drain bias for a 10μm x 1μm Ge-HfO₂ pMOSFET with $V_g = -1.5$V.](image)

Scaling-Dependence

$S_N$ for various gate lengths ($L_g$) and widths ($W_g$) were compared. Figure 4.21 shows the inverse dependence of 1/f noise of Ge-HfO₂ pMOSFETs on gate length, consistent to that of silicon MOSFETs (Section 2.4). Figure 4.21 shows an inverse dependence of 1/f noise of Ge-HfO₂ pMOSFETs on gate width. However, contrary to expectations with the trend in silicon MOSFETs, the log-log plot shows the noise level has a slope of two versus the gate width, which implies an inverse quadratic dependence on gate width. This non-ideality can be attributed to the edge effects (dangling bonds,
edge roughness), which affect a larger proportion of the total current in the narrower MOSFETs.

### 4.4.4 Summary of 1/f Noise in Ge-HfO$_2$ pMOSFETs

The use of 1/f noise as a characterization tool for interface studies of Ge-HfO$_2$ pMOSFETs has shown that the noise level is two orders of magnitude higher than that of conventional Si-SiO$_2$ PMOSFETs, providing evidence that the density of interface traps is much higher, and is the dominant reason for the Fermi-level pinning of the gate in these devices. The bias- and scaling-dependence of the 1/f noise in Ge-HfO$_2$ pMOSFETs appear to be similar to that of silicon MOSFETs, however, the edge effects of the narrower devices may be cause for some concern, if the potential of Ge-HfO$_2$ MOSFETs as a device technology for CMOS logic is to be achieved.
4.5 Carbon Nanotube FETs

Along with many novel properties of carbon nanotubes, it was expected, despite their carrier transport being one-dimensional which generally leads to increase in noise, that the noise properties of CNTs would still be favorable, owing to their being covalent metallic bonds which are less susceptible to atomic location fluctuation, electromigration, and defect propagation. In addition, the one-dimensional transport may even work to its favor through the greatly reduced phonon scattering [82].

Contrary to such expectations, it was discovered that carbon nanotubes actually exhibit unexpectedly large electrical noise compared to the expected thermal noise, $S_V = 4kTR$ (Figure 4.23). The excess noise is $1/f$ in nature [82].

Compared to conventional conductors ranging from high-quality metal films to "noisy" carbon composite resistors, CNT noise is four to ten orders of magnitude higher [82]. This high level of noise can be partly explained by the small number of
Figure 4.22: Normalized noise spectral density Ge-HfO$_2$ pMOSFETs at 10Hz as function of gate width.

carriers, leading to higher relative fluctuations in the conducting current [83]. The effect of surface fluctuations is also considerable, since every atom of the CNT is in fact a surface atom, so the current is easily perturbed by local charge fluctuations [84]. The substrate material on which the CNT lies must also be considered as a possible source of the 1/f noise.

### 4.5.1 Role of Oxide Traps in CNTFET 1/f Noise

A typical carbon nanotube FET (CNTFET) has a back-gate configuration on a thin SiO$_2$ layer with the drain and source contacts made of palladium. The high 1/f noise level in a CNTFET is suggested by some [85–87] to be from the presence of trapped charges in the interface between the CNT and the oxide. In one-dimensional carrier transport, any disruption in a single carrier flow significantly affects the entire current as there is only one "path" that the carriers go through, and any slow-down
causes a "traffic jam". Figure 4.24 shows the 1/f noise spectrum for a CNTFET.

Lin et al [85] have shown that by using rapid thermal annealing (RTA), the 1/f noise can also be reduced (Figure 4.25, supporting the theory that oxide traps are the dominant source of CNTFET 1/f noise. Furthermore, Lin and Avouris [86] have shown that by fully suspending the CNT (Figure 4.26), the 1/f noise is reduced (Figure 4.27) compared to one in contact with the SiO₂ substrate, which again suggests the significant role of oxide traps in CNTFET noise.

### 4.5.2 Summary of 1/f Noise in CNTFETs

Needless to say, the high level of noise in CNTFETs presents a huge obstacle to their status as a viable alternative to silicon in CMOS technology. Carbon nanotube circuits, whether analog or digital, will simply not operate properly.

There is still no consensus as to the source of the noise, but the evidence above,
and further results discussed later in Section 5.5 seem to support that it comes from traps in the CNT-SiO$_2$ interface. This is not surprising in that while SiO$_2$ makes an excellent interface to its native silicon, it does not necessarily do so with non-native carbon, Ge or III-V semiconductors [41, 88–90].

Currently, attempts are being made to use hafnium oxide (HfO$_2$) as the dielectric layer, but noise studies with this material combination is still sparse. There are also attempts to build top-gated CNTFETs, but CNT damage during the process is still a huge problem.
Figure 4.25: Comparison of the noise power spectra of a CNTFET before and after RTA [85].
Figure 4.26: A pair of CNTFETs from a common CNT, one fully suspended and the other in contact with the SiO₂ substrate [86].
Figure 4.27: Comparison of the noise power spectra of a pair of CNTFETs from a common CNT, one fully suspended and the other in contact with the SiO$_2$ substrate [86].
Chapter 5

1/f Noise in MOSFETs and Device Reliability

5.1 Introduction to Device Reliability

The study of the device reliability of MOSFETs is critical to the semiconductor industry, as the success of a particular MOSFET technology is highly dependent on the quality of the products and their usable lifetimes. Such reliability studies include the investigation of failure conditions and their underlying mechanisms, involving diagnostic tools like charge-pumping, for example.

In this chapter, the use of 1/f noise measurements as a powerful diagnostic tool for the investigation of device reliability of MOSFETs is introduced. Through this method, the semiconductor-oxide interface initial quality can be determined, and the progress of device degradation can be tracked using the rising level of the measured 1/f noise, often before any visible degradation of the usual device parameters, like threshold voltage and drain current, is observed.

If carrier-number fluctuation is the dominant noise mechanism in a device, then the generation of interface and oxide traps under electrical stress can be studied. On the other hand, if mobility fluctuation is the dominant noise mechanism, then formation of bulk defects under electrical stress can be investigated. As such, both of these mechanisms can be observed and they will indeed prove very useful in reliability
studies of MOSFETs.

5.1.1 Device Lifetimes

The approximation of device lifetimes is a controversial area at best. The critical level of degradation where the device is classified as "dead" or "killed" varies in different applications, and devices considered to have already failed in one case may still be perfectly acceptable in another case. For example, a degradation level used in many cases to signify the failure of a device is a ten percent drop in the transconductance or drive current [28, 91].

It is not commercially practical to actually wait until a device tested under the operating conditions required by the application fails in order to determine its actual marketable lifetime. The determination of device lifetimes therefore is accelerated by subjecting the device to harsher operating conditions and then extrapolating its failure rate in this case to what is expected in its real world application.

The extrapolation of the lifetime data is done through various power-law formulas involving empirical constants [28, 92, 93]. The accuracy of these formulas is rarely tested, as often, by virtue of Moore's Law, the devices become obsolete in a small fraction of their predicted lifetimes and therefore discarded before they start to fail.

5.1.2 Hot-Carrier Effects

In high electric fields, the carriers within a MOSFET channel achieve velocities that approach $10^7$ cm/s. Since the electric field is inversely proportional to the channel length, the trend for shortening the channel length can lead to extremely high longitudinal fields. The peak electric field usually occurs near the drain-channel junction. When the carriers move in fields that exceed the limit for velocity saturation, they will continue to acquire kinetic energy from the field. Since the carriers are already in saturation velocity, the velocity component in the field direction no longer increases, but their random kinetic energy does. A fraction of the carrier population will therefore acquire a significant amount of energy. These carriers are commonly referred to as hot carriers [26].
Some effects resulting from hot carriers are illustrated in Figure 5.1. Carriers that come near the pinchoff region are accelerated by the high field. The ones that gain enough energy to become hot carriers may start colliding with the lattice, creating impact ionization processes. When this happens, bound electrons are knocked off the nucleus of the semiconductor atoms, and these join the channel electrons moving towards the drain [26].

![Schematic representation of hot carrier effects in a region of high longitudinal electric field in the channel of an NMOS](image)

Figure 5.1: Schematic representation of hot carrier effects in a region of high longitudinal electric field in the channel of an NMOS [26].

If the field is high enough, a significant fraction of the carriers may scatter and acquire velocity in a direction normal to the field towards the oxide. Those carriers with enough energy, in addition to those being injected through Fowler-Nordheim tunneling, may then overcome the semiconductor-oxide barrier and get injected into the oxide layer. This not only results in contribution to the gate leakage current, but also results in damage to both the semiconductor-oxide interface and the oxide [26].

The damage to the semiconductor-oxide interface results in an increase in the
density of interface states, \( N_{it} \), and the damage to the oxide results in an increase in the density of fixed oxide charges, \( Q_{ox} \) [26]. Over time, these processes lead to degradation of device parameters, like threshold voltage shifts, drive current lowering, etc, and are thus a major contributor to the "aging" and ultimate failure of MOSFETs.

**Mechanisms of Hot Carrier Effects**

Despite large efforts spent during the past decades in understanding all the mechanisms of hot carrier effects, there is still no unanimous agreement on this matter. One of the reasons why this is the case is because of the lack of reliable and sensitive techniques to evaluate interface damage from carrier injection.

For NMOS devices, a hot-carrier mechanism called hot-electron-induced-punchthrough (HEIP) is generally accepted where hot electrons injected into the oxide near the drain generate negative oxide charges that reduce the effective channel length. This shorter channel may be treated as an extended drain so the threshold voltage is shifted and the drain extension results in higher drain resistance [93, 94].

For PMOS devices, it is generally accepted that the hot-carrier mechanism is facilitated by the generation of interface states by holes which reduce the transconductance. Also possibly contributing is the injection of holes into the oxide generating positive oxide charges [93, 95].

**Hot Carrier Effects and 1/f Noise**

In the past decade, several papers [96–99] have reported an increase in 1/f noise in MOSFETs subjected to hot-carrier stress. This is not surprising, as such electrical stress results in damage to both the oxide and the bulk region, so the generation of oxide traps in the former case adds to the noise through an increase in carrier number fluctuation, and degradation of the crystal in the latter case adds to the noise through an increase in mobility fluctuations. Section 5.2 will discuss this noise degradation specifically on Si-SiO\(_2\) MOSFETs.
5.1.3 Negative Bias Temperature Instability

Negative Bias Temperature Instability (NBTI) is a reliability issue that affects mainly PMOS devices. As the name implies, the degradation effects occur at negative gate voltages and at elevated temperatures. Typical NBTI stress is generally defined as the stress condition where a gate voltage sufficient to produce a field of $2 \times 10^6$ V/cm in the oxide and temperature higher than 100°C [23, 92]. NBTI effects manifest themselves in terms of degradation of key MOSFET parameters, for example, an increase in the threshold voltage and off current, and the consequential lowering of the drain current and transconductance (Figures 5.2-5.3 [100, 101]).

![Graph showing threshold voltage and charge-pumping current increase](image)

Figure 5.2: Threshold voltage and charge-pumping current increase for a PMOSFET undergoing NBTI stress [100].

NBTI is currently observed in silicon PMOSFETs, whether paired with SiO₂ or other Hi-κ dielectric materials. Not enough studies have been done for bulk materials other than silicon, but the mechanism behind it is likely to be general.
Mechanisms for NBTI

Even though not yet fully understood currently in a Si-SiO₂ MOSFET device, it is widely believed to be caused by the generation of interface traps from silicon dangling bonds [102, 103]. Interface traps are presumed to be electrically active defects with an energy distribution throughout the silicon bandgap. These act as generation-recombination centers and may contribute to increased gate leakage current, mobility degradation, and the possible increase in 1/f noise [104]. The induced threshold voltage shifts may be described by

\[ \Delta V_T = -\frac{\Delta Q_U(\phi_s)}{C_{ox}} \]  

where \( \phi_s \) is the surface potential. As shown in Figure 5.4, interface traps are acceptor-like in the upper half of the bandgap and donor-like in the lower half of the bandgap. Note that this is opposite of that of doping atoms [104].
Figure 5.4: Si-SiO$_2$ interface traps are acceptor-like in the upper half of the bandgap and donor-like in the lower half of the bandgap [104].

A recently proposed mechanism for NBTI is the hole-trapping model, where the application of a negative bias on the gate induces holes to migrate towards the oxide, and if the field is high enough, holes may end up in a trap state within the oxide material, and may subsequently remain there, causing the shift in the threshold voltage [105].

**Recovery**

As the NBTI stress is removed, there is some recovery of the device parameters from the degraded levels, which is enhanced when positive bias is applied on the gate [105].

**NBTI and 1/f Noise**

There have not been any studies of the relationship between NBTI and 1/f noise. In the experiments conducted for the research in this thesis, it was found that the degradation in 1/f noise due to NBTI stress itself is within the error range and is therefore
not significant enough to conclude any relationship between the two processes. This tends to support Shen’s [105] hole-trapping model for NBTI, where fixed charges contribute to the degradation and not trap formation in the oxide. In this case, it can be seen that such mechanism will not significantly contribute to an increase in 1/f noise.

NBTI-enhanced Hot Carrier Effects

When a drain bias on a MOSFET is coupled with a high gate bias, the resulting damage on the device is called NBTI-enhanced hot carrier effects (HC-NBTI). It is not the summation of hot-carrier damage and NBTI damage, as the drain bias can be low for hot-carrier effects at room temperature, but then the device will show significant effects of the HC-NBTI stress [92]. Many of the experiments done in the research in this chapter actually involved NBTI-enhanced hot-carrier effects.

5.2 Silicon-Silicon Dioxide (Si-SiO₂) MOSFETs

As the Si-SiO₂ MOSFET is the main driver of the semiconductor industry, reliability studies of it have been performed extensively, usually involving the observation of external device parameters. A few techniques like charge-pumping allow some insight into the less visible parameters, like trap density. In the past decade, interest has surged in the use of 1/f noise as a reliability diagnostic tool [21, 22].

MOSFETs are usually subjected to electrical stress for a period of time, at higher operational levels than normal operating biases to accelerate the degradation process. Typical methods of electrical stresses used are Fowler-Nordheim tunneling, Hot-Carrier, and NBTI. NBTI stress does not seem to significantly effect the 1/f noise of the device, as discussed above, and although Fowler-Nordheim stress does result in significant 1/f noise degradation [106], hot-carrier stress is closer to what occurs in normal operating conditions, so it is the favored method in the semiconductor industry, and in the investigations of this thesis.

Figure 5.5 shows the \( I_d-V_g \) curve of a submicron (\( W \times L = 100 \mu m \times 0.8 \mu m, t_{ox} = 20nm \)) NMOSFET and its degradation under hot-carrier stress. Figure 5.6
shows the increase in the charge-pumping current of the same device under stress, and therefore the increase in the extrapolated trap density.

![Figure 5.5: I_d-V_g curve of a submicron (W x L = 100 \mu m x 0.8 \mu m, t_{ox} = 20nm) NMOSFET and its degradation under hot-carrier stress [98].](image)

The 1/f noise degradation of the same device is shown in Figure 5.7 in comparison with the relative degradation of the transconductance and charge-pumping current. This clearly shows that the degradation of 1/f noise is faster than that of transconductance and charge-pumping current. This strongly supports the thesis of 1/f noise as a more sensitive diagnostic tool for MOSFET damage analysis under hot-carrier stress than currently utilized techniques.

**Border Traps**

If 1/f noise is determined by the interface trap density, then there should not have been a difference in the degradation rates between the 1/f noise and charge-pumping measurements. However, the observation of this difference in degradation rates led
to questions of what kinds of traps relevant to the 1/f noise mechanism are being created.

Fleetwood [107] suggested a new classification for these kinds of oxide traps. Whereas he defines interface traps as traps exactly at the Si-SiO₂ interface, and oxide traps are those that are within the oxide film that does not interact with the silicon bulk channel. He added a new nomenclature called border traps that are physically similar to oxide traps, but are located close enough to the interface that charge exchange between them and the MOSFET channel happens on a time-scale observable through 1/f noise [107]. This approach suggests that under hot-carrier stress, border traps are created faster than interface traps.

Figure 5.6: Charge pumping current and degradation upon hot-carrier stress of a submicron (W × L = 100 μm × 0.8 μm, t_{ox} = 20nm) NMOSFET at maximum substrate condition of V_g = 2V, V_d = 5V, resulting in increasing extrapolated trap density [98].
CHAPTER 5. 1/F NOISE IN MOSFETS AND DEVICE RELIABILITY

Figure 5.7: The 1/f noise degradation of a submicron (W x L = 100 μm x 0.8 μm, t_{ox} = 20nm) NMOSFET under hot-carrier stress showing a faster rate compared to that of transconductance and charge-pumping current [98].

5.3 Silicon-HfSiON MOSFETs

The Si-HfSiON MOSFETs used in the reliability studies in this section are the same as those described in Section 4.3. The devices are designed for a supply voltage of 1V.

5.3.1 Hot Carrier Stress

The devices were subjected to room temperature hot-carrier stress with a gate bias of 2.5V and drain bias of 2.5V for NMOS devices and -2.5V, -2.5V respectively for PMOS devices for up to 5000 seconds [75].

The I_d-V_g degradation is shown in Figure 5.8 for particular devices. The initial stress period of 100 seconds resulted in a huge shift in the I-V curves, due to the filling of traps within the dielectric through tunneling. The evolution of the threshold
voltage shifts under stress are shown in Figure 5.9. As can be seen, the linear shift over the logarithm of the stress time is similar to those of conventional Si-SiO₂, which suggests that the mechanism degradation is due to hot-carrier injection [95].

Figure 5.8: Evolutions of Si-HfSiON MOSFET I_d-V_g curves under hot-carrier stress for a) 10 μm × 0.4 μm NMOS device with V_g = 2.5, V_d = 2.5 and b) 10 μm × 0.4 μm PMOS device with V_g = -2.5, V_d = -2.5. For both devices the initial stress time of 100s provided the biggest shift.

Figure 5.10 shows the degradation under stress of the 1/f noise behavior of the devices. As can be seen, the linear behavior of the increase in the noise level vs the logarithm of the stress time starts with a steeper slope, then the degradation starts to saturate around 1000 seconds of stress time. This suggests that most of the V_th-shift observed in Figure 5.9 beyond this time can be attributed to deeper oxide trap formation rather than interface traps, as 1/f noise is mainly contributed by either the interface traps or mobility fluctuations in the channel.

5.3.2 Recovery

When electrical biases of opposite polarities to the stress conditions were applied (V_g = -2.5, V_d = -2.5 for NMOS, and V_g = 2.5, V_d = 2.5 for PMOS), some recovery
in both the $V_{th}$-shift and noise were observed. Figure 5.11 shows the recovery in the $V_{th}$-shift for the NMOS and PMOS devices respectively, and Figure 5.12 shows the recovery in the noise for the NMOS and PMOS devices respectively. It can be observed that in both cases, full recovery of the $V_{th}$ and noise degradation does not occur. This is likely due to the lattice damage from the hot-carrier stress, which is virtually irreversible at room temperature and requires high temperature annealing. The partial recovery is due to reverse migration of the mobile charges in the hi-$\kappa$ dielectric stack.

5.3.3 Summary

It was shown that upon application of hot-carrier stress, Si-HfSiON MOSFETs exhibit threshold voltage and noise degradation. Upon reversal of the stress conditions, partial recovery is observed, which is likely due to reverse migration of mobile ions,
providing evidence that the threshold voltage instability in Si-HfSiON MOSFETs is mainly due to the movement of ions in the dielectric stack.

5.4 Germanium-HfO$_2$ MOSFETs

The Ge-HfO$_2$ MOSFETs used in the reliability studies in this section are the same as those described in Section 4.4. The devices are designed for a supply voltage of 1.5V. Even at room temperature, there is some hysteresis in the $I_d$-$V_g$ sweep of the Ge-HfO$_2$ PMOSFETs (Figure 5.14. This gives evidence of carrier trapping-detrapping mechanisms at the Ge-HfO$_2$ interface, and is a serious problem that must be solved before Ge-HfO$_2$ MOSFETs can become a viable CMOS technology.
Figure 5.11: Threshold voltage recovery of Si-HfSiON 10 μm × 0.4 μm NMOS and PMOS devices after hot carrier stress for 2000s and reverse polarity stress bias for another 2000s, showing only partial recovery.

Figure 5.12: Noise degradation recovery of the same devices in Figure 5.11 after hot carrier stress for 2000s and reverse polarity bias for another 2000s, showing only partial recovery.
Figure 5.13: Normalized noise spectral density at 10Hz as function of temperature for a 10\(\mu\)m \(\times\) 1\(\mu\)m GE PMOSFET.

5.4.1 Temperature Dependence

The effect of temperature on 1/f noise and \(I_d-V_g\) hysteresis of the Ge-HfO\(_2\) MOSFETs were measured at temperatures of 100K, 200K, 300K, and 360K. At 360K, the 1/f noise level is virtually the same as at room temperature, but is one order of magnitude higher when measured at 100K and 200K (Figure 5.13). The \(I_d-V_g\) hysteresis is shown in Figure 5.14, the hysteresis at the 100K and 200K is observed to be much worse than at either room temperature or 360K. Both the noise and hysteresis degradations were found to be permanent. Taking this degradation in 1/f noise and low-temperature \(I_d-V_g\) hystereses together, a possible explanation is that due to the strain already present in the lattice-mismatched materials, and the added stress of different material thermal expansion coefficients, the ramping down to lower temperatures adds to the interface defects, thus adding to the hysteresis and the 1/f noise. Interface defects are seemingly the main source of high 1/f noise in Ge-HfO\(_2\) PMOSFETs.
5.4.2 Hot-Carrier Stress

The devices were subjected to room temperature hot-carrier stress with a gate bias of 2.5V and drain bias of 2.5V for NMOS devices and -2.5V, -2.5V respectively for PMOS devices for up to 5000 seconds.

The Ge-HfO$_2$ PMOSFETs were subjected to room temperature hot-carrier stress with a gate voltage of -3V and drain voltage of -3V for up to 5000s. The I-V degradation is shown in Figure 5.15 for a 10\(\mu\)m \(\times\) 1\(\mu\)m device. Similar to the Si-HfSiON devices in Section 5.3, the initial stress period resulted in a huge shift in the I-V curve, due to the filling of traps in the dielectric through tunneling.

The evolution of the threshold voltage under stress is shown in Figure 5.16. Again, it can be seen that the linear shift over the logarithm of the stress time is similar to those of conventional Si-SiO$_2$ MOSFETs, which suggests that the mechanism degradation is due to hot-carrier injection.

Figure 5.17 shows the degradation of 1/f noise behavior of the device. Similar to the Si-HfSiON MOSFETs in Section 5.3, the linear behavior of the increase in the
noise level vs the logarithm of the stress time starts with a steeper slope, then the degradation saturates around 1000 seconds of stress time. Again, this suggests that

Figure 5.15: Ge-HfO\textsubscript{2} MOSFET \(I_d-V_g\) degradation at stress of \(V_g = -3, V_d = -3\).

Figure 5.16: Ge-HfO\textsubscript{2} MOSFET \(V_{th}\) degradation at stress of \(V_g = -3, V_d = -3\).
most of the $V_{th}$-shift observed in Figure 5.17 beyond this time point is attributable to deeper oxide trap formation rather than interface traps which heavily contribute to $1/f$ noise.

![Graph](image_url)

Figure 5.17: Ge-HfO$_2$ MOSFET $1/f$ noise degradation at stress of $V_g = -3, V_d = -3$.

### 5.4.3 Summary

It was shown that Ge-HfO$_2$ PMOSFETs have a hysteresis problem that must be resolved before the technology can progress as a CMOS logic alternative. The hysteresis and $1/f$ noise degraded at lower temperatures, and became permanent, suggesting the occurrence of lattice-mismatch related dislocations and that these devices may not be robust enough under common temperature swings to be useful.

Upon application of hot-carrier stress, Ge-HfO$_2$ PMOSFETs exhibit threshold voltage and noise degradation, which saturated after some time, suggesting that deeper oxide trap formation rather than interface traps which heavily contribute to $1/f$ noise are the cause of the later shift in threshold voltage.
5.5 Carbon Nanotube MOSFETs

An issue that will be of significant importance as the popularity of CNT-FETs grows is the reliability performance of these devices under normal operating conditions, which has not yet been sufficiently studied. Before CNT-FETs can be considered a viable alternative to the Si-SiO₂ MOSFET, they must first demonstrate sufficient resistance against the usual degradation mechanisms.

Currently, owing partly perhaps to the assumption that the superior transport properties of carbon nanotubes offer some immunity against operating condition stress and damage, and partly to the non-existence of a well-accepted standard manufacturing process, the study of the reliability of CNT-FETs has been largely ignored, unlike its silicon-based counterparts.

5.5.1 Device Fabrication and Characteristics

The CNT-FETs in this section use a standard back-gate configuration and are fabricated on a silicon substrate with a 10nm thermal SiO₂. Catalyst sites are pre-patterned by optical lithography and CNTs are synthesized by chemical vapor deposition (CVD). Electron beam lithography is used to write the source and drain contacts. Palladium metal is then deposited followed by lift-off [108].

Figures 5.18 and 5.19 show the $I_d-V_d$ and $I_d-V_g$ curves respectively of one of the devices, where the current fluctuations are clearly seen. The drain current noise spectrum is shown in Figure 5.20.

5.5.2 Device Reliability under Hot-Carrier Stress

As there is evidence of the contribution of oxide traps to the 1/f noise behavior of CNT-FETs [85–87] (see Section 4.5.1), it is probable that hot carrier stress of CNT-FETs may lead to similar observations of device parameter and noise degradations as that of Si-SiO₂ MOSFETs.

In this thesis research, the I-V and 1/f noise behavior of CNT-FETs were measured under hot carrier stress of $V_g = V_d = 1.5V$ up to 10,000 seconds. Multiple devices
Figure 5.18: $I_d$-$V_d$ characteristic of a CNT-FET showing visible fluctuations.

Figure 5.19: $I_d$-$V_g$ characteristic of a CNT-FET
Figure 5.20: Normalized current noise spectrum of a CNT-FET. Noise here is measured at $V_g=-1$, $V_d=-1$.

were tested, all showing the same trends. Figure 5.21 shows the degradation of the $I_d-V_g$ curve under stress, resulting in shifts in the threshold voltage over time. As in Si-SiO$_2$ MOSFETs, this can be explained by the formation of traps in the oxide and CNT-oxide interface due to hot-carrier injection.

Figure 5.22 shows the evolution of the threshold voltage determined from the $I$-$V$ curves over stress time. The linear shift over the logarithm of the stress time is similar to that of conventional Si-SiO$_2$ MOSFETs and supports the explanation that the mechanism behind CNT-FET hot-carrier effects is likely to be the same.

Figure 5.23 shows the degradation over time in the $1/f$ noise behavior of the CNT-FET under hot-carrier stress. Again, the trend and rate of degradation of the noise level is similar to that of conventional Si-SiO$_2$ MOSFETs, which is consistent with an increase in oxide and interface traps. This supports the suggestion that oxide charged traps and defects are the dominant source of $1/f$ noise behavior of CNT-FETs.

5.5.3 Summary of CNTFET Noise and Reliability under Hot-Carrier Stress

Clearly, CNT-FETs suffer under hot carrier stress on a similar level to that of conventional Si-SiO$_2$ MOSFETs, despite their advantage in transport properties. Evidence
Figure 5.21: Degradation of $I_d - V_g$ characteristics of a CNT-FET under hot-carrier stress.

Figure 5.22: Threshold voltage degradation of a CNT-FET under hot-carrier stress.

shows that the suggestions of oxide traps and defects being the dominant source of 1/f
Figure 5.23: 1/f Noise degradation of CNT-FET under hot-carrier stress. Noise power spectral density measured at 1 Hz is used for comparison.

noise in CNTFETs are likely correct. More studies on CNT-FET operating reliability must therefore be conducted before it can be used for practical applications.
Chapter 6

Summary and Future Work

6.1 Summary

The approach of fundamental limits of materials with continued scaling of Si-SiO₂ MOSFETs, has put tremendous pressure to quickly find a suitable alternative material combination to Si-SiO₂ that can be evaluated for CMOS suitability in a short period of time. In addition to the need for advanced devices to satisfy operating benchmarks set by conventional Si-SiO₂ MOSFETs, they must maintain the standard for a commercially useful lifetime. Without the 50 years of history with which Si-SiO₂ MOSFETs were developed, tested, and improved, methods to thoroughly, yet efficiently analyze advanced MOSFETs are sorely needed. In this thesis, it has been shown that 1/f noise can be used as a powerful tool for both device characterization and reliability studies of advanced devices, especially as a complement with other techniques.

Using techniques and analyses of noise developed through the years originally for Si-SiO₂ MOSFETs, the advanced MOSFET devices that were characterized covered various types, and include one where silicon was still used as the channel material, but with a hi-κ dielectric, another where germanium was used as the channel material, and a third where 1-D carrier transport was utilized with carbon nanotubes.

In this thesis, it was shown through noise characterization that advanced bulk
CHAPTER 6. SUMMARY AND FUTURE WORK

MOSFETs (Si-HfSiON and Ge-HfO$_2$) have higher magnitudes of 1/f noise than conventional Si-SiO$_2$ MOSFETs likely due to higher interface trap densities, in agreement with expectations. For these advanced devices, the higher trap density is conducive to Fermi-level pinning of the gate, and must eventually be resolved for their continued consideration as viable alternatives. It was also shown that these advanced bulk devices have similar bias and scaling dependence of the noise to that of conventional Si-SiO$_2$ MOSFETs, giving evidence that the mechanisms for noise are probably also similar.

It was also shown that under hot-carrier stress, contrary to conventional Si-SiO$_2$ MOSFETs, the noise degradation of these devices eventually saturated, while the threshold voltage degradation did not for the period of time tested, giving evidence that with the already higher interface trap densities, the main contribution to the voltage shifts is due to mobile charge migration in the oxide. The presence of mobile charges is in agreement with the observed hysteresis and threshold voltage instabilities.

For CNTFETs, it was shown that despite the transport advantages of 1-D CNTs, hot-carrier stress led to degradation comparable to conventional Si-SiO$_2$ MOSFETs, giving further evidence that a source of 1/f noise in CNTFETs is the underlying oxide. This also emphasized that reliability studies of CNTFETs must not be ignored, if it is to continue as a viable alternative for CMOS technology.

In general, 1/f noise was shown to be a good tool for interface quality characterization. Eventually, it is of interest that the noise levels in these advanced devices be within reasonable magnitudes for ease of integration into current device and circuit standards. In addition, the use of 1/f noise as a reliability tool has also provided valuable insights as to the mechanisms behind the damage experienced by devices under stress. As good long-term reliability is one of the important considerations for choosing a good material combination to replace conventional Si-SiO$_2$ MOSFETs, knowledge of these mechanisms may provide fixes or changes necessary to further the technology.
6.2 Future Work

As more and more MOSFET alternative material combinations are being developed and investigated, they should all become candidates for 1/f noise studies. The exact mechanisms behind 1/f noise up to present are not yet fully understood, but with a wider range of new materials to test, there is hope that the fundamental questions regarding 1/f noise will one day be fully answered.

Several advanced MOSFETs involving germanium, III-V semiconductors, and graphene would have been great additions to the work in this thesis, but unfortunately, although in advanced stages of developments, suitable devices were still not available in time for this thesis. Successors of this research work should consider the investigation of these advanced devices.

Improvements in the noise measurement setup involving better device shielding, better system isolation, etc will make it useful for the noise characterization of other semiconductor devices with lower 1/f noise levels, like diodes. Further automation involving low-leakage relays and programmable probers will greatly speed up the noise measurement process and should definitely be implemented by any student continuing this line of investigation.
Appendix A

Noise Measurement Automation Code

The program code used to run the automated noise measurements was written using Visual Basic in the Microsoft Excel environment. The code follows:

Sub Main()
Dim SMU124 As String

GPIB_CARD = "NATIONAL"
Stop

Call HP35670A("11", "10")
Stop

Call ReadIn_Array
Stop

For c_loop = 1 To c_var
For b_loop = 1 To b_var
For a_loop = 1 To a_var
APPENDIX A. NOISE MEASUREMENT AUTOMATION CODE

SMU124 = Trim(b(b_loop)) & "|" & a(a_loop) & "|" & c(c_loop) & "|START"
Call HP4156C("18", SMU124)
Stop
Next
Next
Next
Stop

Call HP4156C("18", "456|START")
read_result_str(0) = read_result_str(0) & " | " & Str(read_result(0))

End Sub

Sub HP4156C(InstAdd As String, CommandLine As String)

Dim sc_temp As String
Dim GpibAddress As String
Dim Command4156 As String
Dim ForSmu As String
Dim SweepFile As String
Dim temp_str As String

If GPIB_CARD = "HP" Then
    GpibAddress = "hpib7," & InstAdd
ElseIf GPIB_CARD = "NATIONAL" Then
    GpibAddress = InstAdd
End If

'Take the first word of command string
Command4156 = WordNum(CommandLine, 1, "|")
'**********************
'* 4156 Commands follow
'**********************

'Load IdVg Sweep Setup
If Command4156 = "Load" Then

'Load sweep setup file
SweepFile = WordNum(CommandLine, 2, "|")
sc_temp = ":MMEM:LOAD:STAT 0," & SweepFile & ",',DISK"
Call SC(GpibAddress, sc_temp, "NA", "WRITE")
wait_time (10)
End If

'Trigger sweep
If Command4156 = "Sweep" Then

sc_temp = ":PAGE:SCON:SING"
Call SC(GpibAddress, sc_temp, "NA", "WRITE")
wait_time (30)

End If

'Store Data
If Command4156 = "SaveData" Then

sc_temp = ":FORM:DATA ASC"
Call SC(GpibAddress, sc_temp, "NA", "WRITE")
SweepFile = WordNum(CommandLine, 2, "|")
temp_str = WordNum(CommandLine, 3, "|")
Cells(1, 2) = "Writing IV Data..."
sc_temp = ":MMEM:DEST INT"
Call SC(GpibAddress, sc_temp, "NA", "WRITE")
sc_temp = ":MMEM:STOR:TRAC DEF,'" & SweepFile & temp_str & ".DAT','DISK'"
Call SC(GpibAddress, sc_temp, "NA", "WRITE")
wait_time (60)

End If

'Set Stress Biases
If Command4156 = "SetBias" Then

'Set SMU 1 Bias (Drain Voltage)
ForSmu = WordNum(CommandLine, 2, "|")
If Mid(ForSmu, 1, 1) <> "*" Then
sc_temp = ":PAGE:STR:SET:CONS:SMU1 " & ForSmu
Call SC(GpibAddress, sc_temp, "NA", "WRITE")
wait_time (1)
End If

'Set SMU 2 Bias (Gate Voltage)
ForSmu = WordNum(CommandLine, 3, "|")
If Mid(ForSmu, 1, 1) <> "*" Then
sc_temp = ":PAGE:STR:SET:CONS:SMU2 " & ForSmu
Call SC(GpibAddress, sc_temp, "NA", "WRITE")
wait_time (1)
End If

'Set SMU 4 Bias (Substrate Voltage)
ForSmu = WordNum(CommandLine, 4, "|")
If Mid(ForSmu, 1, 1) <> "*" Then
    sc_temp = ":PAGE:STR:SET:CONS:SMU4 " & ForSmu
    Call SC(GpibAddress, sc_temp, "NA", "WRITE")
    wait_time (1)
End If

End If

' Start the stress
If Command4156 = "Start" Then
    wait_time (1)
    sc_temp = ":PAGE:SCON:STR" ' Start the stress
    Call SC(GpibAddress, sc_temp, "NA", "WRITE")
End If

' Stop the stress
If Command4156 = "Stop" Then
    sc_temp = ":PAGE:SCON:STOP" ' Stop the stress
    Call SC(GpibAddress, sc_temp, "NA", "WRITE")
    wait_time (4)
End If

End Sub

Sub HP35670A(InstAdd As String, CountAve As String)
Dim sc_temp As String
Dim GpibAddress As String
Dim ForSmu As String
Dim temp_str As String
APPENDIX A. NOISE MEASUREMENT AUTOMATION CODE

If GPIB_CARD = "HP" Then
  GpibAddress = "hpib7," & InstAdd
ElseIf GPIB_CARD = "NATIONAL" Then
  GpibAddress = InstAdd
End If

' Need nnumber of average and Start
'Stop

Call SC(GpibAddress, "VOLT:RANG:AUTO 1", "NA", "WRITE")
  temp_str = "AVER:C0UN " & CountAve
Call SC(GpibAddress, temp_str, "NA", "WRITE")
Call SC(GpibAddress, "TRIGGER:START 1", "NA", "WRITE")
Call SC(GpibAddress, "Init:Imm", "NA", "WRITE")

Call SC(GpibAddress, "CALC1:MARK ON", "NA", "WRITE")
Call SC(GpibAddress, "CALC1:MARK:POS:POINT 20", "NA", "WRITE")

For i = 1 To 100
  wait_time (20)
  Call SC(GpibAddress, "*0PC?", "NA", "WRITE_READ")
If Val(WordNum(strres, 1, ",")) = 1 Then
  i = 1000000
End If
Next
Call SC(GpibAddress, "CALC1:DATA?", "NA", "WRITE_READ")

  temp_str = WordNum(strres, 2, ",")

'Stop
APPENDIX A. NOISE MEASUREMENT AUTOMATION CODE

If 1 = 2 Then

Call SG(CpbAddress, "Calc1:Mark:mode abs", "NA", "WRITE")

sc_temp = "SENS:FREQ:STAR 0"
Call SG(CpbAddress, sc_temp, "NA", "WRITE")

sc_temp = "SENS:FREQ:STOP 100"
Call SG(CpbAddress, sc_temp, "NA", "WRITE")

sc_temp = "SENS:FREQ:START 0"
Call SG(CpbAddress, sc_temp, "NA", "WRITE")

sc_temp = "SENS:FREQ:STOP 10000"
Call SG(CpbAddress, sc_temp, "NA", "WRITE")

For i = 50 To 5000 Step 25

temp_str = "MMKP " & Trim(i) & " Hz;"

Call SG(CpbAddress, temp_str, "NA", "WRITE")
Call SG(CpbAddress, "RDMK;", "NA", "WRITE_READ")
temp_str = WordNum(strres, 2, ",")
Call PrintDatalog("c:\temp.txt", temp_str)
wait_time (0.1)
Next

End If
'Stop
End Sub

Sub ReadIn_Array()
i = 3
APPENDIX A. NOISE MEASUREMENT AUTOMATION CODE

While Trim(Cells(i, 2)) <> ""
a(i - 2) = Trim(Cells(i, 2))
i = i + 1
Wend
a_var = i - 3

i = 3
While Trim(Cells(i, 1)) <> ""
b(i - 2) = Trim(Cells(i, 1))
i = i + 1
Wend
b_var = i - 3

i = 3
While Trim(Cells(i, 3)) <> ""
c(i - 2) = Trim(Cells(i, 3))
i = i + 1
Wend
c_var = i - 3
End Sub

Sub NoiseTest()
Dim tmp_str1 As String
Dim tmp_str2 As String
Dim tmp_str3 As String
Dim AveCount As String
Dim FilePath As String
Dim FilePathIV As String

GPIB_CARD = "NATIONAL"
APPENDIX A. NOISE MEASUREMENT AUTOMATION CODE

Cells(1, 4) = "v1.0"
RowIndex = 8
FilePath = Cells(5, 2)
FilePathIV = Cells(4, 2)
AveCount = Cells(6, 2)
tmp_str1 = "NoiseTest|SPAN(Hz)|" & Trim(Cells(5, 5)) & "|" & Trim(Cells(5, 6)) & "|" & Trim(Cells(5, 7))
Call PrintDatalogl(FilePath, "OUTPUT", tmp_str1)

' Measure IdVg

Cells(1, 2) = "Sweeping IdVg..."
' Call PrintDatalogl(FilePathIV, "OUTPUT", "0")
tmp_str1 = Trim(Cells(3, 2))
tmp_str2 = "Load" & "|" & tmp_str1
Call HP4156C("18", tmp_str2)
Call HP4156C("18", "Sweep")
tmp_str1 = "SaveData" & "|" & FilePathIV & "|" & "0"
Call HP4156C("18", tmp_str1)

' Loop Noise Measurements

While Trim(Cells(RowIndex, 1)) <> ""

    Cells(1, 1) = RowIndex
    Cells(1, 2) = "Progress..."

    ' Set the bias

    tmp_str1 = Trim(Cells(RowIndex, 1)) & "|" &
Trim(Cells(RowIndex, 2)) & "|" & Trim(Cells(RowIndex, 3))
    tmp_str2 = "SetBias|" & tmp_str1
    Call HP4156C("18", tmp_str2)

'Start the bias

Cells(1, 2) = "Applying Bias"
tmp_str2 = "Start"
Call HP4156C("18", tmp_str2)

'Command the 35670 to start measuring the noise

wait_time (10)
Cells(1, 2) = "Measuring Noise"
Call HP35670A("11", AveCount)
strres = tmp_str1 & "|" & strres
Call PrintDatalogKFilePath, "APPEND", Trim(strres))
wait_time (10)
Cells(1, 2) = "Finished Measuring Noise"

'Stop the bias

tmp_str2 = "Stop"
Call HP4156C("18", tmp_str2)

'Next row

RowIndex = RowIndex + 1

Wend

'Re-Measure IdVg
APPENDIX A. NOISE MEASUREMENT AUTOMATION CODE

Cells(1, 2) = "Sweeping IdVg..."
tmp_str1 = Trim(Cells(3, 2))
tmp_str2 = "Load" & "|" & tmp_str1
Call HP4156C("18", tmp_str2)
Call HP4156C("18", "Sweep")
tmp_str1 = "SaveData" & "|" & FilePath & "|" & "1"
Call HP4156C("18", tmp_str1)

Cells(1, 2) = "Measurement Run Complete"

End Sub
Bibliography


[94] B. S. Doyle, M. Bourcerie, C. Bergonzoni, R. Benedetti, A. Bravis, K. R. Mistry, and A. Boudou, "The generation and characterization of electron and hole traps


