FAST PHOTOCONDUCTIVE MATERIALS FOR WIDEBAND A/D CONVERSION AND MONOLITHIC INTEGRATION WITH CMOS

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF
MATERIALS SCIENCE AND ENGINEERING
AND THE COMMITTEE ON GRADUATE STUDIES
OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

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December 2009

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

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Abstract

Modern communication and high-speed instrumentation require ultra-high speed analog-to-digital converters (ADCs) with bandwidths up to several tens of Giga-Hz and ever increasing resolution. The performance of state-of-the-art electronic ADCs is limited by low input bandwidth and high aperture uncertainty. Significant fundamental advantages of photonic devices are their wide bandwidth and superior timing accuracy. To combine the advantages of both technologies, we investigated a photoconductive-sampling-based photonic analog-to-digital (A/D) conversion system utilizing low-temperature-grown GaAs (LT-GaAs) metal-semiconductor-metal (MSM) photoconductive switches which were flip-chip-bonded with silicon-CMOS ADCs and demonstrated a two-channel prototype system with ~ 3.5 effective-number-of-bits of resolution over an input bandwidth up to 40 GHz and an estimated sampling jitter of less than 80 fs.

This thesis focuses on three approaches to the integration of ultrahigh-speed GaAs photoconductive switches with Si CMOS to form an ADC system. LT-GaAs was chosen as the best candidate material due to its unique property of (sub)pico-second carrier lifetime which provides ultra-fast switching and its reasonably high carrier mobility to provide good responsivity. Using an electro-optic sampling technique, high-speed characterization of the MSM switches exhibited ~ 2 ps full-width at half-maximum switching window. By optimizing the growth and anneal conditions of LT-GaAs, we significantly improved the switch responsivity. As a

result, the optical pulse energy needed to trigger the switches was reduced from > 310 pJ to ~ 50 pJ per pulse for the prototype system.

One of the key innovations of this work was the monolithic integration of GaAs switches with Si CMOS circuits to minimize input parasitics. The common approach for monolithic integration is to grow GaAs device layers onto the Si CMOS wafer prior to metallization steps and then finish the metallization steps after the growth of the GaAs devices. However, this creates significant fabrication complications due to the mismatch between different equipment used to fabricate Si circuits and GaAs devices and potential cross-contamination issues. Since high-speed MSM devices utilize controllable material defects to shorten carrier lifetime, we explored the possibility of directly growing GaAs films at low temperatures on top of completely fabricated Si chips to enable on-chip monolithic integration. The most critical issue is not to damage or modify the characteristics of the underlying Si circuits by the GaAs film growth and device processing steps.

We investigated two alternative options. First was to grow LT-GaAs on Si substrates and the second was to directly grow GaAs on dielectric-coated Si substrates which simulate the actual surface of a finished chip with passivation. All the growths were done at temperatures safe for a completed chip. Switches made from both materials show comparable or even better responsivity and speed combination than their counterparts on a GaAs substrate.

As a final proof-of-principle demonstration, we directly grew a polycrystalline GaAs film on top of a completely finished CMOS amplifier chip previously designed for flip-chip bonding and obtained a properly functional optical receiver without modifying the performance of the Si circuit. In addition to the multiple advantages brought by monolithic integration, the beauty of our approach is its simplicity, minimum fabrication disturbance, which is limited entirely to the tail-end Si processing, thus having much greater applicability into a broader range of applications, such as optoelectronic interconnects. To our knowledge, this is the first time a fully monolithic on-chip integration has been successfully achieved.

Acknowledgments

Over the years, many people have helped me in one way or another. This work would not have been possible without their support and advice.

First, I'd like to especially thank my advisor Professor James S. Harris, the "Coach", who kindly offered me the opportunity to pursue a new direction in my career a few years ago. He was always encouraging, which helped me form a positive life attitude. He is most famous for creating a unique environment where students have the maximum freedom to explore their own research interests (no matter how wild they are). In addition to his title as the advisor, he cares for his students much beyond the research itself. Whenever I felt pressure and talked to him, he always told me cheering stories, passed on valuable experiences, and eased my worries with humor. Thank you very much, Coach! I will always remember the laughter.

I'd like to further thank my Ph.D. orals and thesis reading committee members, Professor David A. B. Miller, Professor William D. Nix, Professor Zhenan Bao, and Professor Mark L. Brongersma. Their insightful and supportive feedback has been very helpful. This project was a collaborative effort between several research groups in the Electrical Engineering Department, including Professor Miller, Professor Bruce A. Wooley, and Professor R. Fabian Pease's groups. In particular, I would like to thank Professor Miller for being a key contributor and bringing his expertise in photonics to this project. I have been deeply impressed by his innovative ideas and keen insights into problems. He was also very generous to allow me full access to his

labs so that I was able to perform all my optical measurements. Since the first day I came to Stanford, Professor Nix has always made me feel at home. He treats all students as his kids, as his friends, and as equals. He is always available to patiently provide line by line detailed explanation to our questions. I am especially impressed by his demonstration of the true spirit of being a great teacher.

I also express my sincere gratitude to the faculty in the Materials Science and Engineering Department who educated me through classes and in other ways. Particularly, I am sincerely grateful to Professor Robert Sinclair, who introduced me to the beauty of Transmission Electron Microscopy. In spite of his unbelievably busy schedule, Professor John Bravman still managed to provide me dearly needed help when I asked. I am indebted to Professor Shan Wang for many delightful discussions.

Gail Chun-Creech deserves high credit for keeping the Harris group, a very large group, in good shape. She has been a good friend to me and helped me with various administrative issues. I truly appreciate her wonderful job which has made my life much easier and enjoyable. As a “prior generation grower”, Glenn Solomon has been very generous in sharing his experiences. He was always willing to physically help us whenever we have problems with MBE systems.

Several students in Professor Miller’s group actively collaborated in this project. Without Ray Chen’s optical receiver chip and his help in testing, I would not have been able to demonstrate the monolithic on-chip integration. He is also such a good and interesting friend who made the long testing hours very enjoyable. I am very grateful to Ryohei Urata’s great work with the electro-optic sampling setup, which was an indispensable characterization technique for the high-speed switches. I thank Henry Chin for many valuable discussions in the monolithic integration processing and chip testing.

The integration process would not have been accomplished on time without several friends’ selfless help. Dan Grupp, Guanxiong Li, Luigi Scaccabarozzi kindly helped me with e-beam lithography. Tom Carver in Ginzton lab provided precious suggestions in metal contact evaporation and lift-off steps so that we were able to succeed in the first process trial.

I'd like to thank past and present members of the Harris group, for making this group such a friendly and fun place. I especially want to thank Thierry Pinguet, the one who first warmly welcomed me and helped me start in the group. Most of my Stanford time was spent in the MBE lab. I thank my fellow growers, Xiaojun Yu, Junxian Fu, Qiang Tang, Yu-Hsuan Kuo, Mark Wistey, Seth Bank, Homan Yuen, Vincent Gambin, Chien-Chung Lin and Xian Liu for keeping the lab running smoothly, for your "comradery" friendship and our fighting together with the "Mostly Broken Equipment (MBE)", and for bringing laughter when greasing bolts and tightening screws. I thank Paul Lim, Alireza Khalili, Zhilong Rao, Vince Lordi, Seongsin Kim, Tom Lee, David Jackrel and Fariba Hatami for frequent valuable discussions. I thank Rafael Aldaz for maintaining group computers. It is almost impossible to list all the names to whom I am grateful. But I should say, it is you, my fellow group members, who have made my time in the Harris group so enjoyable and full of wonderful memories.

I benefited from many insightful discussions with Yaocheng Liu, He Li and many lab members in CIS. I am also grateful to my many friends, either in the US or in China, with whom I never feel lonely.

National Semiconductor generously provided all the CMOS chips used in this work. This work was supported by DARPA/PACT (under contract no. DAAD17-99 C-0048) and MARCO. I personally also want to express my gratitude to the Stanford School of Engineering Fellowship and Komag Inc. for their financial support.

Finally, the most important element in my getting to this stage of my life is the support and love from my family. I thank my dear parents, parents-in-law, brothers and sisters-in-law for their unconditional love. My daughter Karly is the one who keeps me motivated to my work. I thank my husband and best friend Tao, for his love and patience. I am not afraid of challenges in my life, because I know, no matter what happens, he is always there, to comfort, to share, and to help solve my problems. I always have a sturdy shoulder upon which to rest, to laugh, and to cry.

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Chapter 1

Introduction

1.1 Motivation

1.1.1 Importance of A/D conversion and its applications

Today we are living in an information age and everyday we receive a huge number of signals. Almost all naturally occurring signals are continuous-time, analog signals, exhibiting forms of light, sound, images and other electromagnetic waveforms. During the past three decades, the rapid progress of digital technology has led to ever more powerful digital signal processing systems with much lower cost and vastly better performance. The many benefits of digitization include better noise immunity, simplified data storage, easier design and test automation, lower power dissipation, extensive programmability and much more. It is not an exaggeration to say that the combination of powerful digital signal processing and digital computing have changed the way we live everyday.

The key element to interface between the natural continuous-time analog world and the discrete binary digital systems world is an analog-to-digital converter (ADC). This circuit has very wide applications due to the incentive to realize the above mentioned benefits of digitization and to process signals by powerful digital circuitry.

ADCs are used virtually everywhere whenever an analog signal is to be processed and stored in digital form. These include speech, music, telephone, consumer electronics, medical imaging, radar, test equipment, such as sampling oscilloscopes, and telecommunications, etc. R. Walden provided an excellent summary of ADC applications according to sampling speed. Fig. 1.1 is a summary plot taken from his 1999 ADC presentation posted on the internet [1].

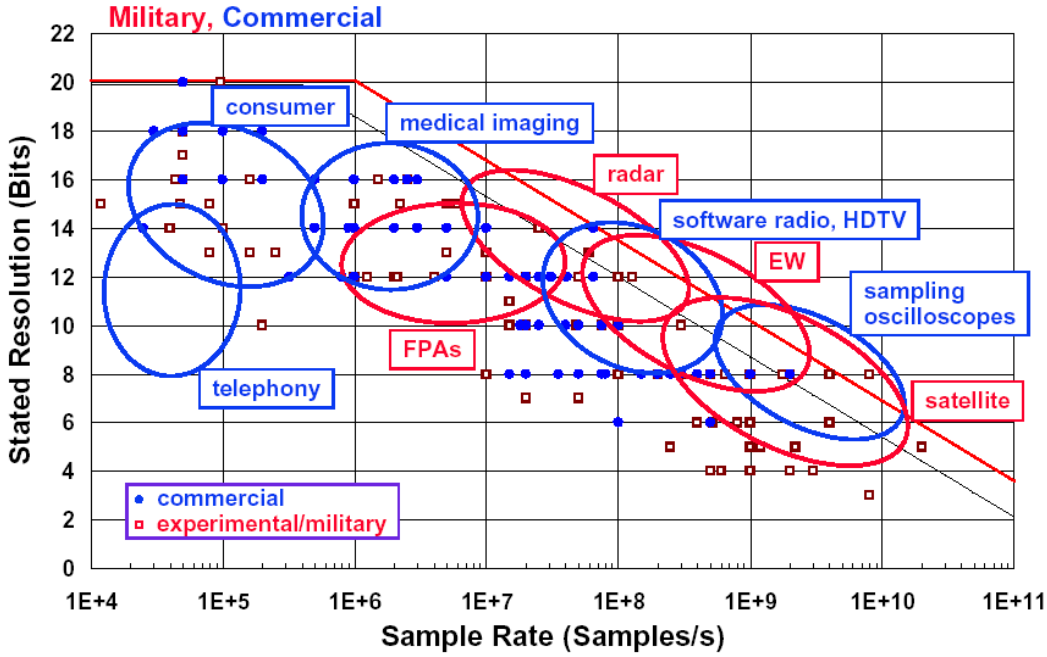

Figure 1.1. ADC applications according to the sampling speed [1].

1.1.2 Brief introduction to ADCs

According to Wikipedia [2], an analog-to-digital converter (abbreviated ADC, A/D or A to D) is an electronic integrated circuit, which converts continuous signals to discrete digital numbers. The reverse operation is performed by a digital-to-analog converter (DAC) and is generally used to convert digital information back to sound or video for human recognition.

Using an input time-varying voltage as an example, an electronic ADC needs to perform two functions: to sample the analog signal in time and hold the resulting voltage until it can be read out; and to quantize the held voltage into a number of digital levels. An analog signal can be understood as a signal having infinite resolution, while a digital signal always has finite resolution. Thus the process of converting an analog signal to a digital one inevitably causes some distortion. Fig. 1.2 [3] is an arbitrary example showing an input analog time-varying voltage (in green), the sampled and digitized signal version (in red) and the calculated quantization error (in blue) which was the difference between the actual input signal and the quantized version.

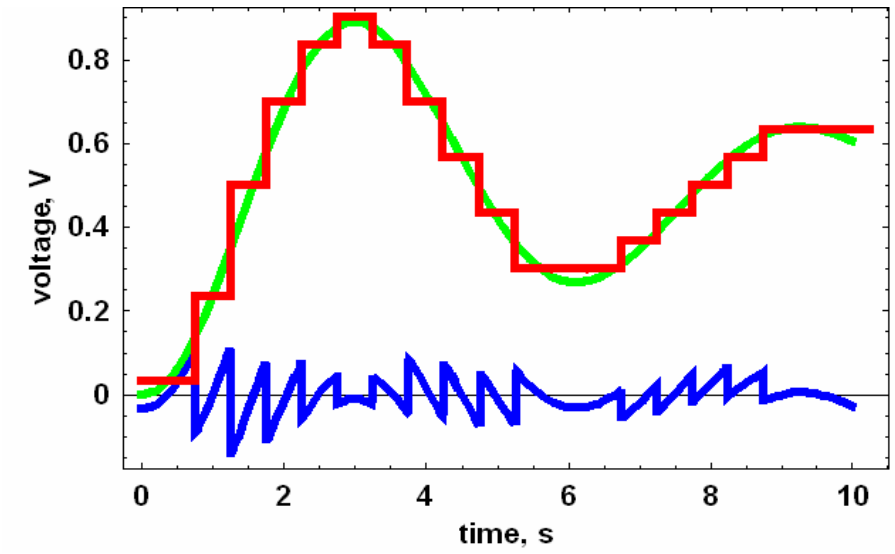

Figure 1.2 An example of an input analog voltage as a function of time (green), the sampled and digitally quantized voltage (red) and the quantization error (blue) [3].

The two main figures of merit for an ADC are the frequency of the sampling (the sampling rate) and the number of levels (resolution). Usually the number of levels is given by 2 to an integer power (2^n, n is called the number of bits) so that a 1024-level ADC is a 10-bit ADC. Errors in both timing and amplitude decrease the ADC performance. The most important timing errors are random jitter and broadening of the sampling time. The main factors that cause error in amplitude are thermal noise and

nonlinearities. Due to these errors, the effective resolution of an ADC is usually expressed as the effective number of bits (ENOB), which may not necessarily be an integer [3].

Typically, a conventional ADC is an all-electronic device that converts an input analog voltage (or current) to a digital number. However, progress for electronic ADCs has not been as fast as the processing power of digital circuitry. Aiming to close this gap for high speed applications, there have been intensive research efforts since the mid of 1990s in the area of photonic ADCs. The concept of photonic ADCs was first proposed by Taylor in 1979 [4].

ADCs have been studied extensively for several decades due to their importance as critical devices to connect the analog and the digital worlds. If you type "ADCs" in "keywords" in EI™ or INSPEC™, you will get more than 20,000 records. If you instead type in "Photonic ADCs", you will still get more than 400 hits and most of them are published during recent years. The in-depth study of ADCs can be found in many text books (for example, ref. [5]) and technical articles. For example, a wonderful book that includes both the basics of A/D conversion and the technology of photonic A/D conversion is B. L. Shoop's "Photonic Analog-to-Digital Conversion" [6].

1.1.3 Limitations of state-of-the-art all-electronic A/D converters

Conventional ADCs are all-electronic. Walden [7] conducted a thorough survey of the then-current state-of-the-art electrical ADCs in 1999. He summarized over 150 ADCs, made by different manufacturers, including experimental systems and commercially available parts, and mapped out the performance of these ADCs based on the sampling rate and the resolution (in SNR bits). These ADCs are mostly made in silicon, although a few are made in GaAs and InP.

Walden used signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) as main performance figures of merit when evaluating the ADCs. This is

because SNR and SFDR are the most accurate measures of dynamic performance which is most important for high speed applications that we are addressing here.

Fig. 1.3 is a summary plot taken from R. H. Walden's 1999 survey of electronic ADCs [7]. In this plot, each dot represents an ADC. The signal-to-noise ratio is expressed as effective number of bits according to

$$\text{SNR-bits} = (\text{SNR (dB)} - 1.76)/6.02 \qquad (1.1)$$

The four sets of lines and curves show the ADC performance limitations caused by thermal noise, aperture uncertainty (or aperture jitter), comparator ambiguity and the Heisenberg limit. Assume T = 300 K for the thermal noise curves. Aperture jitter is calculated for Nyquist sampling, i.e. $f_{sig} = f_{sample}/2$. Comparator ambiguity is determined from the regeneration time constant of the circuit technology.

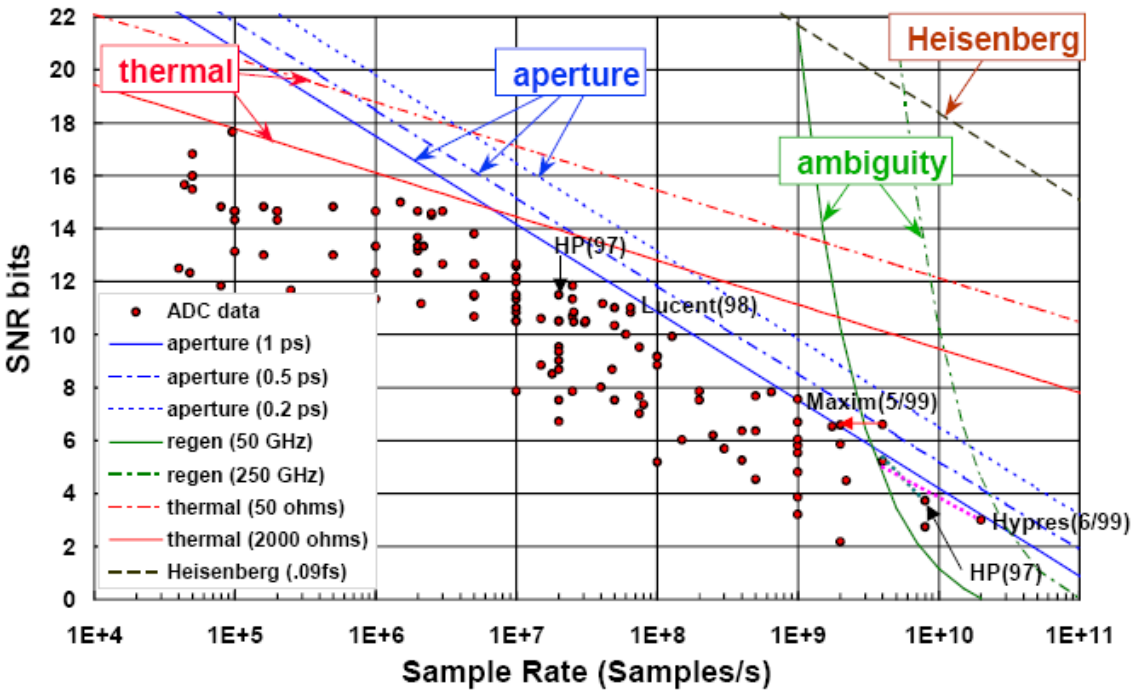

Figure 1.3 R. H. Walden's 1999 survey of electronic ADCs. In this plot, each dot represents a reported AD converter. The signal-to-noise ratio is calculated according to SNR bits = (SNR (dB)-1.76)/6.02. The four sets of lines and curves show the ADC performance limiters caused by thermal thermal noise, aperture uncertainty, comparator ambiguity and the Heisenberg limit. Assuming T = 300K for the thermal noise curves. Aperture jitter is calculated for Nyquist sampling, i.e. $f_{sig} = f_{sample}/2$. (Plot taken from Ref. [1])

In general, increases both in the sampling rate and the resolution are desired. A universally used measure of ADC performance, P, is the product of the effective number of bits and the sample rate.

From Fig. 1.3, by watching the distribution of the dots, we notice that there seems to be a technology barrier to arbitrarily increasing the resolution with speed. At lower sampling rates, ADC performance is mainly limited by thermal noise. At high speed, the technology barrier we have seen corresponds to 0.5 to 2 ps aperture uncertainty. In this plot, aperture jitter is the main factor limiting the resolution for a wide range of sampling rates from a few MS/s to mid of GS/s. Aperture uncertainty, also called timing jitter, means the sample to sample time variation at the moment when an input signal is sampled. Because the affected sampling rates have such a big range, the aperture uncertainty is a dominant factor when developing high speed ADCs.

Over the 6-8 year period studied in this survey, transistor speed increased by at least 6 times due to CMOS scaling. The performance of CMOS based devices also increased proportionally. But ADC resolution only increased by 1.5 bits in SNR. After performance limitation analysis, Walden summarized that technical challenges for the ADC resolution-speed product improvement are:

1) Reduction in aperture uncertainty
2) Increase in the maximum sampling frequency
3) Accomplishing the above two goals while maintaining low power consumption.

The aperture uncertainty of the electrical system is decreasing relatively slowly. Answers to above challenges prompt us to consider photonic technology due to its extremely low timing jitter and high bandwidth.

Assuming timing jitter is the sole source of error, the allowable timing jitter for a Nyquist ADC is calculated as a function of sampling speed and resolution. The results are illustrated in Fig. 1.4 [7-10].

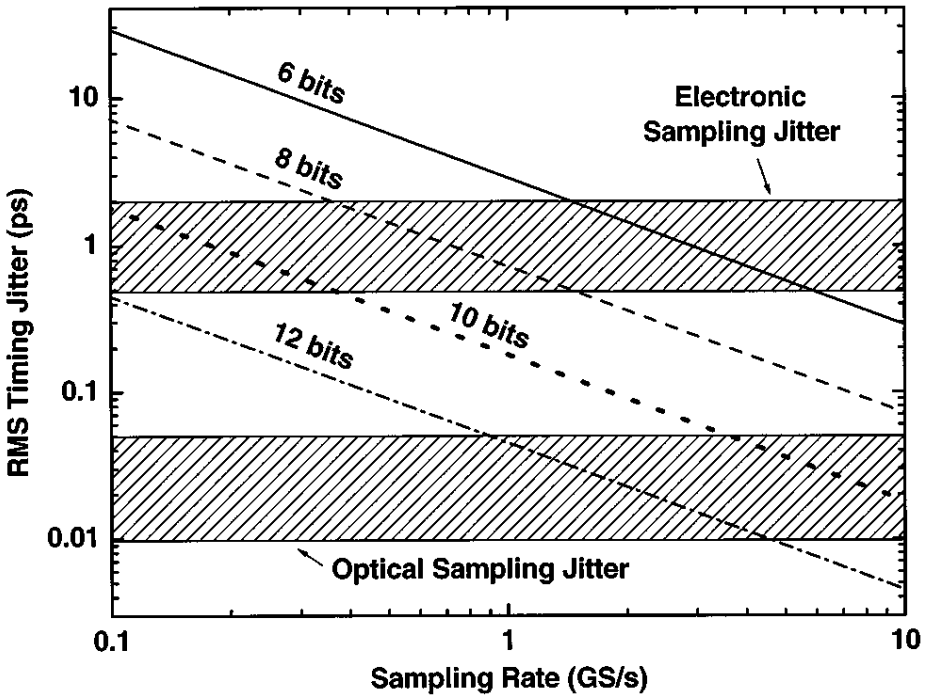

Figure 1.4 Assuming timing jitter is the only source of error, calculated timing-jitter requirements for ADCs as a function of sampling rate and number of effective bits. The hatched areas indicate the recent years' electronic and optical sampling-aperture jitter ranges and the data are from ref. [7-9]. This plot is taken from ref. [10].

1.1.4 Photonic A/D conversion system

1.1.4.1 Hybrid photonic/CMOS A/D conversion system

ADCs have different applications according to their speed and resolution. Our work intends to address the highest speed applications. For example, modern tele- and wireless communications, advanced radar, and high-speed instrumentation require much higher speed ADCs with bandwidths on the order of several tens of GHz or higher.

Conventional all-electronic ADCs are extremely powerful in signal processing, low in power consumption, and compact. However, we have seen that their

performance at high speed is limited by low input bandwidth and fundamental timing jitter problems which causes sampling aperture uncertainty. On the other hand, photonic devices have high bandwidth and superior timing accuracy advantages (state-of-the-art jitter < 50 fs), although their signal processing capability is inferior to electronic devices. In addition, optics offers the promise of parallel information processing. Therefore a hybrid system could potentially combine the advantages of both technologies to achieve superior performance. A/D conversion has two functions, sampling and digitization. We use optical sampling to extend the performance of electronic ADCs. In our approach, the sampling function is performed in the optical domain and quantization is still performed in the electronic domain to harness the electronic benefits.

Based on this idea, we proposed a hybrid photonic/CMOS analog-to-digital (A/D) conversion system utilizing a sample-and-hold scheme with low-temperature-grown GaAs (LT-GaAs) metal-semiconductor-metal (MSM) photoconductive switches. LT-GaAs was used to obtain short carrier lifetimes, therefore, short sampling pulses. This is important in achieving ultra-short (in ps) switch turn-off time and therefore a short sampling aperture and high sampling rate. Note: The materials choice of the photoconductive switches is the major part of this study. Other materials including poly-GaAs were explored and details are reported in the main body of this dissertation.

In order to achieve high input bandwidth in this system, the switches would be triggered by fs-order optical pulses (we proposed to use a mode-locked laser pulse train with 1 GHz repetition rate) to sample the input electrical signal onto a hold capacitor. Sampled data would later be digitized at a slower rate using CMOS ADCs attached to the sample and hold circuit. We use a time-interleaved parallel architecture with multiple channels to achieve an ultra-fast aggregate sampling rate. This dissertation mostly focuses on the materials development of the photoconductive switching function. The details of the other parts of our A/D conversion system can be found in four published papers [11-14] and Urata [15] and Nathawad's [16] Stanford University Ph.D. dissertations as well.

Figure 1.5 is a schematic diagram of our proposed hybrid system. One end of the high speed photoconductive switch is attached to an electrical transmission line and the other end is attached to a hold capacitor. When the input signal propagates down the transmission line, the switch would be triggered by a short mode locked laser pulse (in the femto-second range), sampling the corresponding input voltage onto the hold capacitor. This sampled data would then be digitized by a CMOS A/D converter attached to this sample and hold circuit. We proposed to do the optically-triggered sample and hold at 1GS/s rate at each node. By using a time-interleaved architecture with N channels, the ultimate total sampling rate of the whole system is increased, if the mode-locked laser clock is properly phase aligned. With this structure, the short-pulse mode locked laser provides high bandwidth and accurate clocking. And the high speed photoconductive switches provide a high sampling rate.

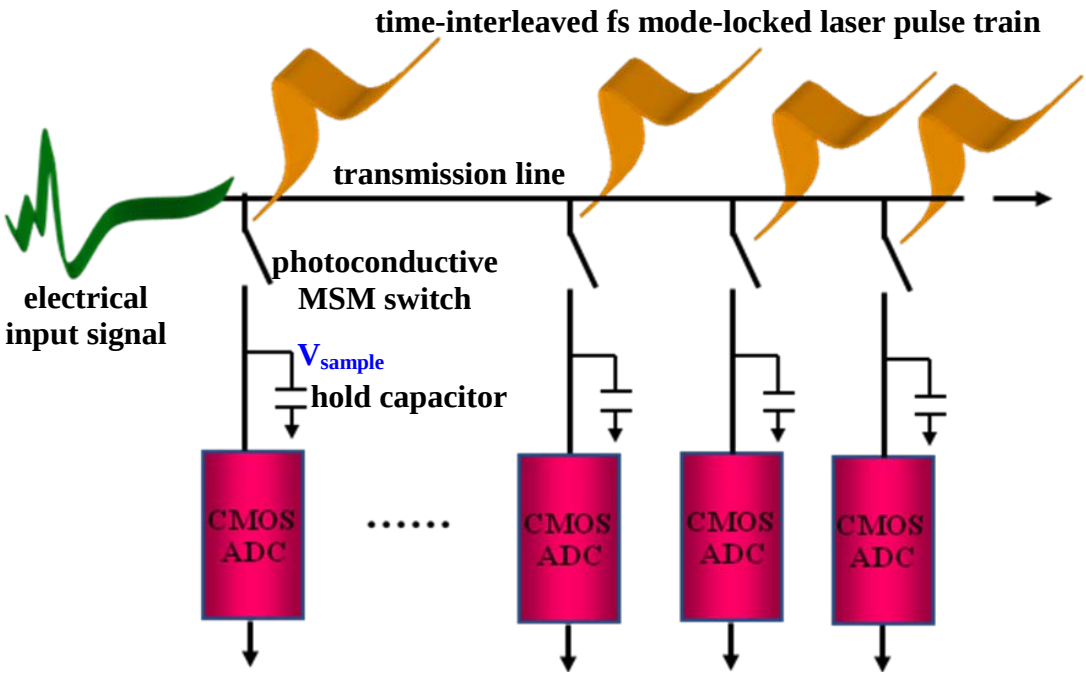

Figure 1.5 Schematics of our photoconductive sampling based photonic/electronic hybrid A/D conversion system.

1.1.4.2 Photonic A/D conversion classification

Our proposed structure to include photonic sampling into an A/D conversion system is not the only approach to provide the benefits of photonics. Literally, the term “photonic ADC” should indicate an ADC in which both the input analog signal and the output digital signal are both in an optical format. However, at least to date, there is still no reported work on such kind of devices. Typically, a photonic ADC means a device with both input and output signals in the electronic domain but utilizing photonics to assist in the process of digitization.

Since Siegman and Kuizenga reported work on optical sampling of RF signals in 1970 [17], there has been a tremendous amount of research work done in this area. Since 1990, the progress on photonic ADC development has grown rapidly. A thorough review of the photonic ADC history can be found in Valley’s recent article [3].

Generally speaking, photonic ADCs can be classified into four categories: photonic assisted; photonic sampled; photonic quantized; and photonic sampled and quantized [3]. There are also sub-classes in each category as illustrated in the classification scheme shown in Fig. 1.6.

Photonic assisted ADCs are those ADCs that still perform both the sampling and quantization functions in the electronic domain but use photonics to improve some performance-limiting properties of electronics. Photonic sampled ADCs perform sampling in the optical domain, but quantization is done in electronic domain. Photonic quantized ADCs are the opposite, that is, sampling is done in electronic domain while quantization is done in optical domain. As the name indicates, photonic sampled and quantized ADCs are those that both the sampling and quantization are done in the optical domain.

According to this classification, our system, a photoconductive-sampling-based A/D conversion, belongs to the photonic assisted ADCs. Flip-chip bonding is used to combine the LT-GaAs photoconductive switches and the Si-CMOS based ADC circuits.

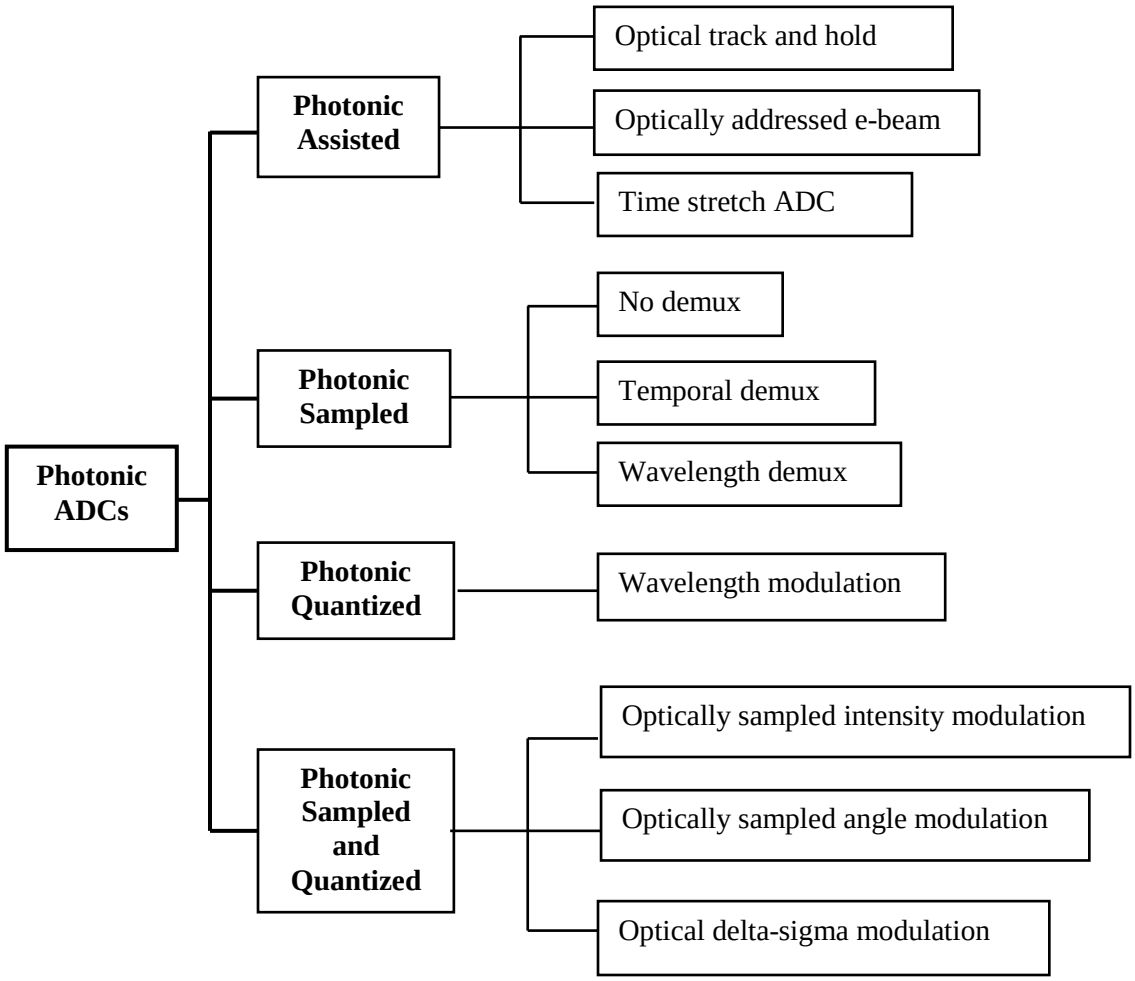

Figure 1.6 Photonic ADC major classification.

1.1.5 Fast photoconductive materials

In our proposed A/D conversion scheme, the multiple photoconductive sampling gates that can produce picosecond times for sampling at high speed are key components. It is imperative to make photoconductive switches with a very short switching window for our system to function as designed.

The switching window includes pulse rise time and fall time. The intrinsic quantum mechanical photoconductive generation process is very fast, the speed with

which carriers are produced is limited only by the uncertainty principle, although the actually measured rise time of a photo-generated electrical pulse depends on the triggering laser pulsewidth and circuit parameters.

The pulse fall time primarily depends on the carrier lifetime of the material. It is possible, with circuit complexity and devices with ultra-small dimensions, to generate short electrical pulses using materials with long carrier lifetimes. But the preferred straightforward option is still to reduce the carrier lifetime and directly generate short pulses.

The general approach to shorten carrier lifetime is to introduce deep-level defects into the material in order to function as traps and recombination centers. Over the years, several techniques have been used. One is to dope with compensating impurities. An example is Cr-doped GaAs [18, 19]. But the lifetime realized by this process is still in tens of picoseconds (50 – 100 ps). Another approach is to use damage induced by high energy particles, such as ion-implantation or proton bombardment to create radiation damage defects [20-23]. 0.5 – 0.6 ps carrier lifetime were reported for proton-irradiated GaAs [20] and oxygen-ion-implanted silicon-on-sapphire (SOS) materials [23, 24]. The main drawback to this approach is that the carrier mobility resulting from these harsh damage processes is too low. Anneals are usually required to improve mobility, but the desired defects then largely removed during the anneal. Amorphous semiconductors have also been studied [25, 26], but the mobility is also low. The grain boundaries in polycrystalline materials usually act as effective trapping and recombination centers [27]. Another ideal candidate for high-speed applications is low temperature growth of semiconductors where the lifetime can be reduced to sub-picosecond range [28].

Both low-temperature-grown GaAs (LT-GaAs) and arsenic-implanted GaAs were our initial candidates when choosing the material to fabricate the sampling gates. LT-GaAs was our final choice for the photoconductive switches due to its excellent properties, especially those suitable for ultrafast switching applications and due to a more thorough understanding of this material after many years' intensive research on this interesting material, which started in 1987 [28, 29]. In addition, LT-GaAs is a

convenient choice if doing epitaxy while the As-implanted GaAs is simpler from process integration point of view. Since we are an MBE group and we do epitaxy for most of our GaAs devices, choosing LT-GaAs was a naturally preferred decision. LT-GaAs grown on both GaAs and Si substrates were studied in this work. In addition, when considering the possibility of monolithic integration of GaAs-based switches with Si CMOS ADCs, polycrystalline GaAs material was also investigated. The following chapters describe detailed studies on these fast photoconductive materials.

1.1.6 Monolithic integration of GaAs devices with Si circuitry

In our A/D system with photoconductive sampling, the entire set of gates, sampling capacitors, and CMOS A/D circuits are ideally integrated onto one chip, thus rendering a small and compact system with short signal propagation distances and therefore a simple RF design. To integrate the GaAs-based opto-electronic devices, such as the MSM switches, with the low power Si-based CMOS ADCs, there can be two approaches. One is a hybrid technique in which the GaAs devices are solder-bonded onto the Si chip using methods such as flip-chip bonding. This is exactly how we achieved our prototype ADC system. Another potentially more desired approach is to monolithically grow the GaAs films on top of the Si chip to further minimize the parasitic capacitances and to allow for smaller photoconductive switches with lower power consumption. Analysis shows that reduction of input capacitance also improves gain/noise limits.

With the challenges brought by more complicated interconnections and thermal dissipation, the scaling of silicon electronic chips and systems has been more difficult and its progress is not in concert with the transistor’s own performance advancement. From the point of view of optical devices and systems, integrating with electronics also promises new functionalities. Therefore there has been a strong motivation for combining optics (usually compound semiconductor technology such as GaAs) and electronics (silicon CMOS technology) at the chip level [13, 30-34].

For decades, monolithically integrating GaAs devices with Si CMOS circuits has been a long-standing goal for many research groups [35, 36]. Most of the time, the research focus was on achieving similar performance for devices made from GaAs films grown on Si substrates compared to those made from conventional high quality GaAs epitaxial films. Due to the difficulties created by crystalline defects caused by the lattice and thermal mismatch, the results have been unsatisfying. Therefore, the direct growth approach has largely been abandoned. However, the desire for monolithic integration has remained strong in the research community and it has spurred a great amount of work to find solutions to the difficulties.

In our ADC system, the need for high-speed sampling gates requires us to produce fast photoconductive materials and LT-GaAs is our choice. In this application, we purposely use controlled material defects to reduce carrier life time without an unacceptable reduction of the carrier mobilities. Therefore, a certain quantity of crystal defects are not only tolerable, but even welcome. Due to this consideration, we believe the monolithic integration of directly grown GaAs on Si finds a niche here. Obtaining insights from LT-GaAs, we are even confident that we should be able to directly grow GaAs on top of completely finished Si chips, at low temperatures. Detailed work on this approach is reported in later chapters.

1.2 Dissertation outline

This work is mainly aimed towards studying high-speed photoconductive materials for the fabrication of wideband photoconductive switches used in photoconductive-sampling-based photonic analog-to-digital (A/D) conversion systems, one example being described in the above introduction. In particular, much effort was invested in monolithic integration of the switches with completely fabricated CMOS chips.

Specifically, this work includes four main aspects. The first part is to optimize the LT-GaAs material grown on GaAs substrates to obtain a good combination of the shortest possible carrier lifetime and highest possible carrier mobility, which translates to high speed and high responsivity of the photoconductive switches made from it.

The material has been successfully utilized in our prototype two-channel system to make metal-semiconductor-metal (MSM) switches that were integrated with CMOS A/D converters using flip-chip bonding hybrid integration technique. This part of work is described in Chapter 2.

The second part of my work is to explore the monolithic integration possibility of high-speed LT-GaAs photoconductive switches with completed Si CMOS integrated circuits, hoping to minimize input parasitics. In addition, in the flip-chip bonding technique, the GaAs substrates are etched at the last step. When considering bonding multiple devices onto a silicon chip, this waste of expensive GaAs material substantially increases the fabrication cost. Therefore, direct growth of GaAs thin films on silicon chips will greatly help cost reduction. We have grown GaAs directly on Si substrates at low temperatures (~ 250 °C). The wafer cleaning and film growth temperatures are chosen at levels safe for finished CMOS circuits. Time-resolved electro-optic sampling characterization shows that the performance of LT-GaAs switches on a Si substrate are comparable to their homoepitaxy counterpart which was used in our prototype ADC with demonstrated outstanding performance. The successful low-temperature growth of GaAs on Si substrates promises the possibility of monolithic integration of ultra-fast LT-GaAs switches with Si CMOS circuits. Chapter 3 focuses on this technology.

The third part of my work is to further explore the idea of growing “fast materials” suitable for ultrafast photoconductive switches on top of finished Si circuits. Modern ICs usually have at least 5-6 electrical interconnect metal layers above the Si substrates. To grow LT-GaAs on Si, deep etching is needed to expose the Si material. To simplify the processing and make the approach more general, we studied the direct growth of polycrystalline GaAs material on top of SiO_2, which is generally available on top of almost all the finished ICs as the insulation layer. Characterized using the electro-optic sampling method, the MSM switches made from poly-GaAs grown on SiO_2 demonstrated quite comparable performance regarding speed and responsivity to the LT-GaAs on GaAs and LT-GaAs on Si materials we studied in this thesis. Therefore, this approach is the most promising for monolithic

integration of GaAs-based photoconductive switches with finished Si integrated circuits. The growth of poly-GaAs on top of SiO_2 can be easily extended to growth on top of Si_3N_4 if a nitride film is the final isolation layer, as is the case for many devices. This part is described in Chapter 4.

Chapter 5 discusses successful monolithic integration of GaAs switches with a completely fabricated CMOS amplifier. After integration, we achieved a functional optical receiver without degrading the Si circuit performance. To our knowledge, this is the first work reported of a monolithic integration of GaAs devices with a completed Si CMOS circuit.

Another part of my responsibility in this multi-group DARPA/PACT project was to help design and grow thin film structures used as negative electron affinity (NEA) photocathodes in the LAVAMAC (Laser-strobed Vacuum-Microelectronic Analog to Digital Converter) approach to high-speed photonic ADCs. This is an innovative electron-optical approach for ultra-high speed A/D conversion, which allows for 100 GHz bandwidths using the principle of electron beam deflection A/D conversion. Fig. 1.7 shows the concept of this optically triggered e-beam ADC [37, 38]. This structure also made a good use of the advantages of a mode-locked laser: short pulse width, low timing jitter and high repetition rate. The details are described in Ioakeimidi's Ph.D. thesis [39] and several published papers [37, 38]. This work will not be included in this dissertation.

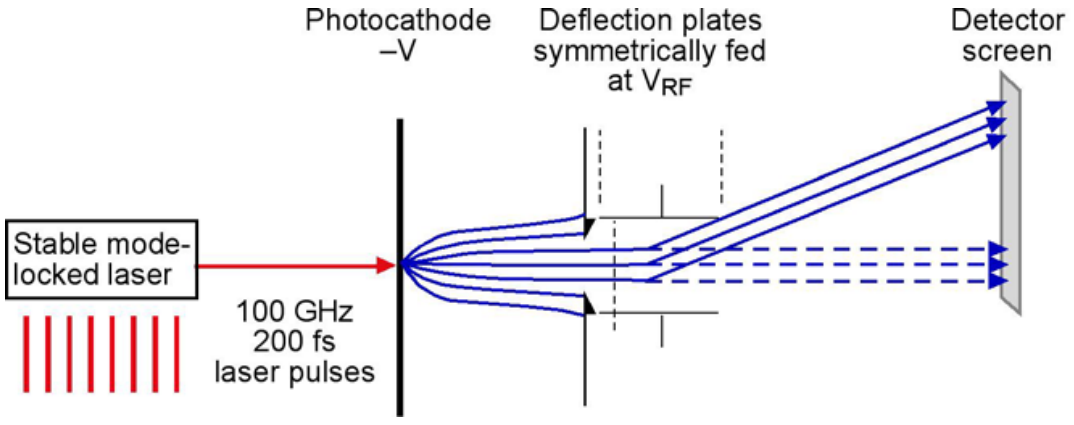

Figure 1.7 Illustration of the LAVAMAC, an optically triggered e-beam ADC [37, 38].

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Chapter 2

LT-GaAs on GaAs Substrates and MSM Switches

This chapter introduces a special type of GaAs film that was usually grown at low temperatures by molecular beam epitaxy (MBE) on GaAs substrates. The low temperature GaAs film (LT-GaAs) has a series of unique properties that make it an ideal material candidate for the high speed photoconductive switches used in our photoconductive sampling A/D conversion system. The film is characterized by measuring the speed and responsivity of the metal-semiconductor-metal (MSM) switches made from it. The MBE film growth process is studied to obtain an optimal combination of the shortest possible carrier lifetime and the highest possible carrier mobility. The LT-GaAs MSM switches were intimately combined in our prototype two-channel A/D conversion system using a flip-chip bonding hybrid integration technique.

2.1 Background

2.1.1 Molecular Beam Epitaxy

2.1.1.1 Overview

All the thin film materials used in this thesis were grown by molecular beam epitaxy (MBE) on a Varian Mod Gen II system.

The concept of MBE appeared in the 1960s [1]. As a means of depositing high-purity and high crystalline quality epitaxial films, MBE was mostly developed in the early 1970s, when Arthur [2] studied the reaction kinetics of Ga and As_2 beams on GaAs surface, and when Cho [3, 4] adapted electron diffraction to *in situ* monitor the surface structure during film growth. Since then it has not only become a major technique for growing III-V and II-VI compound semiconductor films, but also a versatile tool to explore new thin film materials in both research laboratories and industries. Despite the common (mis)conception of its "low" growth rate and throughput, it has even been widely used in the compound semiconductor industry on a mass-production scale to fabricate sophisticated electronic, optoelectronic and magnetic devices. The main reasons for its success are its great flexibility in control of film thickness, composition, and doping profile; its atomically abrupt interfaces; and extensive *in situ* analysis and monitoring of the growth process.

Conceptually MBE is a simple physical vapor deposition (PVD) technique. The constituent elements of a film are in the form of fluxes of "molecular beams" and are deposited onto a usually heated substrate to form thin epitaxial layers with desired composition. The beams are typically from thermally evaporated or sublimated high purity solid elemental sources (solid source MBE). The reactions of one or more such beams with typically high quality single-crystal substrates produce epitaxial films.

There are also other types of sources, such as metal-organic group III precursors (MOMBE), gaseous group V hydride or organic precursors (gas-source MBE), liquid sources (liquid source MBE), or some combination (chemical beam epitaxy or CBE). In this thesis, we used solid source MBE.

Due to the requirement for high film purity, the entire system, including the material sources and the process chamber, have to be put in an ultra-high vacuum (UHV) environment (~ 10^{-10} torr or below). Under UHV, the mean free paths of the evaporated atoms (or molecules) are on the order of meters, much greater than the physical dimension of the MBE chamber. Therefore, the source material fluxes are in the molecular flow regime and behave like "beams" that can be deposited ballistically onto the substrate, ignoring scattering or precursor interaction in their path. The clean setting coupled with independent and precise control of different source fluxes make it possible to fabricate superlattices and heterostructures at single atomic layer dimensions. It is also due to this UHV environment that multiple surface-sensitive diagnostic techniques that need high vacuum can be used to monitor the growth process *in situ*, such as Reflection High Energy Electron Diffraction (RHEED), mass spectrometry, X-ray or Ultraviolet Photoemission Spectroscopy (XPS or UPS), and Auger Electron Spectroscopy (AES). This is a very significant advantage of MBE compared to other epitaxy techniques, such as Metal Organic Chemical Vapor Deposition (MOCVD) or Liquid Phase Epitaxy (LPE).

Primarily due to the UHV environment, MBE growth process does not occur at thermal equilibrium. It is limited by surface kinetics, such as atomic or molecular adsorption, migration and desorption, when the impinging species react with the substrate. Figure 2.1 shows major surface atomic processes happening during MBE growth [5]. Take GaAs as an example, the basic process is a first order chemisorption of an As_2 molecule on a surface Ga atom. There are also possible association reactions to form As_4 at lower temperatures and dissociation of GaAs at higher temperatures.

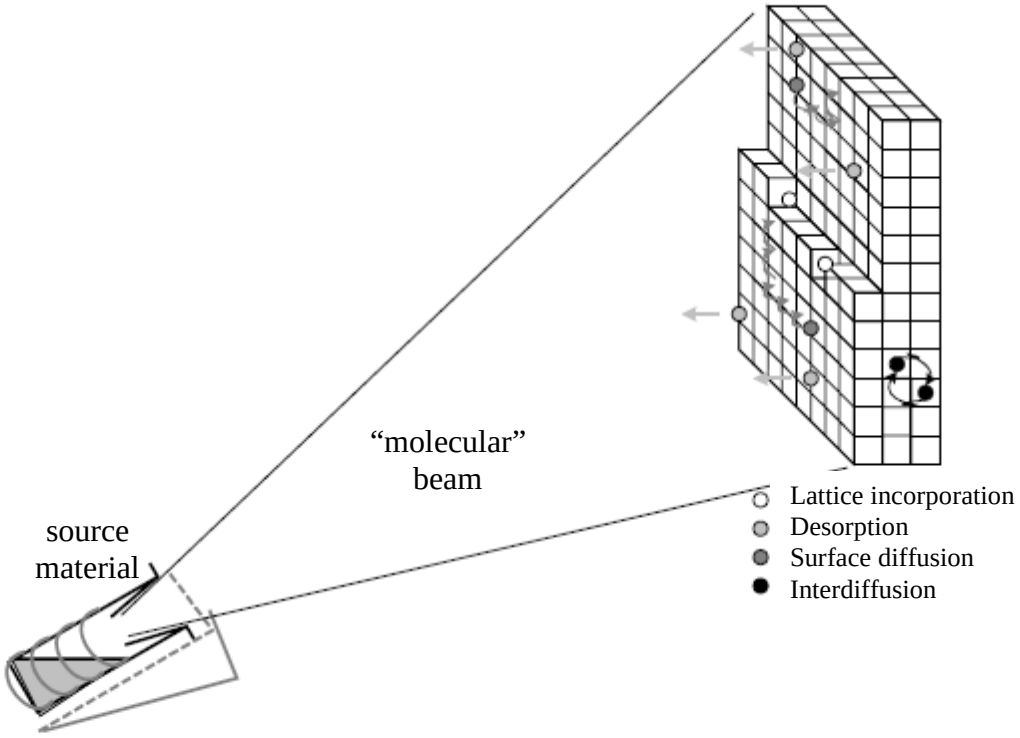

Figure 2.1 Schematic of the atomic processes occurring during MBE growth.

Figure 2.2 shows a schematic illustration of the Varian Mod Gen II MBE chamber. Typical Gen II chambers contain eight Knudsen effusion cells where the constituent materials and dopants of the films are heated. Sometimes electron-beam guns are used for materials with very high melting temperatures. Typically used group III materials are gallium (Ga), aluminum (Al), and indium (In), and they usually provide molecular beams by thermal evaporation. The dominant group V materials are arsenic (As), phosphorous (P) and antimony (Sb). The arsenic flux is formed by sublimation of elemental As as a tetramer molecule, As_4. As_4 has a lower sticking coefficient than dimmer As_2 and is not the equilibrium species over heated GaAs. Therefore As_2 can be absorbed more efficiently into the film and consume less As. Some research has also suggested that using As_2 resulted in better growth due to a simpler incorporation mechanism than As_4. Therefore As_2 is usually favored during MBE growth of GaAs. As_4 is usually cracked to As_2 in a cracker cell. The cracker cell is composed of a lower temperature sublimator section in the bottom and a high

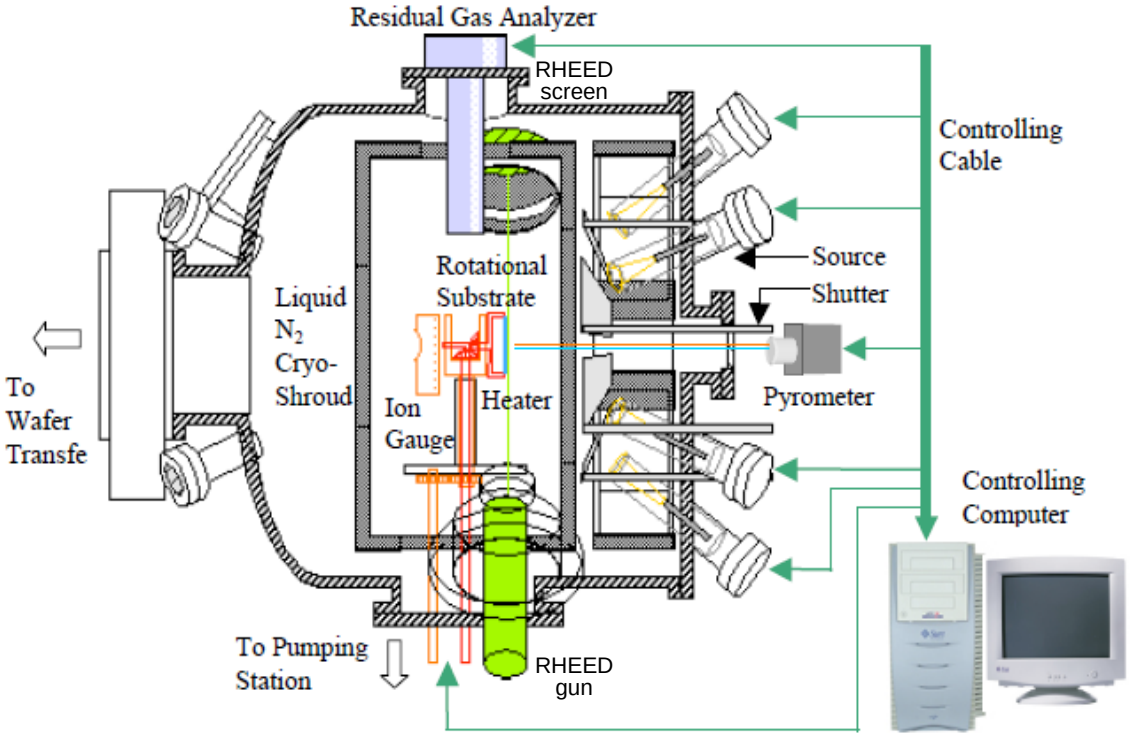

Figure 2.2 Schematic of the Varian Gen II MBE growth chamber. Sources and shutters at the right, loading gate valve at the left, RHEED gun at the bottom, mass spectrometer and RHEED screen at the top, and the sample and beam flux ion gauge at the center of the drawing [6].

temperature cracking zone where As_4 vapor is superheated. The sublimation zone temperature determines the arsenic flux. Usually there is a needle valve placed between the two zones to control how much arsenic flux is released into the growth chamber.

There is a mechanical shutter in front of each cell to open or block the corresponding beam. The cell temperature controls evaporation rate and hence the beam flux. A typical growth rate is around one monolayer per second or ~ 0.5 μm/hr, and shutters open and close in less than 0.1 second. By setting cell temperatures properly and cycling the shutters, the composition, layer thickness and doping can be controlled on a sub-monolayer scale.

Arsenic does not stick to an As-terminated surface, but the sticking coefficient is 1 on a Ga-terminated surface. Therefore, the GaAs growth rate is determined by the

Ga beam flux, although almost all III-V MBE growth is done under As-rich conditions to insure that Ga droplets do not form on the surface.

Our system consists of two Gen II growth chambers coupled by a UHV wafer transition tube. A magnetically controlled wafer trolley is used to hold and transport wafers under high-vacuum between the two chambers. The LT-GaAs films reported in this chapter were mainly grown in one chamber, which is used to grow arsenides. The other chamber, which is usually used to grow group IV materials (Si and Ge) was used when exploring LT-GaAs growth on Si substrates (reported in the next chapter). The capability of coupling the two chambers with more material sources by a vacuum tube enabled more possibilities of growth patterns and films with sophisticated composition combinations. Wafers first enter a low vacuum chamber through a gate-valved load-lock chamber. The load-lock is initially pumped and the wafer is baked to remove moisture and organic contamination. Then the wafer is moved to the buffer transition tube and eventually to the growth chamber without breaking vacuum.

To learn more about MBE, a good reference that includes details of most of the important aspects of MBE is reference [7]

2.1.1.2 Reflection High Energy Diffraction (RHEED)

The fact that MBE takes place in a UHV environment allows the use of reflection high-energy electron diffraction (RHEED) as an *in situ* tool to monitor how atoms arrange themselves on the substrate into a periodic structure. RHEED systems gather information only from the surface layer of the sample. Therefore it is a technique used to characterize the surface of crystalline materials.

RHEED has been extensively utilized in MBE to monitor the growth of the films and to optimize surface morphology and growth conditions. A basic RHEED system consists of an electron gun for electron source, a fluorescent screen (or a CCD camera) for diffraction pattern recording, and of course, a sample to be detected. The electron gun is placed at glancing angle (~ 0.5 – 2 degrees) relative to the sample surface in order to detect only the surface. Fig. 2.2 shows the layout of the gun, the sample and the screen. When the incident electrons strike the sample, they are

diffracted by the surface atoms. The diffracted electrons interfere constructively at certain angles according to the crystalline structure, the atomic spacing on the surface, and the wavelength of the incident electrons. They annihilate otherwise and form a regular diffraction pattern on the detector. The specific diffraction pattern is a direct indication of the surface crystallography during film growth so it has been used in almost all MBE systems to monitor the surface change instantaneously. Also the intensity of each spot on the pattern fluctuates periodically due to the evolution of the relative surface coverage of the growing film. Each oscillation period corresponds to the deposition of one monolayer. RHEED intensity oscillations were first reported in 1981 [8] and have been used widely to quickly and accurately calibrate growth rate.

Overall, RHEED can be used to observe surface oxide desorption, to calibrate growth rate and substrate temperature, to monitor surface atomic arrangement and surface morphology, to determine the proper As overpressure, and to provide growth kinetic information. It is by far the most useful *in situ* monitoring tool used in MBE.

One important use of the RHEED diffraction pattern is to qualitatively provide surface condition information. For example, when the surface is smooth, flat and single crystalline, the diffraction patterns are clear and streaky. When the surface is rough, the streaks change to be spotty and the pattern is diffuse and un-clear. Amorphous surfaces are hazy on the screen and polycrystalline surfaces show ring patterns.

An example of an arsenic-terminated (100) GaAs surface RHEED pattern is shown in Fig. 2.3 [9]. The GaAs symmetry can be determined by observing the RHEED pattern in two orthogonal <110> azimuths. From a reciprocal lattice-Ewald sphere analysis, the main ordering direction displays a two-fold periodicity while the orthogonal direction displays a weaker four-fold periodicity. The primary reconstruction is reflected in the two by four periodicity. This streaky (2×4) surface reconstruction pattern is typical for a good quality As-terminated traditional GaAs (100) surface. The diffraction pattern has GaAs primary lines corresponding to the lattice structure. In addition to that, “2×” along [011] crystalline direction means the secondary lines have half of the spacing of the primary lines and the “4×” along [$01\bar{1}$]

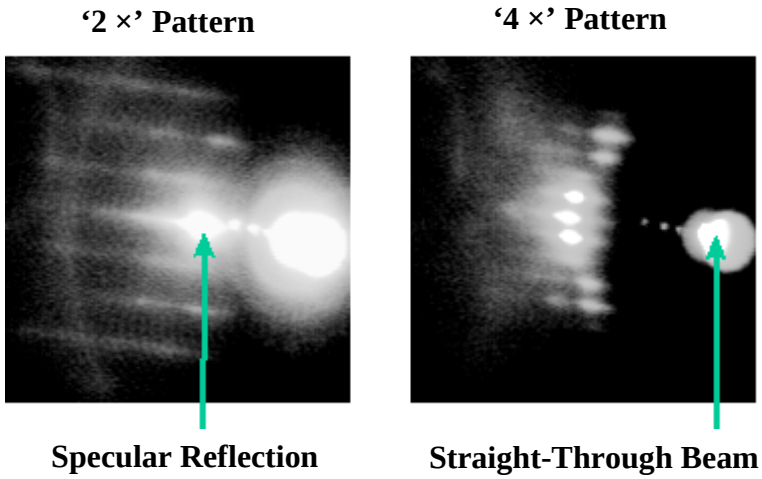

Figure 2.3 RHEED (2x4) pattern of an arsenic-terminated (100) GaAs surface at 600ºC. The (2 x) pattern has the electron beam pointed along the [011] azimuth and the (4 x) pattern is along the [$01\bar{1}$] direction.

direction has secondary lines with a quarter of the primary lattice spacing. What this really tells us is that the GaAs surface atomic cell has a surface lattice unit cell that is 2 times by 4 times larger along these two directions, compared to the bulk material.

2.1.1.3 Substrate temperature determination

The most important growth factor in MBE, or maybe any kind of thin film deposition technique, is temperature. It is the key that impacts all aspects of the thin film quality. It influences the incorporation and redistribution of atoms, impurities, deep levels, and lattice defects. It also influences interface roughness and surface morphology. But it has been historically difficult in MBE to accurately determine the substrate temperatures.

Although thermocouples are installed on the sample holders, usually on the back, it usually has not only large but also non-fixed temperature offsets with respect to the sample surface. Thermocouple measurement was more accurate in the early days of MBE development, when the samples were mounted to the substrate holders by In-bonding. Newer MBE machines mostly use non-In-boned, radiatively heated

substrate holders. For example, in our lab, the wafers are mounted on ring-shaped molybdenum substrate holders by tantalum wires. The temperature uniformity is largely improved and many un-desirable growth nuisances associated with In-bonding are removed. However, the thermocouple no longer intimately contacts the wafer and senses a combined signal from the wafer, the substrate heater, the holder, and at times, even the hottest source cells. The thermocouple location is also a strong factor affecting the temperature reading. It is not surprising to observe a 100 – 200 °C error with the thermocouple reading. Accurate substrate temperature measurement during MBE growth remains a problem and we must be especially careful when comparing experiments reported by different labs.

Other than thermocouple, another commonly used temperature measurement tool is an optical pyrometer operating upon a black body radiation principle. Since it is a non-contact and vacuum compatible temperature sensing method, it is an attractive substrate temperature measurement technique during MBE or MOCVD growth. However, it is not problem-free either. The main limits of traditional pyrometry are substrate transparency (semiconductors are transparent for wavelengths below the bandgap and this transparency causes low substrate emissivity and optical interference from other hot elements in the chamber), bandgap shifts, viewport coating, alignment and optical obscuration errors, pickup of stray light and multilayer interference effects, etc [10].

In our lab, we combine multiple temperature measurement methods together, trying to achieve as accurate, reproducible and consistent temperature calibration as possible. A two-color (dual-wavelength) SVT infrared pyrometer was used to measure wafer temperature and to calibrate thermocouple reading. This pyrometer is specifically designed to avoid the viewport coating problems and instrument alignment errors. We used several well-established known temperatures together to calibrate the pyrometer itself. These include: GaAs surface native oxide desorption temperature at 582 °C [11]; the In melting temperature at 157 °C and Si-Al eutectic temperature at 577 °C. We also referred to different transition temperatures corresponding to various surface reconstructions using RHEED [12].

A pyrometer measures the thermal radiation signal emitted from the wafer surface. The blackbody emission is mainly in the infrared for typical MBE growth temperatures. Pyrometers are usually not sensitive to emission below 400-450 °C. Our group explored accurate ways [13, 14] to measure MBE substrate temperatures that can be extended to low temperatures by measuring the GaAs bandgap from transmission caused by radiation from the substrate heater or an external light source. GaAs is a direct bandgap material. It has a well defined sharp absorption edge. Accurate temperature information can be derived by properly extracting the absorption characteristics. This is very accurate if executed carefully because the temperature dependence of the GaAs bandgap is well defined as following:

$$E_g(T) = 1.519 - 5.405 \times 10^{-4} T^2 \quad /(T + 204) \quad eV \qquad (2.1)$$

where T is the temperature and E_g is the bandgap. One note to be considered is that, the doping level uncertainty of the bare GaAs substrate and the dopant influence on bandgap temperature dependence can add some degree of error. While this technique may yield some variation in absolute temperature, it is extremely reproducible from run-to-run [15, 16].

2.1.2 Low temperature GaAs (LT-GaAs)

2.1.2.1 Introduction

High-speed photoconductive switches are key components for the implementation of our proposed A/D conversion system. We chose LT-GaAs to fabricate these switches due to its excellent properties, especially those suitable for ultrafast switching applications and due to a more thorough understanding of this material (compared to other “fast” materials) after many years’ intensive research starting in 1987 [17, 18].

In traditional III-V growth, a GaAs wafer is usually first ramped to the As desorption temperature (~ 350 °C) when the As flux is turned on to prevent substrate As loss. Then at ~ 582 °C, RHEED is used to monitor surface oxide blow-off. Substrate temperature is usually raised to ~ 600 °C and held for ~ 15 minutes to fully

remove native oxide and possible remaining wafer contaminants. Although modern GaAs wafers are “MBE-ready”, a relatively thick GaAs buffer layer (~ 1 μm) is still typically grown to further flatten the substrate surface and to block any possible defects from the substrate. When the temperature is too high (> 650 °C), the Ga sticking coefficient will be less than unity. Therefore, the best film quality and smoothness of GaAs is achieved at a growth temperature around the oxide desorption temperature, ~ 580 - 600 °C. Films grown under this condition have shallow donor and acceptor concentrations in the range of 10^{13} cm^{-3}, and deep traps at least an order of magnitude lower. AlAs can maintain a unity sticking coefficient to higher temperatures, even above 700 °C. The highest quality AlGaAs films are usually obtained about 20 °C hotter than GaAs. So when people talk about GaAs and AlGaAs films, they are usually referring to the films grown within these “traditional” temperature ranges.

In 1987, a group of researchers (Frank Smith, Robert Calawa and coworkers) at MIT Lincoln Lab discovered that growing GaAs at low temperatures, around 200 - 300 °C resulted in structurally excellent material with unique properties of high resistivity and ultra-short lifetime that enable them to be used in a variety of device applications to achieve record performance. In their earliest research [17] particularly, they solved the long-standing sidegating and backgating problems associated with GaAs integrated circuit technology by using annealed low temperature grown GaAs (LT-GaAs) as a very high-resistivity buffer layer. They also achieved record high output power density and superior microwave-switch performance when LT-GaAs was used as a gate insulator in a metal-insulator-semiconductor field effect transistor (MISFET). Using this material, high speed and high voltage photoconductive switches have also been demonstrated. Researchers at the University of Michigan demonstrated high responsivity (0.1 A/W) and wide-bandwidth (~ 375 GHz) photodetectors using LT-GaAs [19]. They predicted that LT-GaAs could be optimized for systems applications to enhance system performance and enable new systems for military and commercial applications in the areas of radar, communications, instrumentation, and high-speed computing. Since this time in the 1990s’, there has been a burst of research

interest in the low temperature MBE growth of films, not only on GaAs but also on other compound materials as well.

2.1.2.2 LT-GaAs Properties

Due to the very low growth temperature, LT-GaAs is highly non-stoichiometric, with a large density of excess arsenic atoms incorporated into the GaAs matrix during growth, forming a high concentration of As-related deep-level defects. Despite the high concentration of excess As, the crystalline structural quality is still excellent and free of structural defects, such as stacking faults. The unique properties of LT-GaAs come from its non-stoichiometry. The excess As exists in the form of a variety of native point defects, namely arsenic antisites (As_{Ga}), gallium vacancies (V_{Ga}), and possibly some arsenic interstitials (As_i), or complexes of these defects [20]. As antisite point defects are double donors with a trap ioniozation energy near the center of the band gap. Less than 10% of the antisites are ionized, while the majority are neutral. Usually observed concentrations of various defects are: $[As_{Ga}]^0$ $\sim 10^{20}$ cm^{-3}, $[As_{Ga}]^+$ $\sim 5\times10^{18}$ cm^{-3}, and $[V_{Ga}]$ $\sim$ 5×10^{18} cm^{-3}. It has been generally agreed upon in the research community that the most important defect form is the arsenic antisite (As_{Ga}, which is an As atom sitting at a Ga lattice site). It is strongly related to and similar to the extensively studied EL2 defect in bulk GaAs, a deep level defect that leads to the semi-insulating behavior in GaAs. Figure 2.4 illustrates the main types of native point defects existing in as-grown LT-GaAs.

The ionized As_{Ga}^+ was investigated using Electron Paramagnetic Resonance (EPR) [21] and the concentration was found to be around $1\text{-}5\times10^{18}$ cm^{-3}. The observation of neutral As_{Ga}^0 was made using Infrared Absorption (IR) [22]. Also, Liu *et al* determined the neutral and positively charged antisite concentrations independently using Near Infrared Absorption spectroscopy (NIRA) and Magnetic Circular Dichroism Absorption (MCDA) [23]. The results confirmed that the As antisite is the dominant defect and its concentration correlates well with the LT-GaAs lattice strain. Using Positron Annihilation Spectroscopy (PAS), Gebauer *et al* found that only about 1% of the antisites are ionized and compensated by Ga vacancy deep

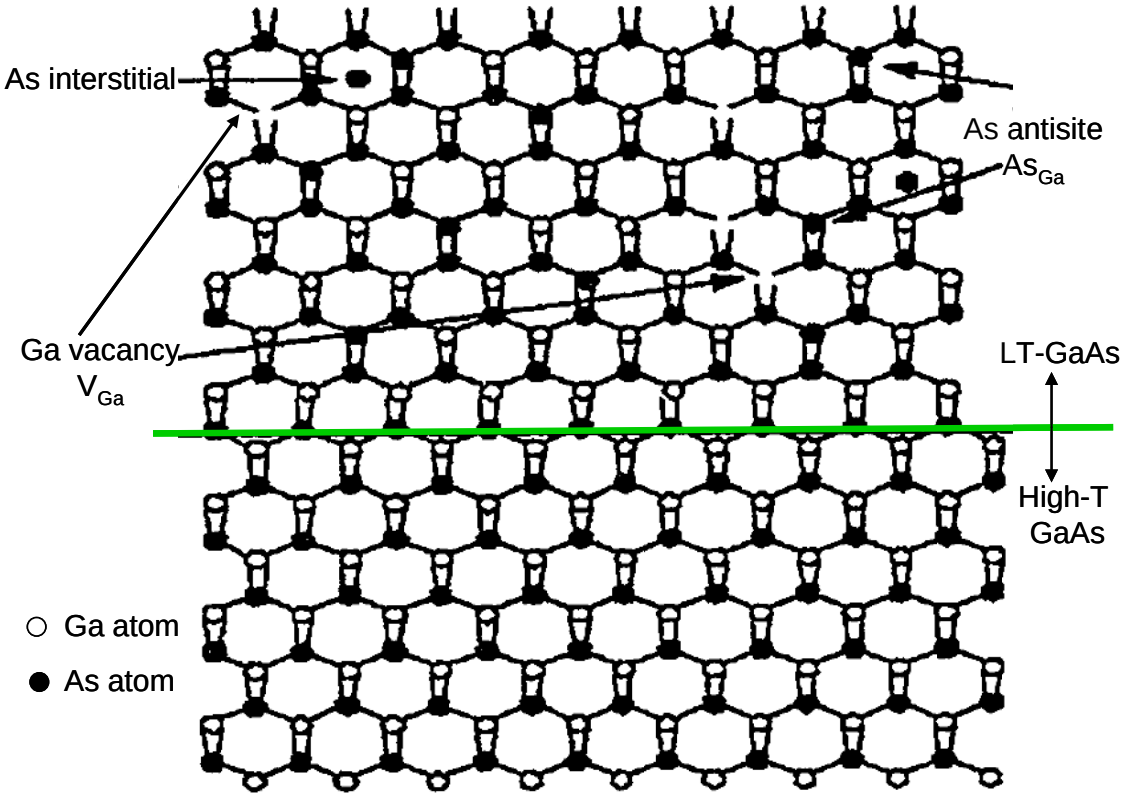

Figure 2.4 Schematics of main types of native point defects existing in as-grown LT-GaAs.

acceptors [24]. Scanning Tunneling Microscopy (STM) [25] also provided direct observation of these defects. Carriers bound to these defects have been found to be responsible for the hopping conduction in the as-grown films [26]. This high concentration of defects creates a large trap density and results in ultra-short carrier lifetime, usually in the sub-picosecond to picosecond range. Due to the massive non-radiative recombination through these mid-gap levels, there is essentially no photoluminescence signal.

As grown LT-GaAs has low mobility and high dark current. Thus a high temperature post-growth anneal above 600 °C (either *in situ* or *ex situ*) is usually utilized to increase the carrier mobility, but not substantially increase the carrier lifetime. After annealing LT-GaAs has very high resistivity (therefore low dark current), high breakdown electric field, a good combination of extremely short photo-

excited carrier lifetime and reasonably high carrier mobility. We will also show later in this chapter that this material has the capability to engineer defects to systematically achieve a tradeoff between speed and mobility. These properties make it ideal for ultrafast photoconductive switch application. Table 2.1 [27] summaries and compares the properties between LT-GaAs and "conventional" MBE GaAs which is typically grown at around 600 °C. Note here that the LT-GaAs properties are for annealed samples. As-grown and annealed LT-GaAs differ significantly in many regards. After sufficient annealing, excess As precipitates to form semi-metallic clusters in the GaAs matrix and the LT-GaAs becomes amazingly a non-stoichiometric material with very high crystal quality, a two-phase composite system with precipitates in an otherwise highly perfect lattice matrix. This differs from other fast photoconductive materials, such as ion-implanted GaAs in that annealed LT-GaAs has much lower degree of mobility-inhibiting damage and thus has a significantly higher mobility.

Table 2.1 LT-GaAs main properties comparison with "traditional" GaAs.

	"traditional" GaAs	LT-GaAs + anneal
Growth temperature	580 – 600 °C	200 – 300 °C
Stoichiometry	1:1 GaAs	~ 1 - 2 at% excess As $Ga_{0.495}As_{0.505}$
Structure	Single crystalline	Single crystalline
Trap density	$< 10^{15}$ cm^{-3}	~ 10^{19} cm^{-3}
Breakdown field	~ 3×10^4 V/cm	~ 5×10^5 V/cm
Resistivity	0.3 – 20 Ω-cm	~ 10^6 Ω-cm
Photo-excited carrier lifetime	~ 1 ns	~ 150 fs
Mobility	7000 cm^2/V-sec	1 - 2000 cm^2/V-sec (depending on growth)
Overgrowth film quality	excellent	excellent

As atoms are bigger than Ga atoms. The As-As bond (2.51 Å in the rhombohedral As crystal lattice) is also slightly longer than the Ga-As bond (2.45 Å). Due to the anti-bonding effect between As antisites and their surrounding As atoms, as well as the possible existence of As interstitials, the incorporation of excess As introduces a lattice expansion and hence a compressive strain in the epi LT-layer. Therefore we see a distinct LT-GaAs peak in as-grown samples in X-ray Diffraction (XRD), as shown in Fig. 2.5, a high resolution rocking curve spectrum, where a 1 μm LT-GaAs film was grown at 250 °C on top of a GaAs substrate with a high quality GaAs buffer layer. The stronger peak corresponds to the GaAs substrate (004) peak with a lattice constant a_0 = 5.653 Å and the weaker peak is due to the LT-GaAs layer. Note that although the film is strained, when the thickness is below the critical thickness, the LT-layer can still be grown pseudomorphically, meaning that the in-plane GaAs lattice constant remains the same as the substrate while the out-of-plane

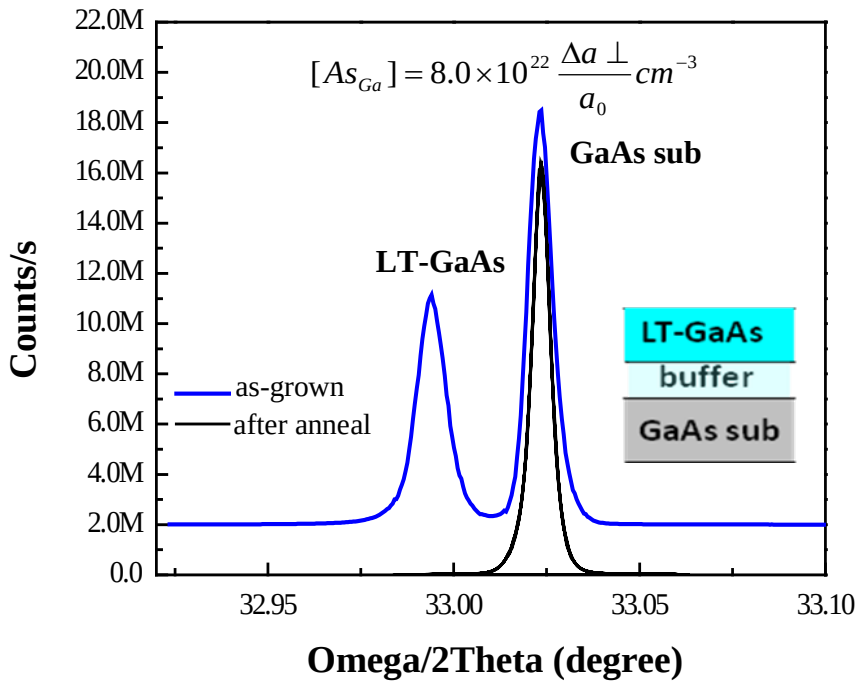

Figure 2.5 XRD of a LT-GaAs epi-layer on top of GaAs substrate. The as-grown film shows the LT epi-layer peak. After anneal, the film relaxes and shows no difference from high temperature GaAs.

lattice constant is elastically distorted to accommodate the strain energy. Beyond the critical thickness, the LT film turns polycrystalline or even amorphous. The critical thickness is a function of the amount of excess arsenic incorporated into the epilayer, which is a function of the substrate temperature, As-to-Ga flux ratio (BEP), etc. Experimental data [20] suggest that the dominant defects responsible for the lattice expansion in LT-GaAs are As_{Ga} defects. According to Vegard's law, the defect concentration is linearly proportional to the lattice strain caused by that defect. The relationship was measured and fit to be [20]:

$$\Delta a_{\perp} / a_0 = 1.24 \times 10^{-23} \cdot [As_{Ga}] \qquad (2.2)$$

where $\Delta a_{\perp} / a_0$ is the out-of-plane lattice strain in the [004] direction, and the unit for $[As_{Ga}]$ is cm^{-3}. Therefore,

$$[As_{Ga}] = 8.0 \times 10^{22} \cdot \Delta a_{\perp} / a_0 \qquad (2.3)$$

Based on this relationship, from high resolution XRD, the concentration of arsenic antisites in the materials we grew is usually found to be in the order of 10^{19} cm^{-3}. This high concentration of defects results in ps carrier life times.

After anneal, the LT-GaAs peak disappears in the XRD spectrum, which means that the excess As which caused the strain is diminished. Where do these As atoms go? Large number of studies indicate that excess As forms precipitates during the anneal and removes the strain. The primary technique to study As precipitates has been Transmission Electron Microscopy (TEM). Fig. 2.6 is a TEM bright field image showing the As precipitates in the GaAs matrix after a 600 °C anneal [28]. It has been found that smaller size (2-3 nm) precipitates are coherent, in a "pseudocubic" or amorphous structure and induce a strain field in the surrounding GaAs matrix; while larger sizes (above 4 nm) are usually a hexagonal, semi-metallic form of As [29]. The number and size of the precipitates strongly depends on the growth and annealing conditions, such as growth and anneal temperature, duration, group V/III beam equivalent pressure ratio (BEP) etc.

The As precipitation process is a solid-solid phase transformation. The solid phase nucleation and growth mechanism can be used to explain the precipitation mechanism in which the final goal is to minimize the free energy of the two-phase

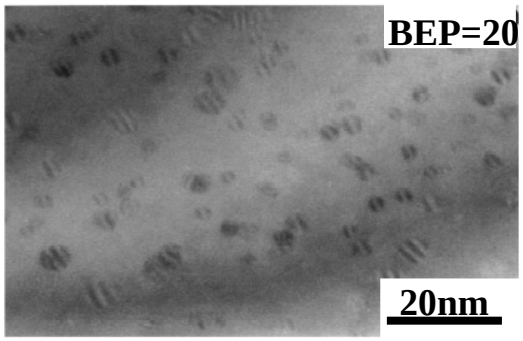

Figure 2.6 TEM bright field image showing As precipitates formed after annealing at 600 ºC in a sample grown at BEP = 20 condition. The precipitates are characterized by Moiré fringes that are typical for hexagonal As.

system. When more than one precipitate exists in the matrix, we can expect that the growth of each precipitate will affect the others to further minimize the total free energy of the whole system by reducing the interfacial area between the As precipitates and the GaAs matrix – a process of precipitate coarsening that is known as "Ostwald ripening" [30].

In the annealing, the presence of Ga vacancies was proposed to enhance the diffusion of As_{Ga} to precipitate. The diffusion and precipitate mechanism could be:

$$As_{Ga1} + V_{Ga2} \leftrightarrow As_{Ga2} + V_{Ga1} \quad \text{(through lattice diffusion)} \quad (2.4)$$

$$As_{Ga2} \rightarrow As_{prep} \quad \text{(form at As precipitate interface)} \quad (2.5)$$

where 1 and 2 mean the two different next-nearest-neighbor sites. Precipitates and point defects are both very important in explaining the unique LT-GaAs behavior, as described in the next section.

2.1.2.3 Models explaining LT-GaAs properties

There have been two dominant but competing models to explain the semi-insulating (SI) nature of LT-GaAs based on whether the excess arsenic exists in the form of point defects or precipitates. Fig. 2.7 illustrates the basics of the two models.

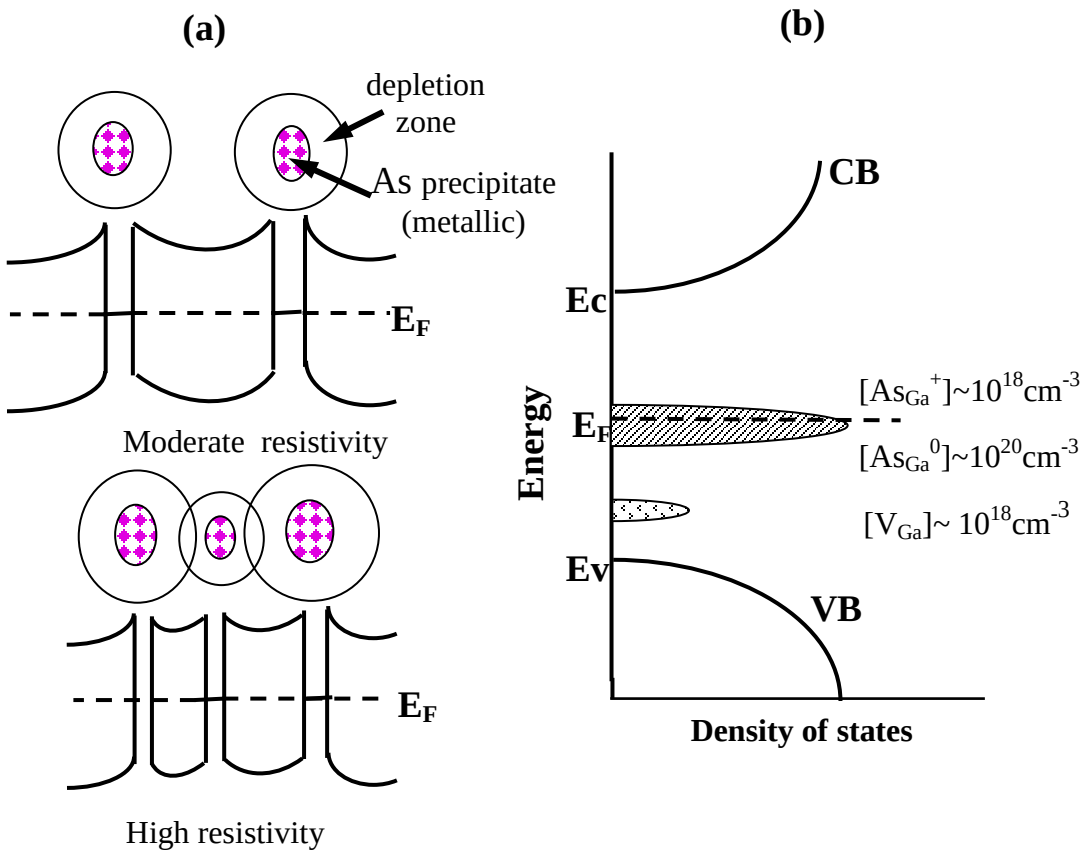

Figure 2.7 The two dominant physical models to explain the LT-GaAs properties. (a) the buried Schottky barrier model. (b) the point defect model.

Look *et al.* [26] proposed the point defect model, which has been applied to explain the EL2 compensation mechanism in SI-GaAs. In this model, the short carrier lifetime can be explained by the fast carrier trapping and recombination in mid-gap levels. As antisites and Ga vacancies have deep levels in the bandgap. Look asserts that the Fermi level is firmly pinned at the midgap As_{Ga} positions. The large density of As_{Ga} yields small distance (~ 1.3 nm) between antisite defects and the wavefunction overlaps. Therefore the conduction in as-grown LT-GaAs is dominated by carrier hopping from occupied to unoccupied antisites. After annealing, the mid-gap state density is reduced by turning antisites into precipirates, hence the samples exhibit higher resistivity by suppressing the hopping conduction.

The other usually cited model is the “internal (or burried) Schottky barrier” model proposed by Warren *et al.* [31], in which As precipitates play a critical role in determining the LT-GaAs properties. Arsenic is semi-metallic and forms a Schottky barrier contact with GaAs with potential barriers. This model assumes that As precipitates are surrounded by spherical depletion regions. For materials with high As precipitate density, these depletion regions overlap and the GaAs is totally depleted, thus shows semi-insulating behavior. These As precipitates also act as effective carrier recombination centers and reduce the photo-carrier lifetime.

Both models are satisfactory only for certain situations and they are usually used complementary to each other.

2.2 LT-GaAs growth and characterization

2.2.1 LT-GaAs film preparation

All samples in this study were grown on semi-insulating MBE grade GaAs substrates in a solid source Varian Gen II MBE system where arsenic is in the dimeric form (As_2) and is provided through a valved thermal cracker. The LT-GaAs layer growth temperatures varied from ~ 200 °C to 350 °C and the V/III element beam equivalent pressure (BEP) ratio varied between 10 and 30. *In situ* RHEED was used to monitor the GaAs wafer native oxide desorption before the growth and the LT-GaAs film evolution during growth. After oxide desorption, we usually grew a high quality GaAs buffer layer about 0.3 μm thick. If samples were to be used in a device processing sequence that needs an etch-stop layer, an $Al_{0.6}Ga_{0.4}As$/AlAs layer would be grown after the buffer and before the LT-GaAs. Then the substrate temperature was lowered to the desired value and the LT-GaAs layer was grown with the desired thickness. Fig. 2.8 shows a typical RHEED pattern development during growth. After the GaAs buffer layer was grown at ~ 600 °C and cooled down to a low growth temperature, the film quality was very good and we can clearly see the streaky 2×4 surface reconstruction pattern (a, b). After the LT-layer was grown, the pattern

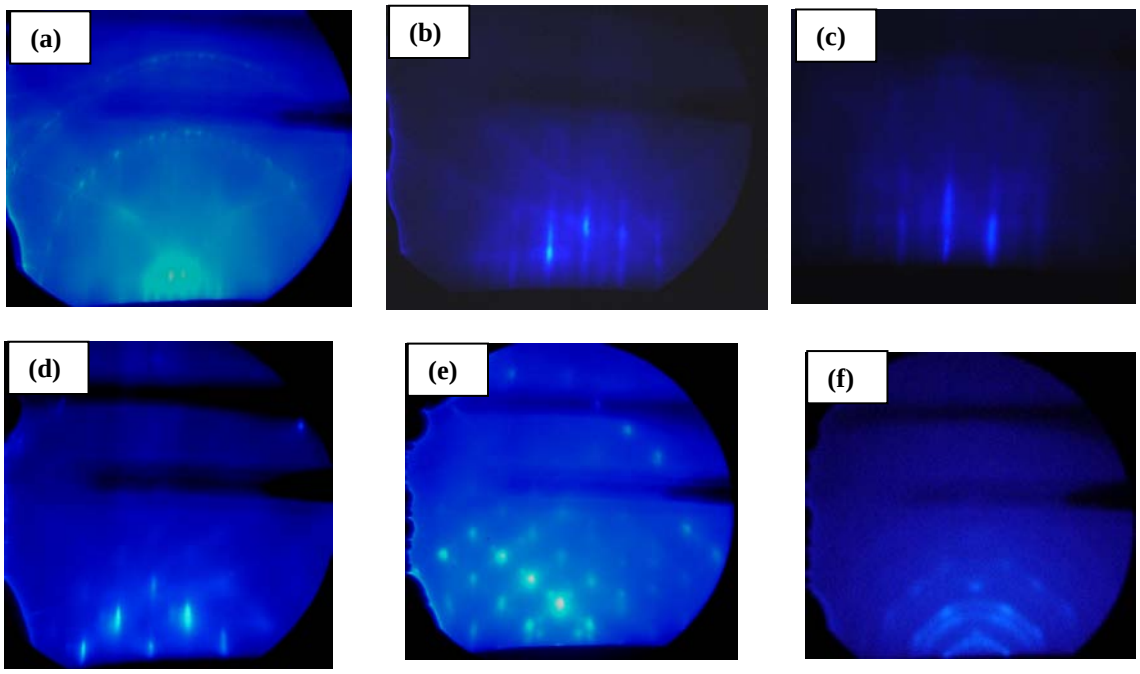

Figure 2.8 Typical RHEED pattern development during LT-GaAs growth.

became 2×1 or 2×2 (c), which is typical for LT-GaAs. If we continue to grow the LT layer thicker than the critical thickness, the streaks first become shorter (d) and then the pattern becomes completely spotty (e), indicative of "pyramidal defects" [32] and "island growth". If we continue to grow an even thicker film at low temperature, the film would finally become polycrystalline, as indicated by the Debye rings (f). The breakdown of single crystallinity of LT-layers at a specific critical thickness may be related to the following possible mechanisms [33]: 1) As agglomeration due to strain; 2) kinetic factors in MBE become dominant due to the low growth temperature; or 3) nucleation of misoriented GaAs at strain-induced nucleation sites caused by the large concentration of excess As. In our samples, we carefully controlled the growth conditions to make sure films prepared for devices have a thickness below the critical value. Therefore the films were of high crystalline quality and free of pyramidal defects.

After growth, the wafers were cut into pieces and annealed at temperatures between 600 ºC and 800 ºC for different time periods (30 seconds to 10 minutes) using

rapid thermal annealing (RTA). To avoid arsenic desorption from the LT-GaAs films during anneal, we covered the LT-GaAs samples with a GaAs dummy wafer on top of the sample to provide an As overpressure environment. The annealed samples were then used in different experiments, including characterization and MSM switching devices.

2.2.2 LT-GaAs carrier lifetime characterization

2.2.2.1 Introduction

We used two time-resolved measurement techniques to characterize the LT-GaAs films and switches made from them. To study carrier dynamics of the film itself in the absence of an external electric field, an all-optical pump-probe transmission technique was used. When characterizing the MSM switches made with the LT-GaAs film and studying the carrier transportation and photocurrent with an applied external electric field, we used an electro-optic sampling method which will be shown in the next section. In this section, the experimental details of the transmission pump-probe technique are briefly shown in order to characterize the LT-GaAs film carrier lifetime. There are at least two benefits to using an all-optical pump-probe technique to study the carrier trapping mechanisms in nonstoichiometric materials such as LT-GaAs. First, since there is no need to make metal contacts on the sample, the sample preparation process is simple. Second, it is usually not easy to electrically inject free carriers from contacts into the semiconductor when the semiconductor material is highly-resistive. Besides the difficulty of carrier injection, the injection speed is also in large part affected by the RC time constant and the structure of the external circuit. Therefore the analysis of the dynamics is not material-intrinsic. Using optical carrier injection, the dynamic range of the carrier density can be very large, and the injection speed is only limited by the pulse width of the injection light sources, usually a mode locked laser [34].

2.2.2.2 Pump-probe measurement setup and results

Figure 2.9 is a schematic of the differential transmission pump-probe measurement experimental setup that we used to characterize the carrier lifetime of LT-GaAs films. As a comparison, we measured the lifetimes of a traditional high temperature GaAs film sample, an as-grown LT-GaAs film and an annealed LT-GaAs sample. The conventional GaAs film was grown at ~ 600 °C with a thickness of approximately 1.5 μm. The LT-GaAs sample was grown at 250 °C with a similar thickness. The annealed sample was heated to 600 °C for 30 seconds. Since we need to measure the transmission and therefore the GaAs substrates need to be removed, an $Al_{0.6}Ga_{0.4}As$/AlAs etch-stop layer was first grown before growing the films that need to be measured. A mixture of hydrogen peroxide (H_2O_2) and ammonium hydroxide (NH_4OH) was used for substrate removal when making the samples.

In the setup schematics, PBS stands for polarizing beam splitter and PD stands for photodetector. In order to study the carrier dynamics and the photoconductive responses of the LT-GaAs that are known to have extremely short sub-picosecond lifetimes, it is necessary to use time-resolved techniques that can measure transients happening within a picosecond or shorter. Therefore a femtosecond pulsed laser is necessary for our pump-probe experiments and electro-optic sampling. The most

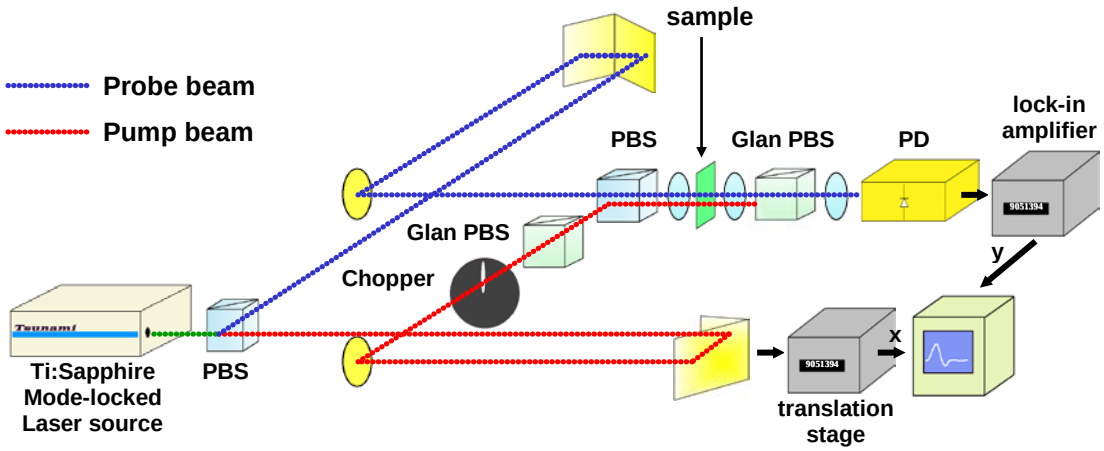

Figure 2.9 Experimental setup of the differential transmission pump-probe measurement used to characterize the GaAs film carrier lifetime.

frequently used femtosecond laser system for the transient measurement has been the mode-locked Titanium-Sapphire laser. Our Ti-Sapphire laser source output pulses have ~ 150 fs full-width at half-maximum (FWHM) and ~ 80 MHz repetition rate. The center wavelength is ~ 850 nm. After leaving the laser source, the laser beam is split into a pump beam with ~ 6 pJ energy and a probe beam with ~ 0.6 pJ energy through a PBS. Following the optical path shown in the setup, the pump beam is focused onto the sample with ~ 20 μm diameter spot size. The pump pulse illuminates the sample and generates electron-hole pairs. After transmitting through the sample and reaching the photodector, the probe pulse detects the carrier behavior as a function of time by adjusting the time-delay (therefore the relative phase) between the two pulses with the translation stage. Due to various carrier-induced absorption effects in the sample, the transmission or reflection of the probe pulse is changed in response to the carrier density in a particular band, including the conduction band, valence band or defect band. By measuring the probe beam intensity change, the time-resolved carrier information can be obtained. Using lock-in detection improves the signal-to-noise ratio. Glan polarizing beam splitters (Glan PBS) are employed to reduce stray pump beam light coupling into the photodetector and saturating it.

The main carrier-inducing transitions in LT-GaAs are valence band to conduction band and the defect band (mainly neutral As antisite band) to conduction band transitions. The absorption effects that affect the optical refractive index or absorption coefficient change, and therefore the transmission change that we measure in our setup, are mainly due to the bandfilling effect. That is, for a fixed photon energy, the absorption coefficient decreases when there are already electrons and holes in the conduction and valence bands, respectively. Therefore the optical transmission increases when a high density of carriers are present. This increase decays as the carriers are trapped, recombine and relax. This process provides carrier dynamic information.

Figure 2.10 shows the normalized results for the pump-probe transmission measurement of a conventional GaAs sample, an as-grown LT-GaAs sample and an annealed LT-GaAs sample. As can be seen, compared to the long carrier lifetime that

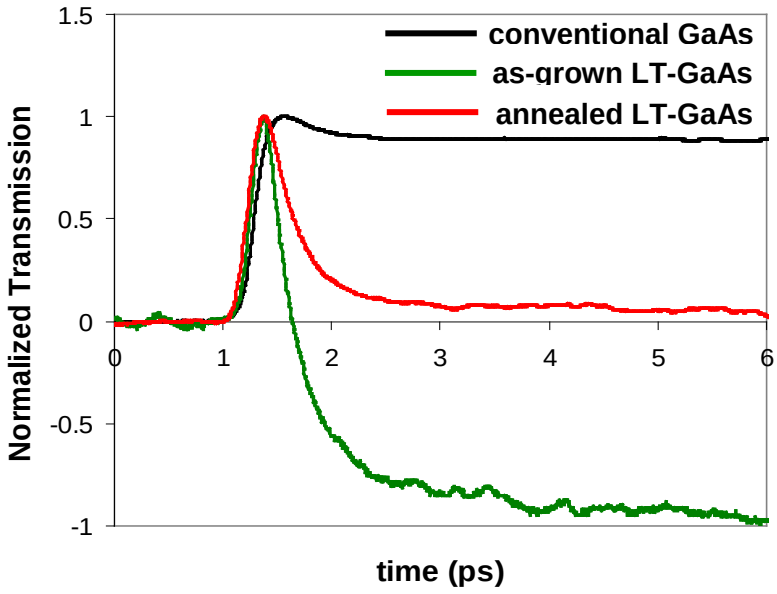

Figure 2.10 Normalized transmission pump probe measurement results for conventional GaAs, as-grown LT-GaAs and annealed LT-GaAs samples.

is in the nanosecond range (too long to show in this plot) of the conventional GaAs film due to the lack of trapping centers, the LT-GaAs samples both show fast transients in the ~ 1 ps range, caused by the carrier-induced transmission increase and a rapid decay because of the carrier trapping due to the existence of the large concentration of defects and precipitates in the materials. One noticeable phenomenon is that there is an induced absorption in the as-grown LT-GaAs sample with a relatively long time constant (a few hundred picoseconds). This can be explained as photogenerated electrons that are initially trapped by the electron traps -- ionized antisites (As_{Ga}^{+}). When the transition of As_{Ga}^{0} to conduction band happens, the trapped carriers are excited again and cause absorption. Due to the physical distance of the electron traps (As_{Ga}^{+}) and the hole traps (V_{Ga}), this recombination process has a long time constant. The annealed LT-GaAs does not have this induced absorption that is caused by carrier re-excitation. This is because annealing significantly decreases the As antisites and forms precipitates. The As precipitates quickly trap and recombine both electrons and holes. This measurement shows that annealing of LT-GaAs causes

only a slightly longer carrier lifetime. Therefore, along with the gain of much higher mobility, annealing of LT-GaAs still preserves the picosecond carrier lifetime and shortens the overall carrier recombination time at the same time.

2.3 MSM switches and high-speed characterization

2.3.1 MSM switch introduction

We need a type of high-speed and sensitive photodetector to be used as the sampling switches in our A/D conversion system. The ultimate speed of a photoconductive switch is determined not only by the semiconductor material of the device, but also by the configuration of its electrodes. To achieve picosecond speed, very short photo generated carrier lifetimes are required. For good sensitivity, high carrier mobilities are needed. Usually defects are introduced into the semiconductor to shorten the carrier lifetime but they generally reduce the carrier mobility at the same time. High speed and good sensitivity are two conflicting goals to achieve in a single detector. As we have discussed above, the engineered LT-GaAs material is a suitable material to achieve a good trade-off between these two figures-of-merit. However, even if the active material itself has a short lifetime, the overall switch speed can still be masked by slower transients caused by parasitic capacitance and inductance of the device electrodes. Thus the switch electrode structure is also equally important.

There are several types of photodetectors used in optical systems, such as vertical structure avalanche photodiodes and p-i-n diodes and surface structure metal-semiconductor-metal (MSM) devices. We chose MSM diodes as our photoconductive switches. These devices were first demonstrated on semi-insulating GaAs by Sugeta *et al* [35]. The main reasons that we chose the MSM structure are due to its process simplicity, high detection bandwidth and good sensitivity. Fig. 2.11 shows a representative pattern for MSM switches. MSMs are mostly made with interdigitated coplanar stripline electrodes deposited on top of the semiconductor material.

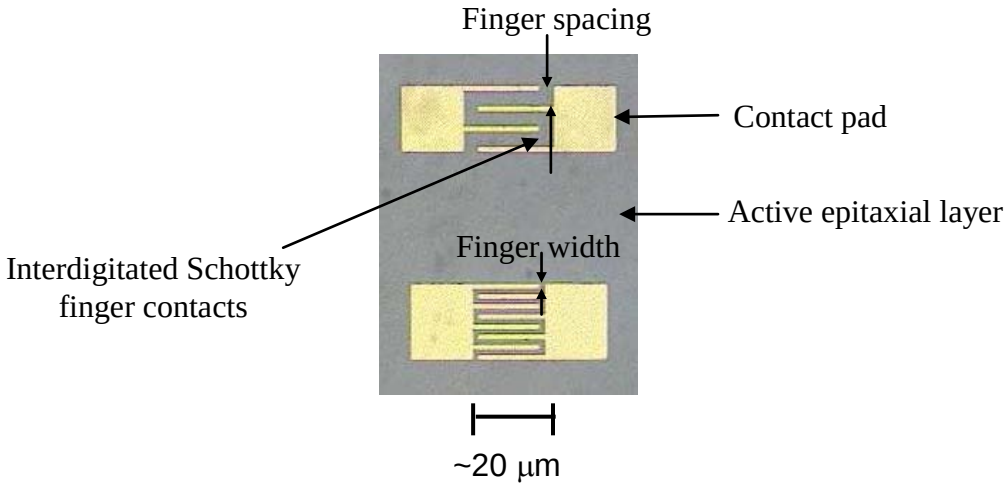

Figure 2.11 Top-view pictures of the typical MSM structures. Yellow parts are metal electrodes. Gray part is semiconductor material.

Photogenerated electrons and holes are collected by opposite contacts biased with suitable voltage to produce a photocurrent. By adopting the interdigitated layout and shortening the electrode finger spacing, the electric field applied on the semiconductor area is increased and the collection of photocarriers is enhanced, improving both the device speed and sensitivity. MSM detectors can be made very fast with detection bandwidth reaching hundreds of gigahertz, making them suitable for high-speed optoelectronic applications.

As can be seen, the MSMs are entirely planar devices and only one type (n or p) of semiconductor is required. Therefore, these devices are very simple to fabricate and are inherently compatible and easy for lateral integration. It is also easy to optimize the switch performance by varying the device geometry, such as electrode finger width, spacing, and size. Usually the dark current of a MSM photodetector is much less than that of other photoconductive detectors because one of the electrodes is always a reverse biased Schottky barrier diode. MSMs are usually illuminated from the top surface, thereby simplifying optical beam alignment. Due to its lateral structure, another important advantage is that MSMs usually have lower capacitance per unit area compared to other types of detectors [36]. Because the only parasitic element is the inter-gap capacitance between two metal electrodes, this can be

decreased to the order of 0.01 pF [35]. Of course, a MSM switch does not come free of any shortcomings. For example, a moderately large portion of the photo-absorption area is masked by the electrical contacts, resulting in an overall responsivity loss by as much as 50%, unless transparent electrodes or backside illumination is used to eliminate the shadowing effect.

2.3.2 MSM switch fabrication

Fig. 2.12 is a schematic of the process flow illustrating the MSM switch fabrication. We employed a standard lift-off process. Starting with a piece of GaAs

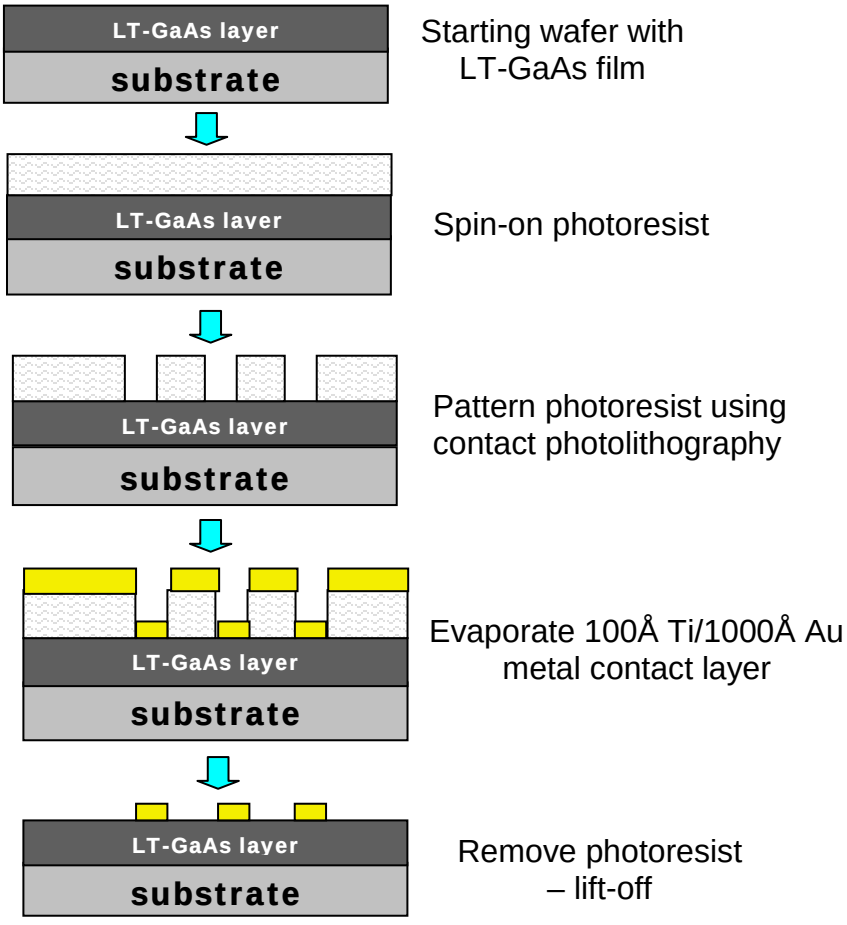

Figure 2.12 Schematics of the standard lift-off process flow to make MSM switches.

wafer with annealed LT-GaAs, we first spun on a photoresist layer and exposed it into an interdigitated pattern using contact photolithography. Then a 100 Å titanium film followed by 1000 Å gold layer were evaporated on top. The Ti layer was used to increase the Au adhesion to the GaAs film. The last step was the liftoff with solvent, leaving the Ti/Au interdigitated metal electrodes on top of LT-GaAs epi-layer with the desired pattern and size to form an MSM switch. Devices with different finger spacing and finger width (0.8, 1, 2 and 5 μm for spacing and width) were patterned in a ~ 20 μm × 20 μm area, as this is approximately the optical spot size used for characterization. For a 1 μm width switch, the calculated device capacitances for 0.8, 1, 2 and 5 μm finger spacing switches are 18, 16, 10 and 4 fF, respectively. Fig. 2.11 shows a picture of two such switches.

2.3.3 Basic device physics

Fig. 2.13 illustrates how a MSM switch works. A MSM photodetector typically utilizes an interdigitated pattern as shown in Fig. 2.13 (a). A MSM device is made by forming two Schottky barrier contacts back-to-back on the same semiconductor surface. The resulting structure is biased with some d.c. voltage during device operation (Fig. 2.13 (c)). Strictly, since the MSM diodes have a co-planar structure, the electrical field distribution within the device is two-dimensional. Numerical 2-D models are needed to accurately determine the device electric field. However, under many situations, the photo-generated carriers are confined to the surface region and a one-dimensional simplification is usually justified and is used to derive analytical solutions [37].

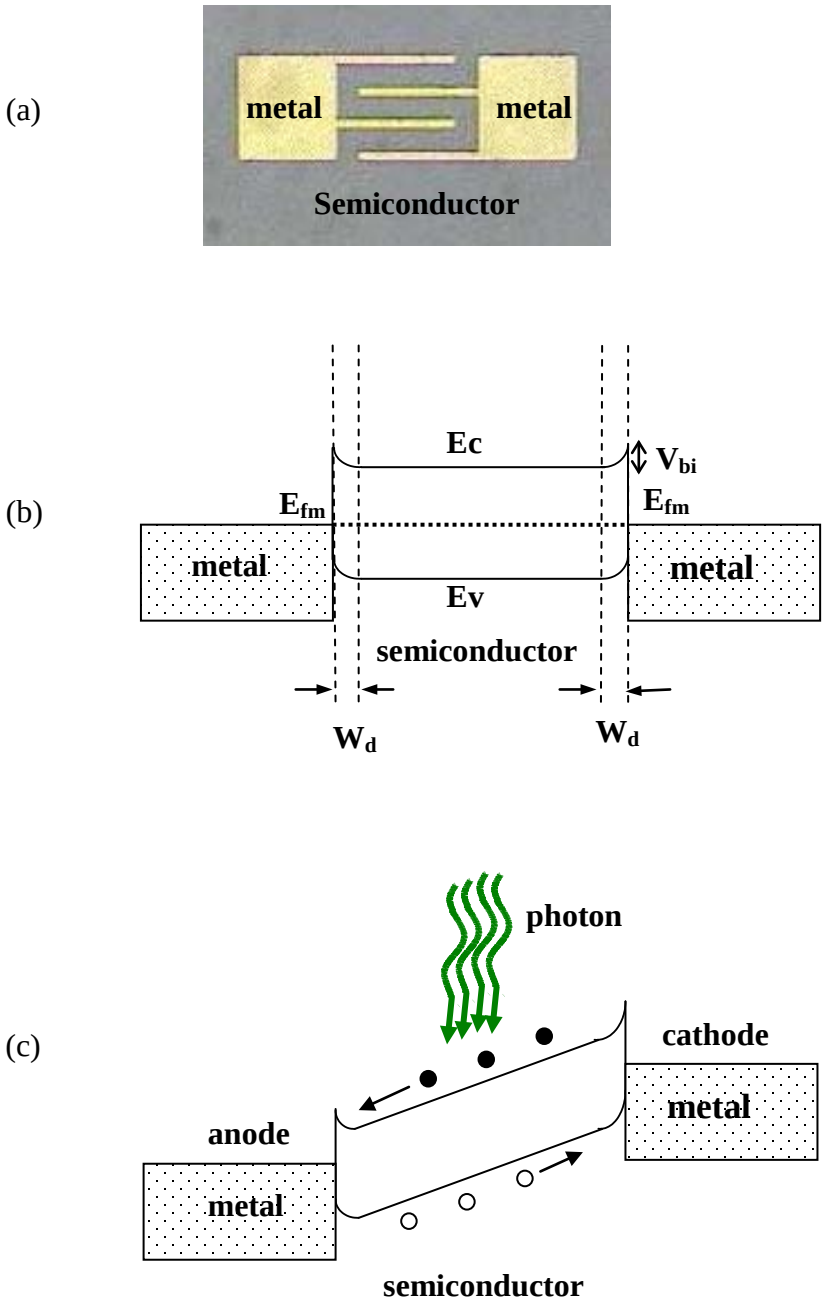

Figure 2.13 (a) Picture of a MSM switch made on the surface of a semiconductor film. (b) Band diagram of a LT-GaAs MSM device with no bias voltage applied. W_d is the width of the depletion regions, V_{bi} is the build-in voltage and E_{fm} is the metal Fermi level. (c) Band diagram of this switch when an external bias voltage is applied and when the device is under photo illumination. Electron and hole carriers are created by the incident photons and are swept to the metal contacts by the electric field.

Fig. 2.13 (b) is such a simplified 1-D band diagram for a LT-GaAs MSM switch when no bias voltage is applied and no light shines on the device. The two Schottky junctions are symmetrical under thermal equilibrium. As we have discussed, the LT-GaAs is semi-insulating in nature. Due to this fact and the high density of surface states, the metal Fermi level is usually pinned at approximately 2/3 of the band gap below the conduction band edge. This results in a small built-in voltage, V_{bi} for Schottky barrier junctions. The GaAs semiconductor thus consists of a space-charge neutral region and two contact space-charge regions (depletion regions). The depletion region width, W_d, is given by

$$W_d = \sqrt{\frac{2\varepsilon V_{bi}}{qN_{dd}}} \tag{2.6}$$

where N_{dd} in the case of LT-GaAs is the antisite (As_{Ga}) deep donor density which is very high as we have shown earlier. The large N_{dd} and small V_{bi} result in short depletion regions.

When an external bias is applied, one Schottky contact (anode) is forward biased and the other one (cathode) is reverse biased (Fig. 2.13 (c)). When electron and hole pairs are created by photo-illumination, the bias-created electrical field sweeps the photocarriers out toward the electrodes – holes drift toward the cathode and electrons toward the anode as illustrated in the illustration. Since the LT-GaAs depletion regions are short, most voltage drops across the bulk absorption region. Most carriers are generated within the light penetration depth, which is approximately the inverse of the light absorption coefficient ($1/\alpha$). Depending on the geometry and size of MSM device, and the characteristics of the semiconductor materials, the MSM detectors can function in either a carrier transit time limited regime or a carrier lifetime limited regime. This will become clearer in the following sections when we discuss the MSM photoconductive switch transient current responses.

2.3.4 Switch characterization by high-speed electro-optic sampling

In our ADC system, to obtain a large input bandwidth in the sample-and-hold scheme, an important benefit that prompted us to incorporate optics into the A/D conversion process, a fast impulse response in the sampling switch is necessary. Also, to charge up the hold capacitor as much as possible during the sampling process, the switch needs to have good responsivity. Here we define responsivity as the output photocurrent per unit incident optical power (Amp/Watt), or to be exact in our study, how much effective output charge is produced by each input triggering photon (Coulombs per Joule). Therefore, it is of paramount importance that the photoconductive switches respond to the ultra-short triggering laser pulses very quickly and with high responsivity.

2.3.4.1 Switch impulse response test structure

To characterize the switching response to a short laser pulse, we placed the switch in the middle of a coplanar waveguide (CPW) transmission line structure that has 50 ohm impedance. When mounting the photoconductors, the most frequently used method is to incorporate them as an integral component of a high-speed transmission line. Then the electrode capacitance and inductance are distributed in the transmission line, leaving only a small capacitance associated with the active region of the photoconductor to affect the speed of the response. Therefore this structure minimizes the parasitics [38]. The test structure is shown in Fig. 2.14. The switch size is approximately 20 μm by 20 μm. The switch, the signal lines and the ground lines were made with the same Ti/Au material through the same lift-off process shown earlier. During measurement, the switch is d.c.-biased through one side of the signal line and optically triggered by a short laser pulse. The laser source is the same one that we used when characterizing the LT-GaAs carrier lifetime, a Ti-Sapphire mode-locked laser with ~ 150 fs pulse width. The photo-generated electrical pulses propagate from

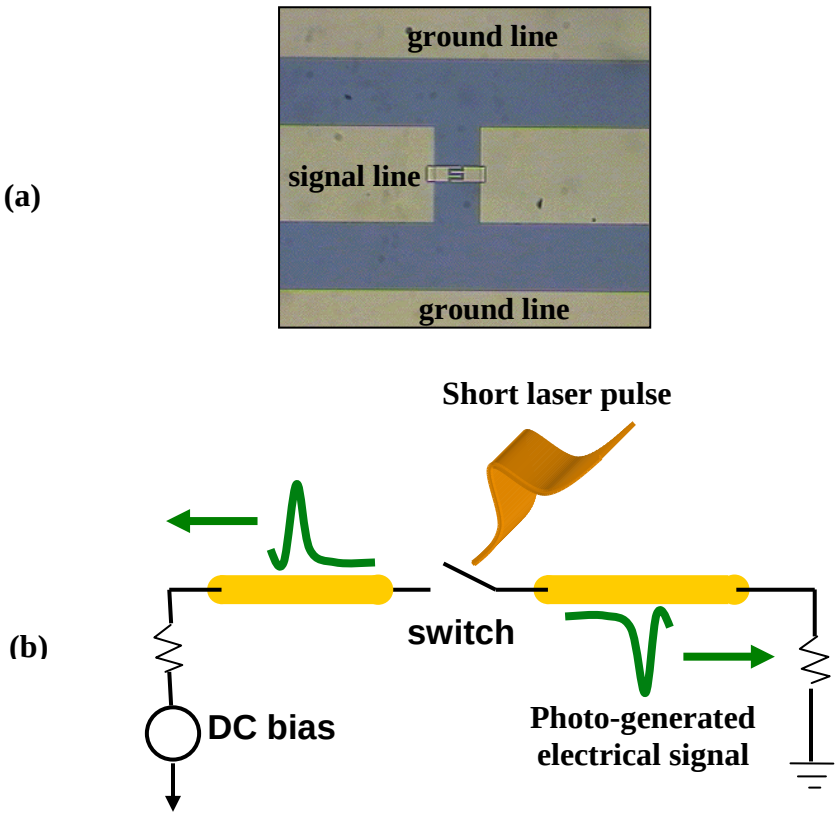

Figure 2.14 Illustration of a MSM photoconductive switch impulse response characterization. (a) Photograph of the test structure. The switch area is approximately 20 μm by 20 μm and it is placed in the middle of a coplanar waveguide transmission line structure. (b) Schematic illustration of the test process. The two golden color bars are signal lines. When a femotosecond laser pulse triggers the switch, photo-generated electrical pulses are created and propagate down the transmission lines under the d.c. bias. The switch speed and responsivity are characterized by measuring the electrical transients.

both sides of the MSM switch down the transmission line. By measuring these transients, the responsivity and speed of the switch are characterized.

2.3.4.2 High speed characterization by electro-optic sampling

Conventional testing instruments, such as sampling oscilloscopes (with state-of-the-art temporal resolution of better than 10 ps) are not fast enough to measure the (sub)picosecond transients generated by the LT-GaAs MSM switches. Luckily, due to

the demands for high-speed and high spatial resolution instrumentation required by the steadily increasing bandwidth of electronic and optoelectronic devices, and the capability of femto-second optical pulse generation, several novel high-speed characterization techniques have been developed, such as photoemissive sampling, photoconductive sampling, charge-sensing probing, photoelectron scanning electron microscope, and electro-optic sampling [39]. There are several comprehensive review papers discussing these subjects [39-45]. We chose an optical sampling technique called electro-optic sampling (EOS) to characterize the switch performance due to its superior temporal resolution, high linearity and accuracy, high voltage sensitivity, minimal invasiveness, and versatility.

2.3.4.2.1. Principle of electro-optic sampling

The electro-optic sampling technique was first reported by Valdmanis *et al* [42]. It was used to repetitively probe the electric field on a transmission line excited by a photoconductive detector with lithium niobate ($LiNbO_3$) as the electrooptic medium in his early research. Lithium tantalate ($LiTaO_3$) later proved to be superior to niobate to achieve subpicosecond temporal resolution with similar voltage sensitivity.

The underlying principle for the EOS technique is the Pockels effect, a linear electro-optic effect. This classical phenomenon was discovered by F. Pockels in 1906. He found that when applying an electric field to some crystals, the birefringence properties (indexes of refraction) of the nonlinear crystal are changed. Therefore, when light passes through the crystal, its polarization is changed. These acentric crystals are called electro-optic crystals. When placing such an EO crystal in a light beam propagating between crossed polarizers, the light intensity changes as a function of the electric field or the applied voltage. This is a light intensity modulation process and the crystal is the modulator. Fig. 2.15 depicts the basic principle of this technique. From review articles [36-42], it is clear that the electro-optic sampling systems have various configurations. Fig. 2.15 shows a photoconductive gap switch configuration, embedded in a coplanar strip transmission line structure. The EO crystal's intrinsic polarizability to an electric field has a temporal response in the femtosecond regime.

Combining mode-locked laser technology that produces ultrashort femtosecond optical pulses, electro-optic sampling has made it possible to achieve a temporal resolution less than 1 ps. An important advantage of the EOS is that the optical pulses sample the induced electric field without damaging or altering the circuits or devices under test, thereby providing a non-destructive technique.

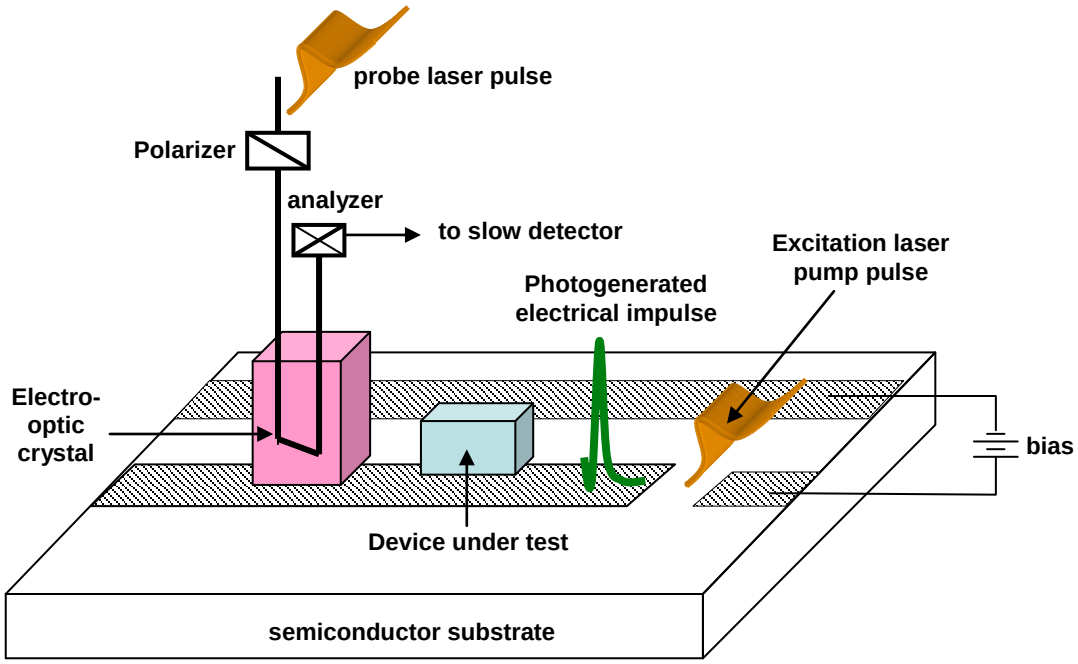

Figure 2.15 Illustration of the electro-optic sampling principle. Produced after [46].

2.3.4.2.2. Experimental setup

Fig. 2.16 shows the essence of the experimental setup of our electro-optic sampling system. A lithium tantalate electro-optic crystal is placed on top of the transmission line. We use Ti/Sapphire mode-locked laser pulse trains to repetitively trigger the MSM switch and create electrical pulses. This laser is the one we used when characterizing the LT-GaAs lifetime. It has approximately 150 fs full-width at half-maximum (FWHM) at around 80 MHz repetition rate. The center wavelength is ~ 850 nm. After leaving the laser source, the laser beam is split into a pump beam and a probe beam through a beam splitter. With d.c. bias applied to one end of the switch, the electrical signal created by the pump pulse propagates down the transmission line. The fringing electrical field causes voltage dependent birefringence in the $LiTaO_3$

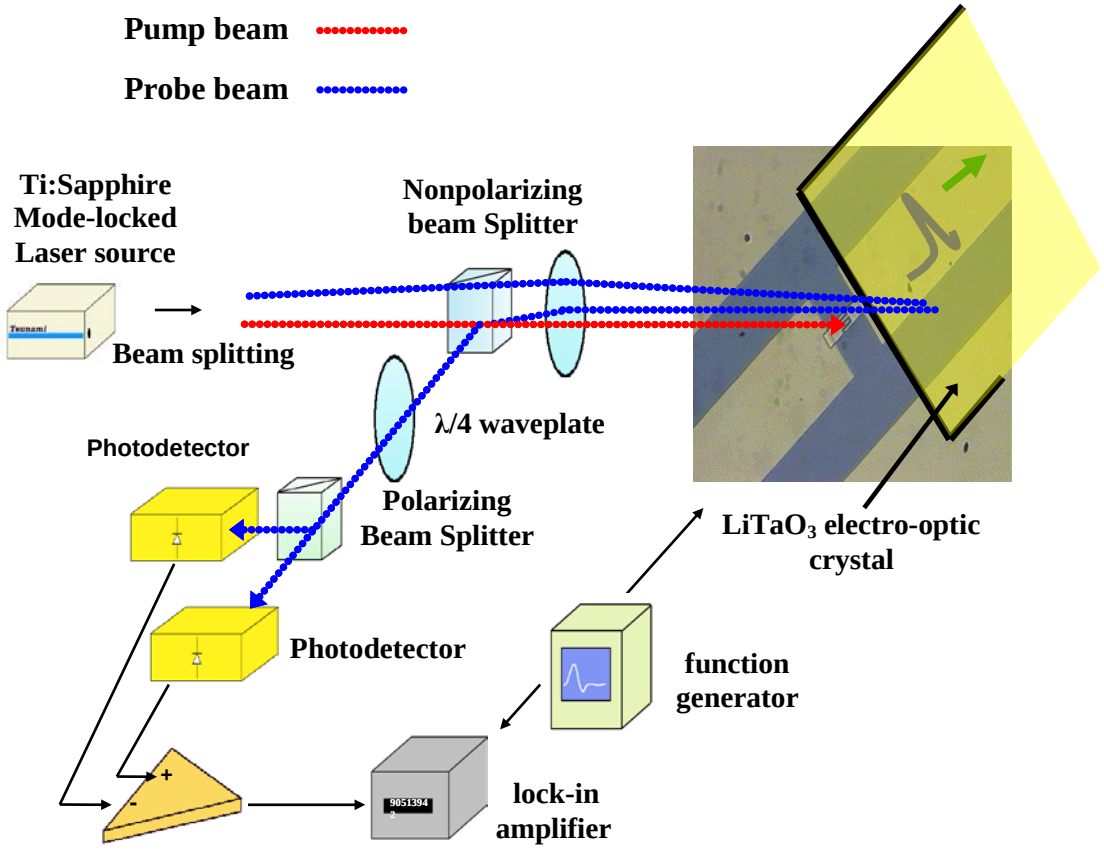

Figure 2.16 Schematics of the electro-optic sampling experimental setup. The yellow piece represents the transparent ~ 90 μm thick $LiTaO_3$ crystal that is AR/HR coated on top and bottom sides and placed on top of the transmission lines.

crystal, which can be detected by a probe pulse. The $LiTaO_3$ crystal has anti-reflection (AR) and high-reflection (HR) coating layers on the top and bottom sides to maximize the signal strength of the probe pulse that hits the crystal and completes a round-trip through it. Probing should be done as close to the MSM switch (where optical excitation happens) as possible (50 – 100 μm). The shortest propagation distance minimizes the extent of distortion of the electrical transients during propagation down the transmission line that results from a combination of modal dispersion, radiation, skin-effect conductor loss and substrate shunt loss [47]. The modulated probe beam is reflected back from the crystal and fed into the photodetectors. A quarter waveplate is added to the path to create more phase retardation in order to improve the detection sensitivity. A pair of conventional silicon photodetectors is used for differential detection in order to boost (double) the output signal amplitude and to cancel out the noise. The speed of the photodetectors does not need to be so fast to resolve each individual optical pulse. A lock-in amplifier (excellent signal-to-noise ratio) measures the amplitude of the modulated intensity and gives an output proportional to the sampled electrical signal amplitude. By using a translation stage to change the relative time delay between the pump and the probe pulses, the photo-excited electrical transient is characterized in the time domain.

2.3.4.2.3. LT-GaAs MSM switch response

1) Characteristic impulse response

Using the EO sampling technique, we characterized a series of MSM switches made from LT-GaAs films with various growth and anneal conditions, and with different MSM patterns.

Fig. 2.17 shows a raw response signal obtained from EO sampling. This is an output waveform of an MSM switch made on 0.6 μm thick LT-GaAs film grown at 250 °C with 20× As BEP and annealed at 700 °C for 1 min. This particular MSM switch has 1 μm finger width and 1 μm finger spacing. The amplitude and the width of the impulse represent the responsivity and speed of the switch. In general, many factors affect the final switch response, including LT-GaAs film growth and anneal conditions, film thickness, MSM pattern, excitation optical pulse intensity and external bias voltage etc. There is always a tradeoff between these two switch figures-of-merit. The typical cost for faster speed is loss of responsivity. This switch was illuminated by a ~ 12 pJ laser pump pulse and the measurement was done under 10 V bias voltage. The FWHM switching window is approximately 2.4 ps for this condition.

The final waveform is a convolution of intrinsic impulse response, device parasitics, and measurement system limitations. Regarding the MSM Schottky photodiode's impulse response to short optical pulses, theoretical calculations and simulations have been attempted by several research groups [48-52] to understand the

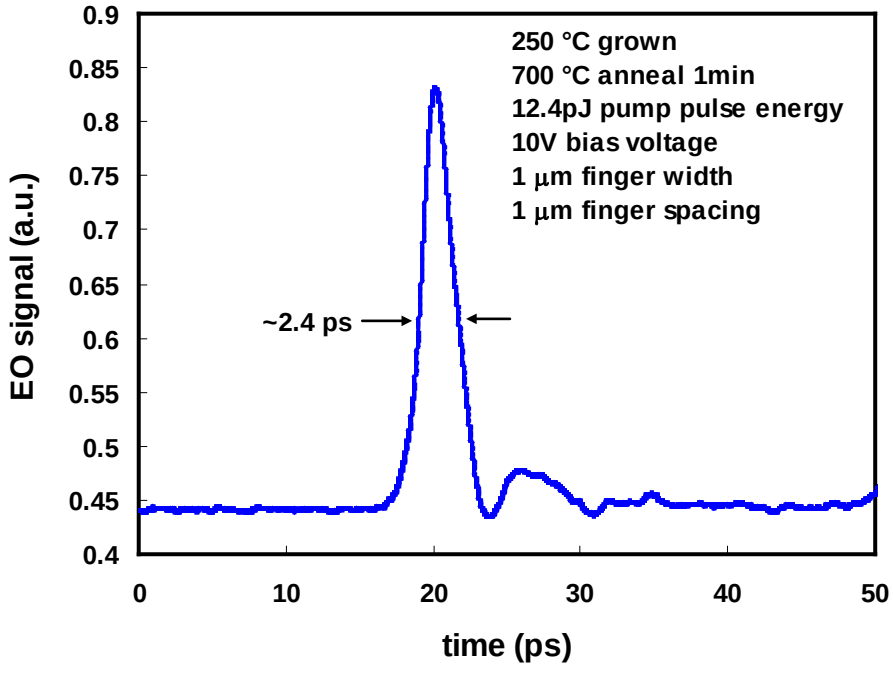

Figure 2.17 Electro-optic sampling tested temporal response at 10 V bias for an MSM switch with 1 μm finger width and 1 μm finger spacing, made from LT-GaAs grown at 250 °C and annealed at 700 °C for 1 minute. The FWHM switching window is ~ 2.4 ps.

experimental data. For theoretical treatments of the transport mechanisms of the photocarriers, the following basic governing equations should be applied.

Possion equation:

$$\nabla^2\psi = \frac{-q}{\varepsilon_s}(p - n + N_D^+ - N_A^- + n_t^-) \tag{2.7}$$

where Ψ is the electrostatic potential function, ε_s is the dielectric constant of the semiconductor material used for the MSM active layer, n and p are electron and hole carrier concentration, N_D^+ and N_A^- are the ionized donor and acceptor concentration, respectively, n_t is the electron-filled trap concentration and this item is especially customized for nonstoichiometric materials such as LT-GaAs.

Current density equation:

$$J_n = q\mu_n nE + qD_n\nabla n \tag{2.8}$$

$$J_p = q\mu_p pE - qD_p\nabla p \tag{2.9}$$

$$J_d = \varepsilon_s\frac{\partial E}{\partial t} \tag{2.10}$$

where μ_n and μ_p are the electron and hole mobilities, D_n and D_p are the electron and hole diffusivities, respectively. E is the electric field, J_n and J_p are conduction current contributed from electrons and holes, respectively, J_d is the displacement current, and ε_s is the dielectric constant of the semiconductor. Displacement current is usually not considered because typically either the variation of the electric field with time is slow or the electric field is constant. But when a detector (or switch) is illuminated with short laser pulses with high injection levels, the field could be suddenly screened by the photocarriers on a sub-picosecond time frame. This process could cause a displacement current component that cannot be neglected.

Continuity equation:

$$\frac{\partial n}{\partial t} = G_n - R_n + \frac{1}{q}\nabla \bullet J_n \tag{2.11}$$

$$\frac{\partial p}{\partial t} = G_p - R_p - \frac{1}{q}\nabla \bullet J_p \tag{2.12}$$

where $G_{n,p}$ and $R_{n,p}$ are the electron/hole generation and recombination rates, respectively, $J_{n,p}$ are electron/hole current densities.

For materials with a high concentration of traps, such as as-grown LT-GaAs, Schockley-Read-Hall events should also be considered, therefore,

$$\frac{dn_t}{dt} = (R_n - G_n)_{SRH} - (R_p - G_p)_{SRH} \qquad (2.13)$$

where n_t^- is the electron-filled trap concentration, and $G_{n,p}$ and $R_{n,p}$ are the electron/hole generation and recombination rates. In most situations, including the annealed LT-GaAs, the trap density is not high enough such that the effects of n_t^- can be neglected.

The electrical transient is a result of the conductivity increase caused by the photogenerated carriers as a result of illumination on the switch area, and their annihilation due to various carrier capturing mechanisms, including carrier trapping, recombination, and collection at the electrodes. Because the intrinsic photogeneration process happens in a quantum mechanical time frame, the measured pulse risetime is mainly limited by the excitation laser pulse width and the measurement system (in our case, the electro-optic sampling system) time response. This is a non-varying factor for the same laser and system setup. The falltime is determined by the intrinsic material properties, parasitics and test conditions. In Fig 2.17, the first dominating sharp peak is followed by a current tail. This is more obvious in Fig. 2.18, to be shown later. The immediate negative-going dip following the initial peak is usually attributed to the displacement current component [48, 49], parasitics [52] and electro-optic sampling effect due to the flatness of the probe [54]. It can be concealed by the second peak and the current tail under high illumination. The second small peak is not well accounted for or agreed upon from theoretical simulations. We understand it to be caused by subsequent carrier dynamics, such as carrier relaxation or reemission of captured carriers. There are also some small ripples or ringing features, which are mainly due to parasitic inductance and spurious reflections on the transmission line.

This result clearly shows that other than a small following shoulders, switches made from properly processed LT-GaAs exhibit a nearly ideal photocurrent response that completely turns off after the main transient in about 10 – 15 ps. Generally for

conventional high temperature grown GaAs and even for LT-GaAs films that were not optimally prepared, there is a long slow tail due to residual current. Figure 2.17 confirms that switches made from LT-GaAs with properly chosen conditions are able to eliminate the slow tail that deteriorates the -3dB frequency response and adds to the sampling noise level. This is a result of the moderate density of deep traps created by optimal growth and annealing.

2) Bias voltage dependence

Fig. 2.18 shows the time-domain responses of the same switch, illuminated by fixed energy (12.4 pJ) pump pulses, but under different bias voltages ranging from 0.5 V to 10 V, a range large enough for most practical situations. For clear comparison of

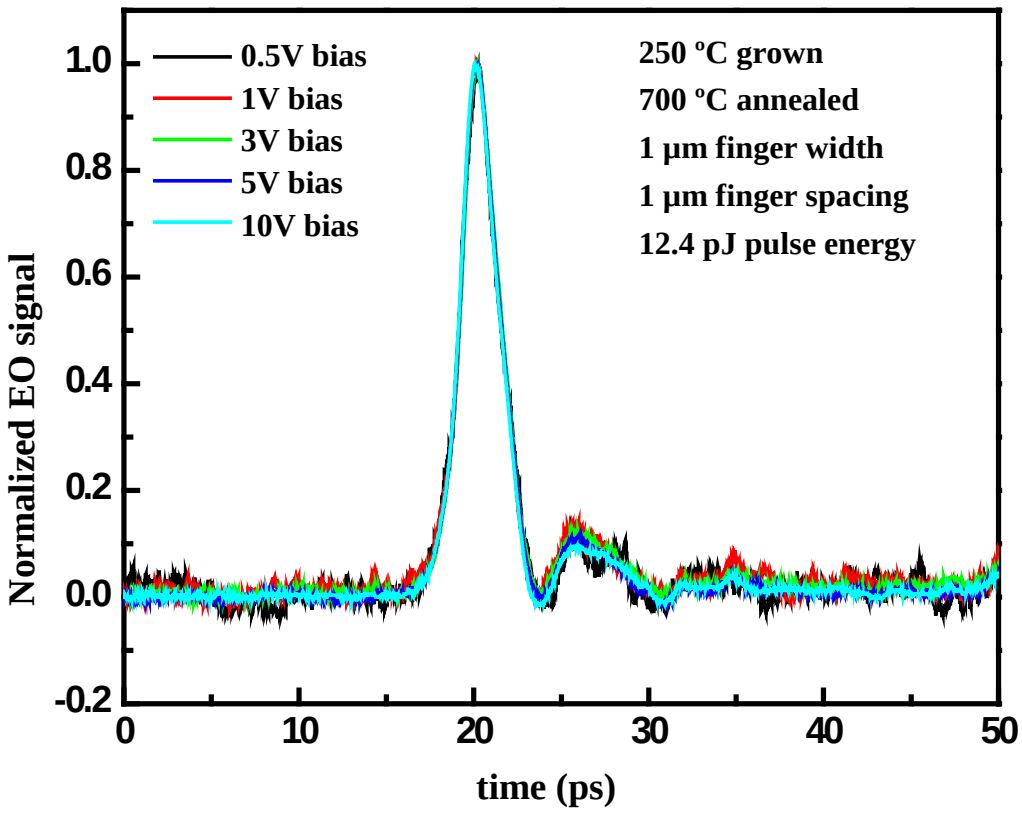

Figure 2.18 Normalized EO sampling signals for an MSM switch with 1 µm finger width and 1 µm finger spacing, made from LT-GaAs grown at 250 °C and annealed at 700 °C for 1 minute. Five amplitude-normalized transients obtained from measurements with the same illumination energy but different bias voltages are shown in this plot and they are almost completely overlapping, indicating bias-voltage independence of the switching response.

the transient shapes, the amplitudes of the signals were normalized to 1 and the five impulses were superimposed in the same plot. It is obvious that these curves almost exactly overlap with each other. This indicates there is virtually no dependence of the pulse shape on bias voltage. This result is consistent for the entire energy range for all the switches we tested. This attribute is very important for our ADC system. For the sample-and-hold scheme, if the switch response changes in the time domain as a function of the input voltage, it will lead to distortions in the output, breaking the linearity, adding to the aperture uncertainty, producing sampling inaccuracy.

It needs to be pointed out that this desired characteristic is not necessarily true for all MSM switches made with any materials and any pattern. Transit-time limited switches (many made with conventional high temperature, high crystal quality GaAs films) all exhibited large temporal response dependence (FWHM) on bias voltage [52, 53]. This is because the bias voltage affects the switching time response significantly because of the electric field dependence of carrier drift velocities when the carrier (mostly holes) transit time is the limiting factor. The measured switching response is a combination of various parameters, including: optical pulse width, photogenerated transient time, the electro-optic sampling time resolution, carrier transit time and recombination time, and circuit parasitics (switch capacitance, parasitic inductance, transmission line impedance etc). Among these factors, carrier transit time is the one heavily affected by the electric field. This result confirms that our switches are in the lifetime limited regime. LT-GaAs carrier trapping time is usually in a few hundred femtosecond to a few picosecond range, much shorter than the transit time between electrodes in typical lithographic geometries. The photocurrent will stop after the free carriers are trapped. The disadvantage of this carrier trapping is reduced responsivity because only a fraction of the carriers reach the electrodes.

Fig. 2.19 shows the photocurrent as a function of bias voltage for different illumination energy and for switches made with different MSM finger spacing. The measurement was done with an Agilent 4155C parameter analyzer. As the bias increases, the photocurrent increases almost linearly for all the cases. In our setup, pump pulse power of 1 mW, 5 mW, 10 mW and 20 mW corresponds to pulse energies of 12.4 pJ, 62 pJ, 124 pJ and 248 pJ, respectively. Decreasing finger spacing results in an increase in the electric field. Although the effective switch illumination area is smaller, the results show that the switch responsivity still increases. The electric field mainly determines the speed of carrier sweep out. Due to the short carrier trapping and recombination time, this speed is essential in determining how many carriers reach the electrode within the switching time (responsivity). For high quality GaAs material, the carrier drift velocity increases with smaller electric fields and saturates at an electric field of ~ 0.3 V/μm. In our LT-GaAs switches, due to the much smaller carrier mobility, and due to the fact that the internal filed is substantially dropped by the field-screening effect in our high illumination condition, the drift velocity linearity with electric field is maintained to 10 V/μm and higher. This directly leads to the linear increase of the photocurrent with the bias voltage.

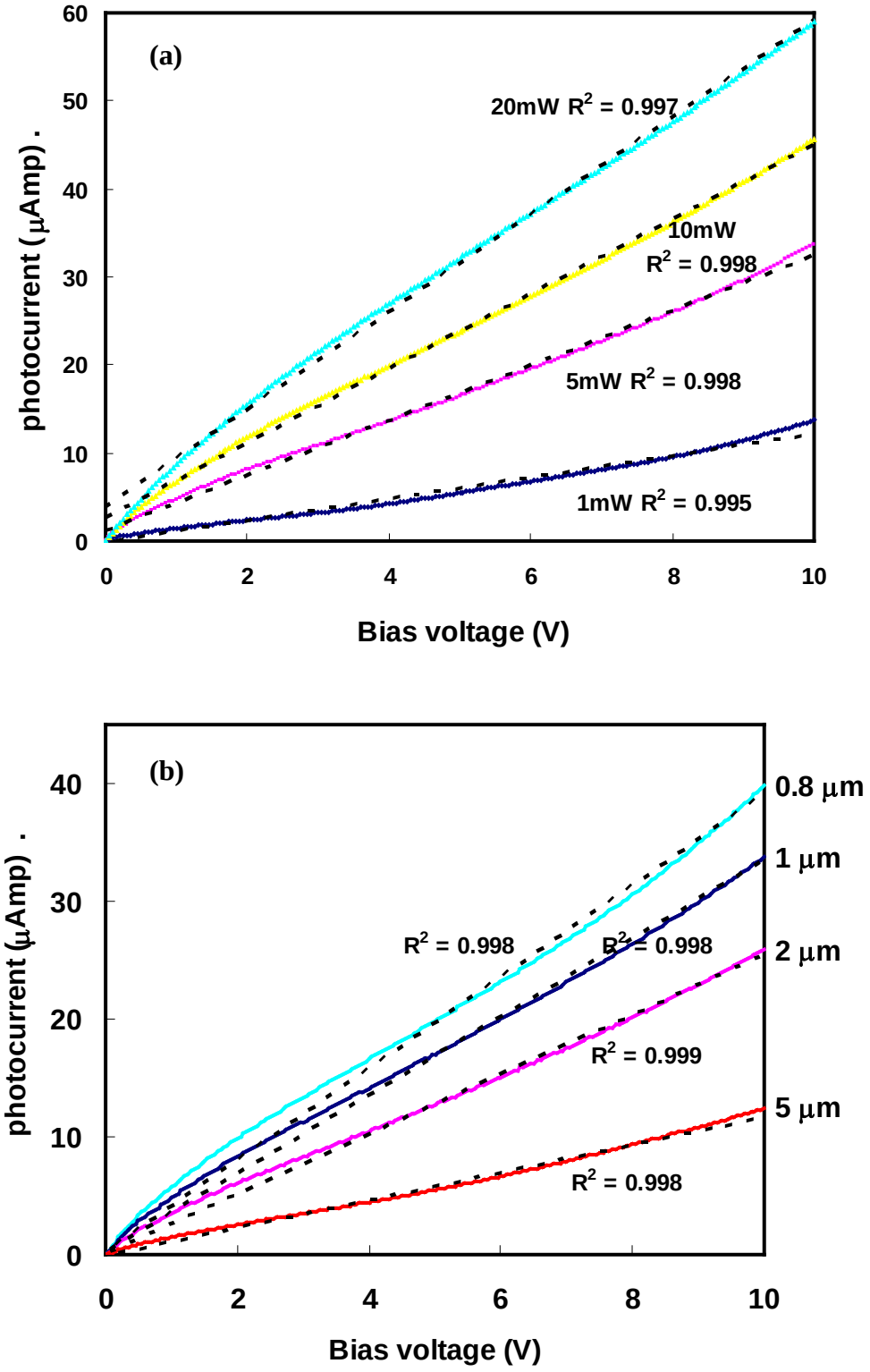

Figure 2.19 (a) Photocurrent as a function of bias voltage for different illumination powers. (b) Photocurrent as a function of bias voltage for different finger spacing. Dotted lines are linear fits for each curve. The R^2 values indicate that these IV curves are almost all linear to the large part.

3) Illumination optical energy dependence

Fig. 2.20 shows the normalized electro-optic sampling signals in time domain for different illumination levels under constant 1 V bias. This is the same switch tested above. Varying the optical pump pulse energy from 12 pJ to 250 pJ, the main peak stays almost the same. Only the relative level of the second small peak rises with excitation power. A satisfying trait is that the current tail still turns off in 10 – 15 ps following the main transient.

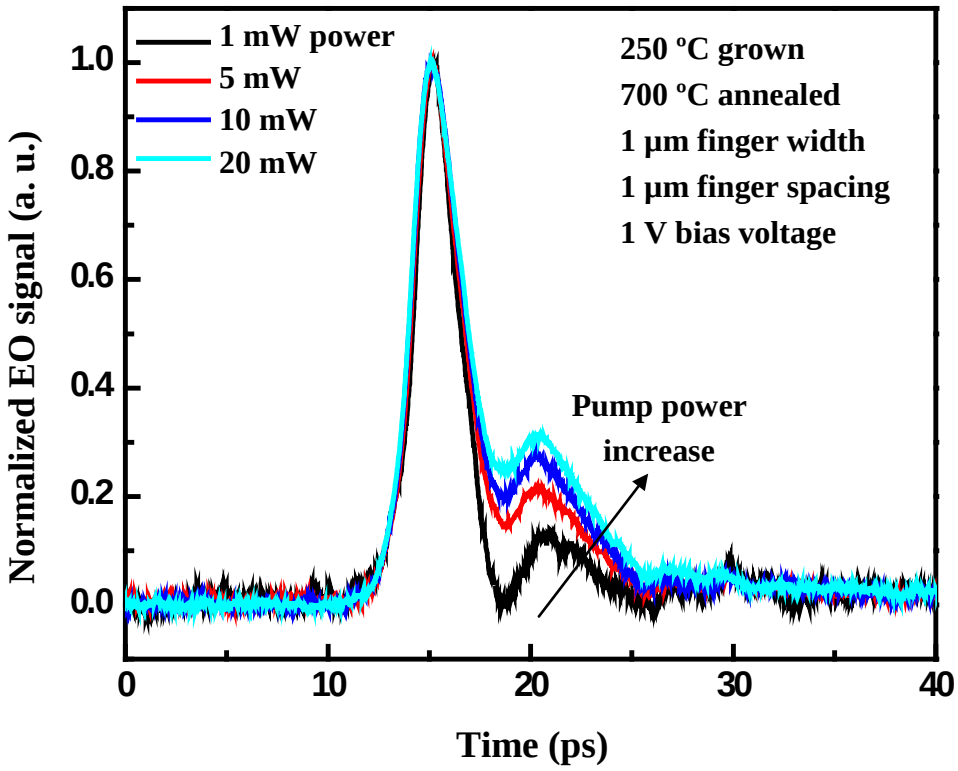

Figure 2.20 Normalized EOS signals for an MSM switch with 1 μm by 1 μm finger size, made from LT-GaAs grown at 250 °C and annealed at 700 °C. Four amplitude-normalized waveforms obtained from measurements with constant bias voltage but different illumination energy are shown superimposed in this plot. The relative intensity of the second peak to the main peak increases with the optical excitation energy.

Fig. 2.21 shows the photocurrent as a function of optical pump pulse power for different bias voltage and finger spacing, for the same switch. More carriers are generated with increasing pulse power at a certain bias or finger spacing, and

therefore, higher responsivity. In Fig. 2.21 (b), by decreasing the finger spacing, the illumination area is effectively reduced. But the responsivity still increases with smaller spacing due to the increased electric field. It is clear that the current saturates with pump pulse energy. Both bias voltage and finger spacing affect the internal electric field, and this saturation trend is seen across the whole voltage and spacing range we have tested. This phenomenon has been seen in previous work [50, 52, 53, 55]. Both this saturation with power and the shoulder increase with power seen in Fig. 2.20 are due to the same causes. One important reason is the space charge effect. The laser pulse energy we used is considered to be at a high illumination level. After the carriers are generated under illumination, the opposite-direction-going electrons and holes will induce a screening electric field to counter/screen the externally applied field. The field-screening effect caused by the photogeneration is more pronounced at high energy illumination as higher screening filed is built up by the lager number of photocarriers, which contributes to the photocurrent saturation behavior. Another possibility is that under high level illumination, there are more free carriers waiting for the traps to become available after the trap relaxation process (recombination of trapped electrons and holes). This leads to the shoulder growth with increasing optical energy. Also, since our LT-GaAs MSM switch works in the carrier lifetime limit regime, most photo-generated carriers are trapped and recombine before they are collected by the electrodes. The number of carriers generated near the surface and close to the electrodes, i.e., the current-contributing carriers, will eventually saturate as the optical pulse energy increases due to finite number of available states for light absorption.

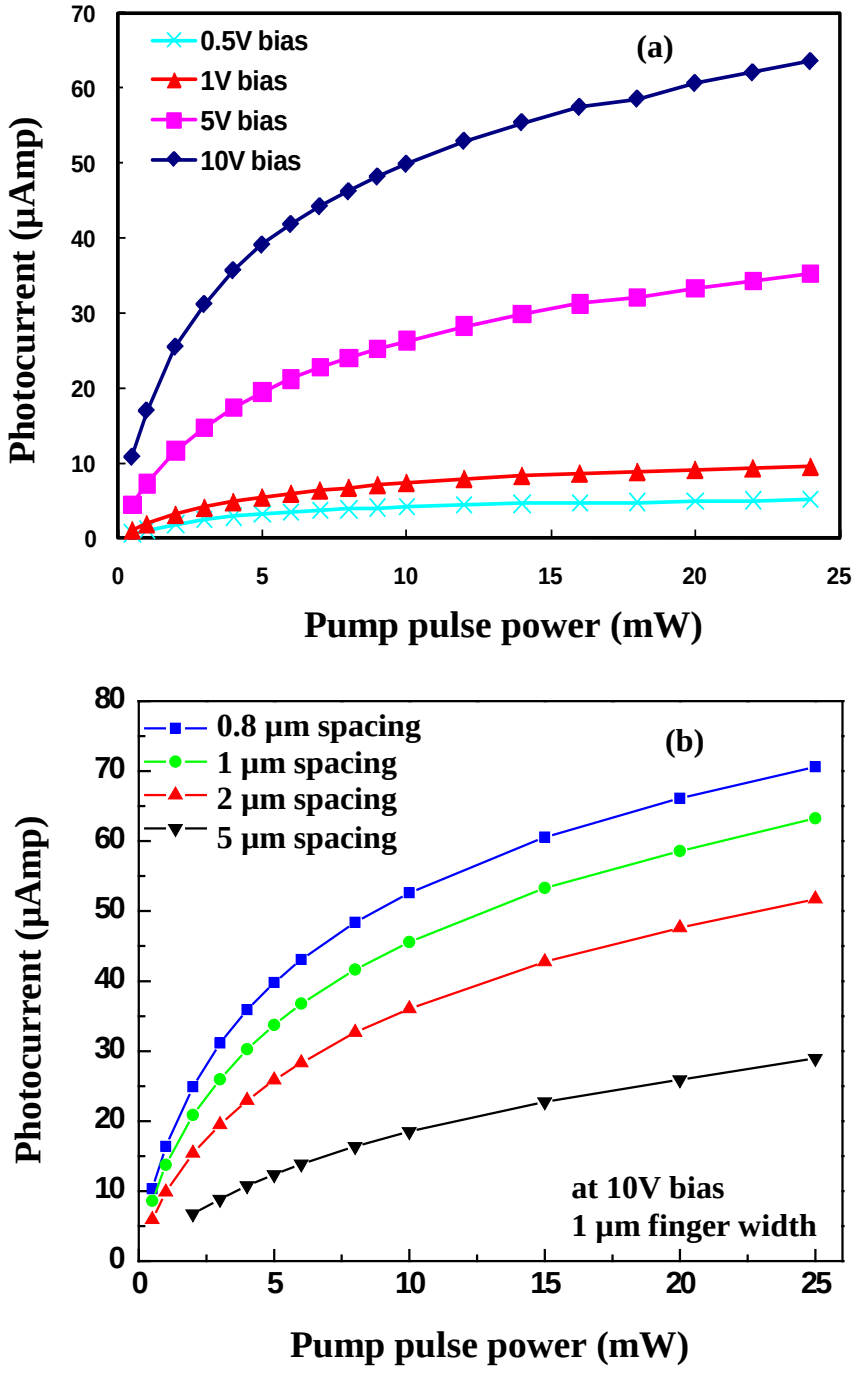

Figure 2.21 The MSM switch photocurrent as a function of pump pulse power for different bias voltages and finger spacings (LI curve). (a) Photocurrent as a function of optical power for different biases. (b) Photocurrent as a function of laser power for different finger spacings.

4) Dark current

Fig. 2.22 shows the dark current of two switches with different finger spacing. We can see that the dark currents are at a very low level, less than 1 nAmp or 0.1 nAmp at 10 V bias for 1 μm finger spacing and 5 μm spacing switch, respectively. The switch with smaller finger spacing exhibits a higher dark current than the device with larger spacing, due to the higher internal electric field. The calculated differential resistance (dV/dI) at 1 V is in tens of giga-ohms! This is a very important figure-of-merit for LT-GaAs material. The extremely high OFF-state resistance minimizes the held voltage fluctuation and the inter-channel coupling in our multi-channel ADC system with sample and hold structure.

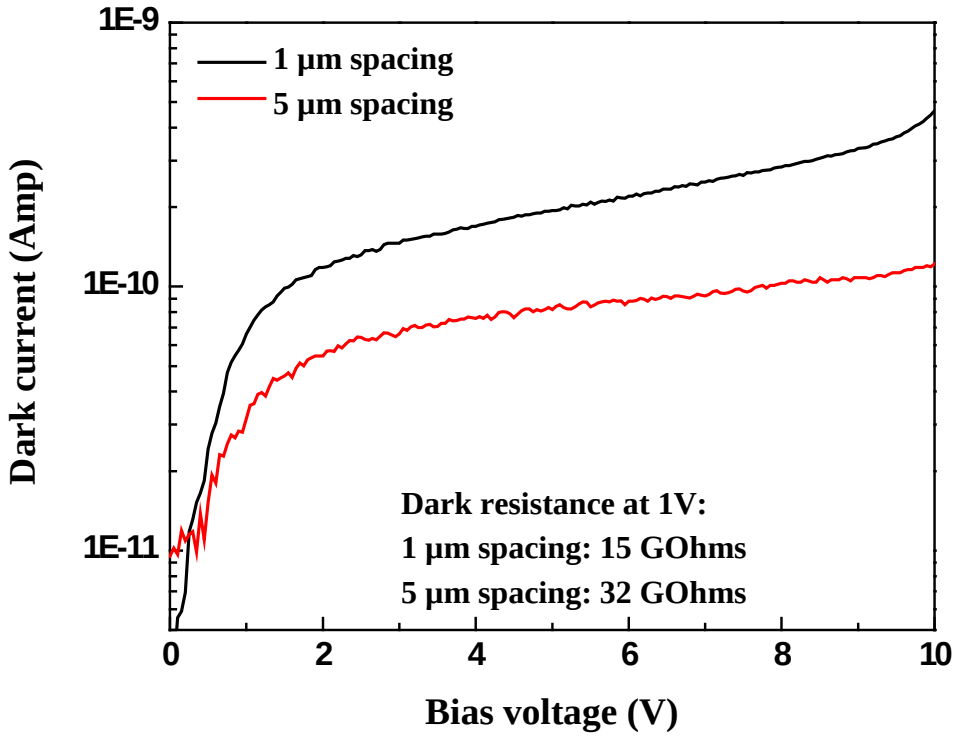

Figure 2.22 Dark current for two switches with 1 μm and 5 μm finger spacing.

2.4 LT-GaAs growth and anneal optimization

We have shown the characterization of the MSM switches and demonstrated that their switching properties are strongly dependent on the properties of the active semiconductor layer. However, it is not trivial to grow LT-GaAs films with such desired performance. The main reason is that the film properties are very sensitive to many conditions, for example, wafer growth temperature, As to Ga flux ratio (BEP), growth rate, post-growth anneal temperature and duration, film thickness, and so on. Varying each condition significantly affects the defect density and distribution, and affects the film critical thickness. To make it more challenging, we already know from previous introduction that in MBE it is very difficult to measure the real substrate temperature below 400 °C. So achieving good reproducibility is a difficult task. As mentioned earlier, we combined several different methods to carefully calibrate and measure substrate temperature.

On the other hand, the LT-GaAs film's sensitive response to growth and anneal conditions offers the opportunity to control the electrical and optical characteristics, thus engineer the speed and responsivity of photoconductive devices made from the LT-GaAs film. A large amount of research data had been published on investigations of the effects of process conditions on the LT-GaAs film properties. Some have even applied a stochastic model to theoretically study the growth mechanisms of LT-GaAs [56-58], i.e. the kinetics of excess As incorporation. Their model addresses the effects of temperature, flux ratio, and growth rate on the incorporation of As_{Ga}. It discusses the time evolution of the LT-epilayers through the change of the normalized macrovariables (such as layer coverage of atoms, inplane atom-vacancy pairs and inplane atom-atom pairs) in every layer due to surface processes, such as adsorption, evaporation, and surface migration. The dependence of antisite As concentration on growth rate is discussed. The critical As flux to reach lattice mismatch saturation is predicted. Their simulation result was referred as a guideline for choosing appropriate growth conditions as we want to control the properties of the LT-GaAs during the growth process.

Fig. 2.23 shows examples of prior research data that summarize the general trends on how process parameters affect the LT-GaAs properties. In general, at a constant As to Ga flux ratio (BEP, beam equivalent pressure ratio, measured by ion gauge), decreasing growth temperature rapidly increases the density of defects. At a constant growth temperature, increasing As supply increases the density of defects. Increasing the annealing temperature and duration promotes growth of precipitates and the precipitate density to drop, indicating an Ostwald ripening process. Also the film thickness needs to be controlled well in order not to exceed the critical thickness and cause extended crystal defects such as dislocations and stacking faults.

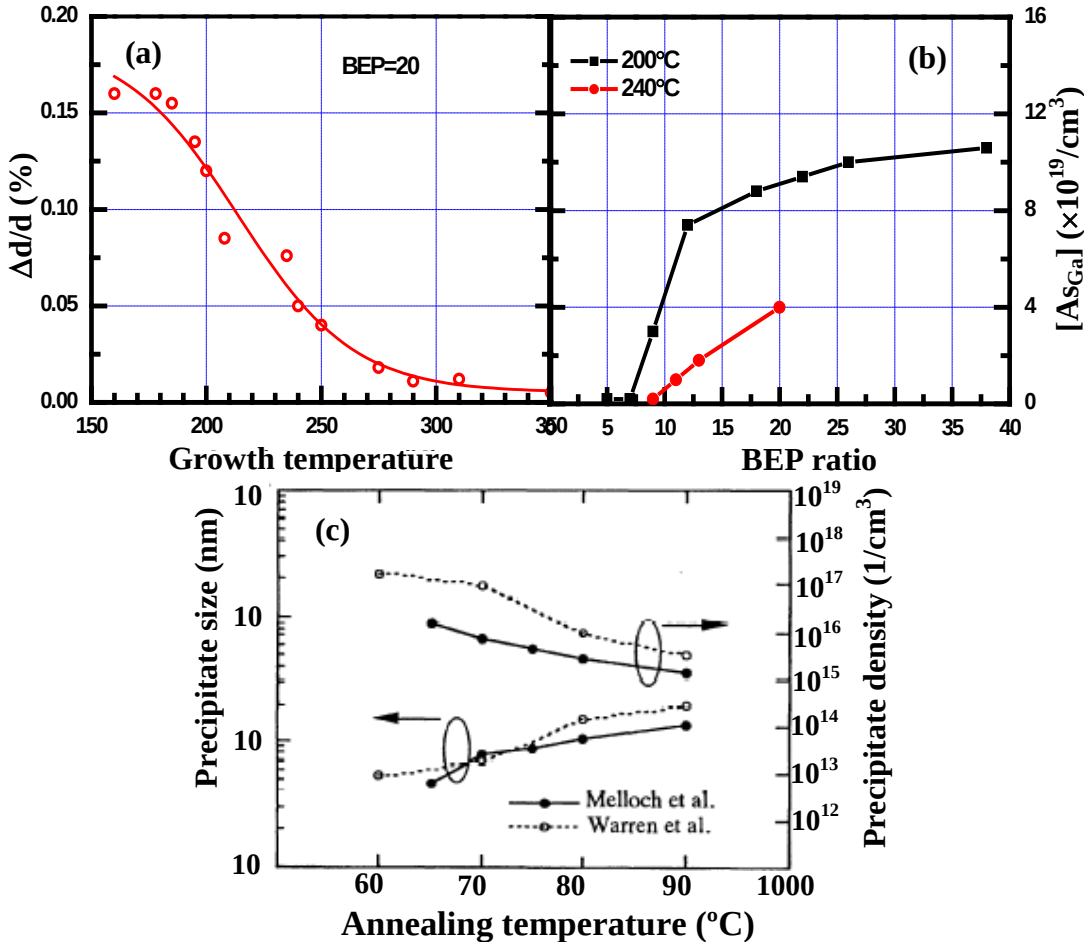

Figure 2.23 The dependence of LT-GaAs properties on process conditions such as growth temperature (a), BEP ratio (b) and annealing temperature (c). (a) and (b) are reproduced from ref [59] data. [As_{Ga}] concentration is calculated from eqn. 2.3 from lattice mismatch obtained by XRD. (c) is reproduced from ref [60], where data taken from [61, 62].

That said, increasing growth and anneal temperature and anneal duration will improve the carrier mobility, but increasing carrier lifetime too at the same time. The optimal material we need for the photoconductive switch application is desired to have the shortest possible carrier lifetime and highest possible mobility (therefore high responsivity). These two goals compete against one another when choosing process conditions. Therefore an optimization of the growth and anneal parameters is needed for good responsivity and speed. We mainly need to consider appropriate substrate growth temperatures, As to Ga BEP ratio, anneal temperature and time, and film thickness. With such a large number of factors to consider and possible interactions between them, experiments with trial-and-error search for the best process range and one-factor-at-a-time approach are not efficient. Especially given the fact that the general trends of LT-GaAs growth processes are well studied, using these methods is costly, time consuming, and not necessary.

Fortunately, there are effective statistical ways with the principle of Design of Experiments (DOE) that we can use to find the optimal combination of process conditions. These days, the use of DOE in industry has been increasing and become a norm in process development due to its cost benefits and quality and productivity improvement. There are several powerful commercial software suites available, such as JMP®. However, reports of DOE use in the academia are still rarely seen. Interested readers are encouraged to refer to any statistical books talking about DOE, or the simplest way is to skim through the JMP website to quickly get the idea [63].

Doing a full factorial design would be thorough but not affordable both in cost and time. Being reasonable in the number of experiments that we have to run, we decided to design fractional factorial experiments following a Taguchi orthogonal array $L_9 3^4$. Table 2.2 shows the experiment arrangement with the four factors and three levels. We decided to investigate four main factors (growth temperature T_g, BEP, anneal temperature T_{anneal}, and anneal time t) at three different levels (low, medium, high). Combining the initial rough tests and the DOE runs, the process window we explored are following: T_g = (190 °C – 400 °C), BEP = (10× - 30×), T_{anneal} = (500 °C – 800 °C) and anneal time t = (30 sec – 10 mins), film thickness = (0.3 μm – 3 μm). The

final optimized condition is to grow 0.6 μm thick LT-GaAs film at 250 °C with As to Ga BEP ratio of 20 times, followed by RTA annealing at 700 °C for 1 min. All the experimental data we showed in the previous MSM switch characterization section were obtained from switches made with such optimized LT-GaAs films. The material quality is significantly improved compared to the LT-GaAs at the beginning of this study and the optimized material is successfully utilized in the prototype A/D system to be shown below.

Table 2.2 Taguchi L9 array of the growth and annnel conditions

Run	T(grow)	BEP	T(anneal)	t(anneal)	pattern
#1	1	1	1	1	----
#2	1	2	2	2	-000
#3	1	3	3	3	-+++
#4	2	1	2	3	0-0-
#5	2	2	3	1	00+-
#6	2	3	1	2	0+-0
#7	3	1	3	2	+-+0
#8	3	2	1	3	+0-+
#9	3	3	2	1	++0-

2.5 Hybrid integration and prototype system

In our A/D conversion system, the photoconductive sampling switches need to be connected to the input Si CMOS ADC circuits that perform the digitization function. Due to the limited responsivity of the LT-GaAs switches, the input capacitance has to be minimized in order to obtain high enough signals for the sample-and-hold circuit. We utilized a hybrid integration method when developing the prototype two-channel system. In the following chapters, monolithic approaches will be discussed. In hybrid methods, a flip-chip bonding technique is a practical integration means that can minimize the input load by minimizing the parasitics with the compact connection of the GaAs-based optoelectronic chip with the silicon integrated circuit. The process was first developed by Miller *et al* at Bell Labs [64]. Fig. 2.24 illustrates the flip-chip bonding process flow.

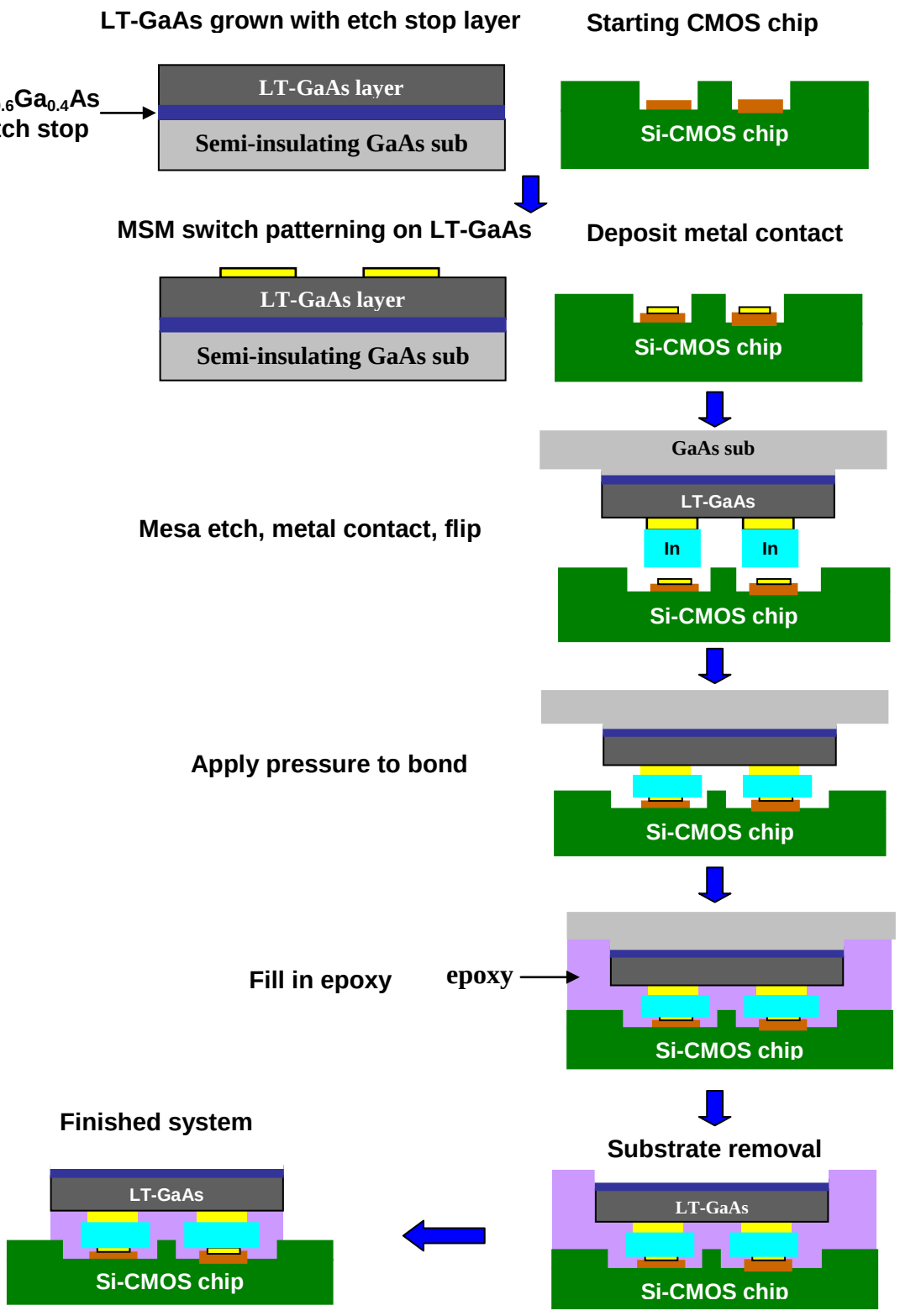

Figure 2.24 Illustration of flip-chip bonding process flow.

The CMOS A/D converter chip was designed by Nathawad [65] and fabricated by National Semiconductor Inc. with its 0.24 μm CMOS technology. The bonding was done with a Research Devices M8 flip-chip bonder. Indium was deposited on top of the MSM switches as solder material. The details of the process can be found in ref. [66]. It should be noted that the flip-chip bonded switches are backside illuminated, which increases the switch responsivity compared to the front-side illuminated switches characterized previously. Improved switch responsivity allows the hold capacitor to fully charge up during the sampling process.

We used a differential configuration for the sample-and-hold to eliminate the feedthrough error. The prototype two-channel A/D conversion system was made by bonding two pairs of LT-GaAs MSM switches with a CMOS chip with two A/D converters. Fig. 2.25 is the picture of the finished chip with two pairs of flip-chip bonded MSM switches. Since the MSM switches were flipped, they are below the gray AlGaAs etch stop layer and are not directly observed in this photo. The Ground-Signal-Ground pads connect to the coplanar waveguide (CPW) transmission line connecting to the switches, and allow the input signal to propagate to the sampling switches.

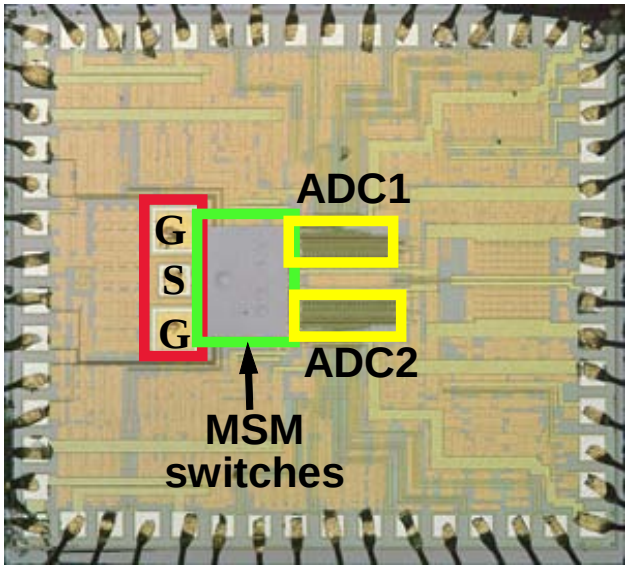

Figure 2.25 Micrograph of the two-channel prototype A/D conversion system with two pairs of MSM switches flip-chip bonded to the Si CMOS chip with two A/D converters. GSG represents ground-signal-ground pads.

This finished system is the first hybrid photonic-CMOS A/D conversion system to our knowledge. It combines the photoconductive sampling and time-interleaving to achieve a high input bandwidth. The prototype has two time-interleved channels, exhibits an effective number of bit resolution of ~ 3.5 bits and an input bandwidth greater than 40 GHz. An important feature is that the aperture uncertainty is smaller than 80 fs, which will allow a higher sampling rate with more channels in future designs. Details about our A/D conversion system can be found in Nathawad and Urata's theses [65, 66]. This work demonstrated that photoconductive switches made from LT-GaAs offer high speed sampling capability. In addition, the prototype system shows that full charge up of the hold capacitor occurs at a pump pulse energy as low as 50 pJ. Before the LT-GaAs optimization, it only charged to ~ 70% charge with over 300 pJ pump energy [66]. This is due to the large improvement in the material growth and anneal process of the LT-GaAs.

2.6 Summary

We chose LT-GaAs as the active photoconductive material to make MSM switches used as the sampling gates in a hybrid photonic/CMOS A/D conversion system. The films were grown by MBE on semi-insulating GaAs substrates at low temperatures, around 250 °C. The film was characterized by measuring the speed and responsivity of the MSM switches made from it. An optimization process was done on the film growth and annealing conditions in order to obtain the optimal trade-off between switch speed and responsivity. Switches made with the optimized LT-GaAs were electrically connected to the digitization silicon CMOS A/D converters with a flip-chip bonding technique to make a two-channel time-interleaved A/D conversion system. The prototype system has an input bandwidth over 40 GHz and an ENOB resolution of ~ 3.5 bits. The aperture uncertainty is less than 80 fs. This is the first hybrid photonic-CMOS A/D conversion system.

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Chapter 3

LT-GaAs Grown on Si Substrates

This chapter describes an investigation of growth of GaAs directly on Si substrates at low temperatures (~ 250 °C). The wafer cleaning and film growth temperatures are chosen to be safe for finished CMOS circuits. Material characterizations indicate good film quality. Time-resolved electro-optic sampling characterization shows that the performance of LT-GaAs MSM switches on a Si substrate are comparable to their homoepitaxy counterparts which were used in our prototype ADC with demonstrated outstanding performance. The successful low-temperature growth of GaAs on Si substrates promises the possibility of monolithic integration of ultra-fast LT-GaAs switches with completely fabricated Si CMOS circuits.

3.1 Background

3.1.1 Motivation

In the last chapter, we showed that a photonic-CMOS A/D conversion system could be built by integrating LT-GaAs photoconductive switches with silicon CMOS

A/D converters using a hybrid flip-chip bonding technique. But monolithic integration is preferred. It removes the necessity of etching, and wasting, the expensive GaAs substrate after bonding. It also allows for a more compact system with lower power consumption. More importantly, it further minimizes the circuit parasitics and the input capacitance. With the limited responsivity of LT-GaAs switches due to the defective nature of the active film, this is especially valuable.

Using co-integration to complement the maturity and density of Si technology with the high speed advantages and optical links of GaAs technology has been very attractive. Previous GaAs-on-Si studies mostly focused on achieving high crystalline quality GaAs films heteroepitaxially grown on Si for applications such as HBTs, MESFETs, lasers and LEDs that require long carrier life times and minimal recombination effects. High temperatures in both surface cleaning and film growth are usually necessary in order to minimize crystal defects. Therefore, the commonly adopted approach for monolithic integration is to finish the metallization layers of the Si-circuits after the growth of GaAs (or other compound semiconductor) devices on Si substrates. This is because the Si surface cleaning and GaAs film growth temperatures are usually higher than the melting or softening temperatures of Si-IC metal contacts. However, this kind of procedure creates significant process complications and fabrication perturbation due to the mismatch between different facilities/equipment used for fabricating Si circuits and GaAs devices, and due to potential cross-contamination issues, etc.

High-speed applications, such as our ultra-fast photoconductive switches, require some controllable density of crystal defects to shorten the carrier lifetimes. The material quality requirements are far more forgiving and the low growth temperature is compatible with completely fabricated CMOS circuits. Low temperature treatments also promise not to alter the doping profile in the underlying Si ICs and greatly reduce the thermal stress caused by the 60% difference in the thermal expansion coefficients between GaAs and Si. Therefore, we investigated the direct growth of GaAs on completely finished Si CMOS chips at low temperatures. This approach has much

broader applicability to CMOS optoelectronic interconnects beyond the scope of this thesis.

In this chapter, we started this study from LT-GaAs growth on a Si surface. Since the GaAs film is grown at temperatures below 300 °C, the critical step is cleaning the Si wafer surface at temperatures low enough not to damage the metal interconnects and other components in the underlying Si circuits.

3.1.2 Challenges of growing GaAs on Si

Good crystal quality GaAs on Si growth has been extremely difficult due to several fundamental problems.

First is the most obvious concern for heteroepitaxy. The GaAs lattice constant at 300 K is 5.65 Å, while the Si lattice constant at 300 K is 5.43 Å. There is a ~ 4% lattice mismatch between GaAs and Si, which leads to a high misfit dislocation density in the interface that can reach the active epilayer and cause other crystal defects. These dislocations are usually viewed as deep level traps and are detrimental to the performance of most devices.

There are typically two useful approaches to improve the GaAs epilayer quality, targeting either dislocation density reduction or hindering their propagation/threading into the active layer. One is to grow various types of buffer layers with various thicknesses before the active epi-layer growth, including either strained layers or strained-layer supperlattices (SLSs) that bend and anchor dislocations to be parallel to the interface. The second approach is to use post-growth thermal treatments, such as rapid thermal annealing and thermal cycling, to reduce dislocation density by allowing the dislocations to move, redistribute and react with the assistance of added thermal energy. [1]

The second problem is due to the growth of a polar compound semiconductor, GaAs film, on the non-polar Si substrates. Si has a diamond cubic lattice structure, where the two interpenetrating FCC (face-centered-cubic) sub-lattices are exactly the same, with both sub-lattices occupied by the same atom. Si is thus called a non-polar

semiconductor. While GaAs has a zincblende lattice structure where the two FCC sub-lattices are not equivalent, one composed of Ga atoms and the second, As atoms. Therefore GaAs is called a polar semiconductor. Growth of polar material on a non-polar material can potentially lead to a kind of structure defect called antiphase domains (APDs). APDs are areas where atoms reside in incorrect sub-lattice positions. In the case of GaAs, the boundaries of APDs (called antiphase boundaries, APBs) consist of As-As and Ga-Ga bonds.

Fig. 3.1 illustrates two conditions under which an antiphase boundary can be formed [2]. In case (a), assuming the Si substrate is perfectly flat with no atomic steps on the surface, when the GaAs growth is started with simultaneous exposure of the Si surface to both Ga and As fluxes, it is almost certain that the initial monolayer is covered by both Ga and As atoms and form Ga layers in some areas and As layers in other areas. This is because the Si lattice sites are all the same to the arriving atoms and therefore provide no preferential nucleation sites for Ga versus As atoms. After this first monolayer, the subsequent Ga and As atoms have their clearly preferred sites in which to bond. As shown in the cartoon (a), this will lead to Ga-Ga and As-As bonds in the epi film. In situation (b), although the initial monolayer is uniformly covered by the same atoms, either Ga or As, there are single atomic layer height steps on the Si surface (or any odd number steps). It shows that APBs can still be formed. This is because the GaAs (100) plane alternates between Ga and As planes. The existence of odd number Si steps perturbs this periodicity. It needs to be pointed out that the APB formation requires high energy and is not usually favored by the growth kinetics [2]. It is thus not a surprise to have APD-free growth when the above conditions are met.

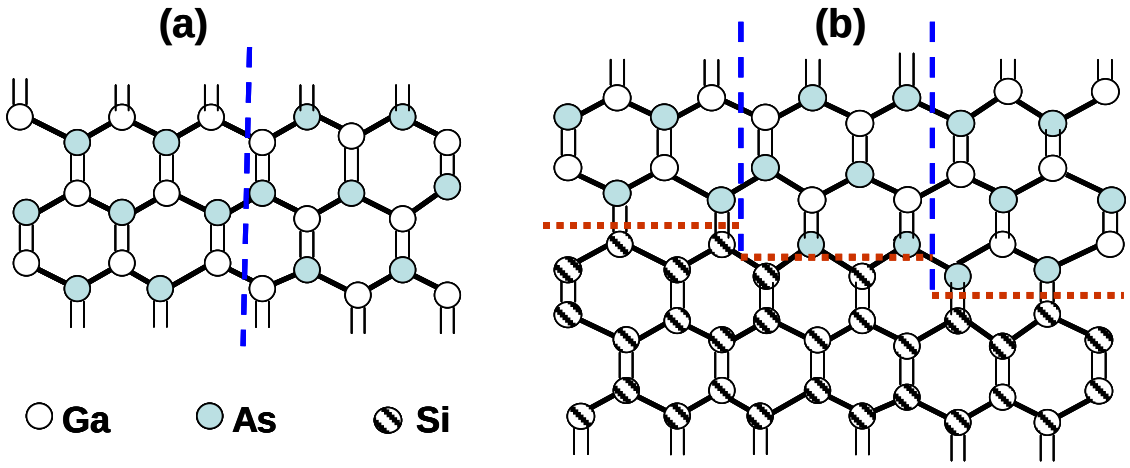

Figure 3.1 Illustration of two situations that an antiphase boundary (APB) is formed. (a) APB formation on an ideal, no step silicon surface due to a non-uniform coverage of initial Ga or As monolayer. (b) Even when the initial monolayer is uniformly covered by the same atom, APBs can still be formed when there are single atomic layer high steps on Si surface. The thick dashed lines show the Ga-Ga and As-As bonds forming the APBs. The dotted line separates the Si substrate and the GaAs film. (reproduced after ref [2])

APBs can be highly charged defects. Ga-Ga bonds have an electron deficiency and As-As bonds have excess electrons. These bonds are generally created in equal densities. They act as acceptors and donors and the epilayer is compensated. Therefore they are usually harmful to device performance.

Corresponding to the two situations analyzed above, there are two mostly used techniques to suppress antiphase domain formation. One is to ensure a uniform initial coverage of the Si surface with only one type of atom, either Ga or As, by only exposing the surface to one type of flux. Both Ga pre-layers and As pre-layers were extensively studied [3-7]. Although it was claimed that both types of pre-layers work equally well [2], As pre-layers have still been more widely used. A distinguished advantage of the As pre-layer is that there is always some residual background As pressure in the MBE system and second, the As-terminated Si surface is highly un-reactive. After the initial As layer is formed on Si, any additional As atoms can only stick to Ga atoms. This is beneficial for obtaining a smooth interface and a 2D growth mode. The other often used technique to eliminate antiphase domains is using Si substrates misoriented from the [001] axis by a few degrees (4º in our practice). The use of tilted substrates is to ensure that double (or an even number) atomic layer height

steps occur on the Si surface. It has been shown that double steps occur preferentially in tiled orientations [8]. Substrate tilt can help to reduce the dislocation density as well [8]. The largely accepted explanation to account for APD suppression with vicinal substrates is the creation of double-height steps [9]. After observation of APD-free GaAs-on-Si growth with standard cleaning processes that actually resulted in many-atomic-layer high steps (instead of all double steps) [10, 11], a self-annihilation model is proposed for their reduction [1, 12].

The third problem is due to thermal expansion coefficient mismatch between GaAs and Si. The bulk thermal expansion coefficient is 6.0×10^{-6} /K for GaAs and 2.3×10^{-6} /K for Si. The 60% difference leads to large stresses in the epilayer and limits the epilayer thickness before cracks are generated (critical thickness). Greater critical thickness is desirable because it has been agreed that growing thicker GaAs layers improves the material quality by offering more room for the dislocations to annihilate with each other. Depending on the relative thicknesses, sometimes the stress can also cause substrate bowing, bending and warpage. This complicates lithography and raises reliability concerns for GaAs/Si devices. In addition, the strain consists of a uniaxial component and a hydrostatic component. These two components cause valence band splitting, remove valence band degeneracy and therefore affect the GaAs epilayer optical properties [2].

Based on the above analysis, it has been extremely difficult to grow GaAs films on Si substrates with equivalent device performance characteristics to homoepitaxial GaAs films on GaAs substrates. However, in our specific application, we can tolerate a significantly higher concentration of defects to achieve short carrier lifetime, as long as the responsivity is not considerably sacrificed due to excessive recombination. Growth parameter optimization is the key. Therefore, we can compromise the material quality to a certain degree by lowering the surface cleaning and film growth temperatures in order to meet the general Si technology trend toward low-temperature processing. Another big benefit is that, since we grow the epilayer at low temperatures, the thermal stress caused by the thermal expansion coefficient

mismatch is greatly reduced compared to high temperature processes. Therefore, the third set of problems described above are non-existent.

3.1.3 Migration Enhanced Epitaxy (MEE)

In this work, we used a special growth technique at the beginning of the GaAs film growth to initiate a two dimensionally smooth layered growth mode, prevent island growth, and to provide a uniform prelayer with only one type of atom in order to suppress APDs. This technique is called Migration Enhanced Epitaxy (MEE). It was first demonstrated by Horikoshi *et al* when studying low temperature growth of GaAs and AlAs-GaAs quantum well structures [13] and was carefully reviewed in 1993 [14].

In typical MBE growth, the group III and V element fluxes are allowed to co-deposit onto the substrate by keeping both shutters open. The special thing in MEE growth is that the two types of beams are supplied alternatively by alternating the shutters. Take GaAs growth as an example: the As shutter is first opened to deposit a layer of arsenic, then it is closed and the Ga shutter is opened to supply Ga. This process is repeated until the desired thickness is reached. Figure 3.2 shows the difference between traditional MBE and MEE growth.

This technique is usually used when growing at low temperatures. By shutting off the group V supply during the group III supplying period, the group III atoms, such as Ga and Al can migrate over a much longer distance on the surface due to the As-free environment. Therefore these atoms have more opportunities to find energy-preferable sites, such as kinks and steps on the surface. The result is a layer-by-layer growth mode and smoother interfaces. Two major factors determine the Ga atom mobility. It is proportional to substrate surface temperature and inversely proportional to the density of excess As atoms present on the surface. At higher temperatures, Ga atoms have long enough surface diffusion length to grow a flat surface, even by conventional MBE. Therefore the benefit of using MEE is not pronounced at high substrate temperatures (> 550 °C). It is even considered harmful sometimes because

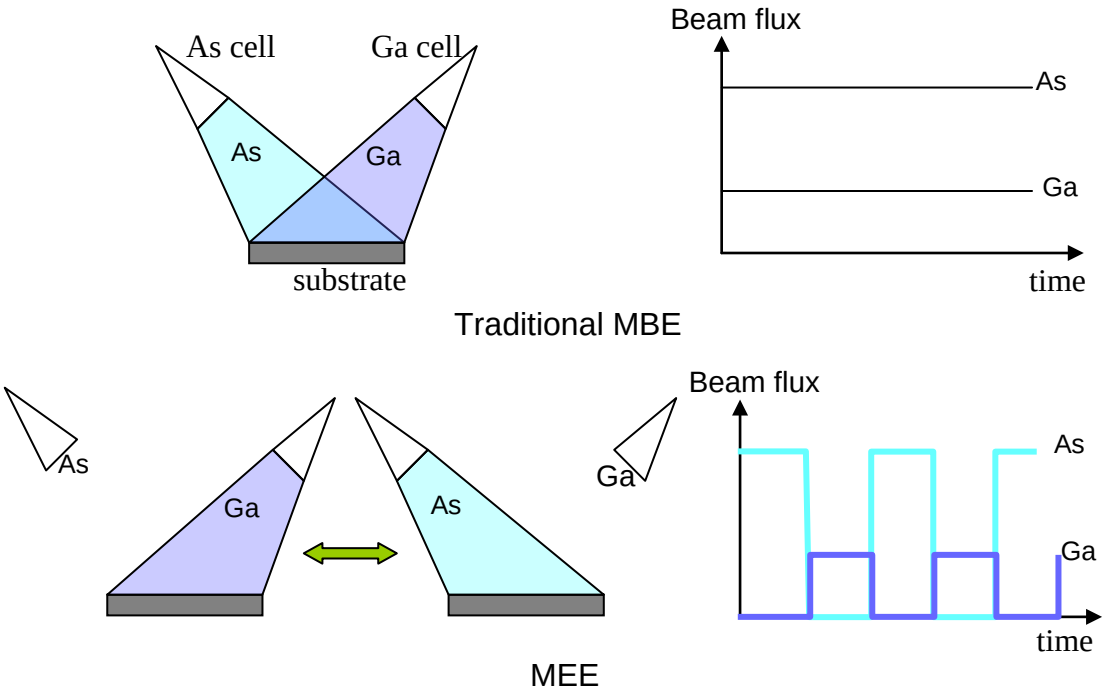

Figure 3.2 Difference between traditional MBE and MEE growth.

Ga atoms can be too mobile at very high temperatures and form islands in one place. Therefore the high Ga mobility achieved by lowering the As flux at a relatively low surface temperature is preferred for good quality films.

Obviously, if using MEE to grow the entire film, growth rate and throughput would be a great concern. In our study, this was not a problem because we only used MEE for the initial few layers. We take great care in the beginning because the initial growth stage plays the most critical role in determining the film quality.

3.2 Si substrate preparation and GaAs film growth

3.2.1 Si substrate

Effects of substrate orientation on the epilayer morphology, growth model and the device performance have been carefully studied. Since a majority of Si devices are

built on (100) substrates, we only studied GaAs growth on (100) Si. It has been largely agreed that GaAs on Si {100} misoriented toward <110> with an tilt angle between 2° and 4° shows the best surface roughness and minimal APB density [1, 8]. In addition to that, titled substrates reduce the dislocation density and preferentially induce type I dislocations whose Burgers vectors are in the plane of the nominal substrate orientation and whose dislocation lines run parallel to the interface and do not generate threading dislocations [8]. For illustration purpose, Fig. 3.3 shows a nominal (100) surface and a vicinal (100) substrate with a tilt angle toward the [011] direction.

In our study, the LT-GaAs layers were grown on both nominal (100) Si substrates and vicinal (100) Si substrates oriented 4° off toward [011].

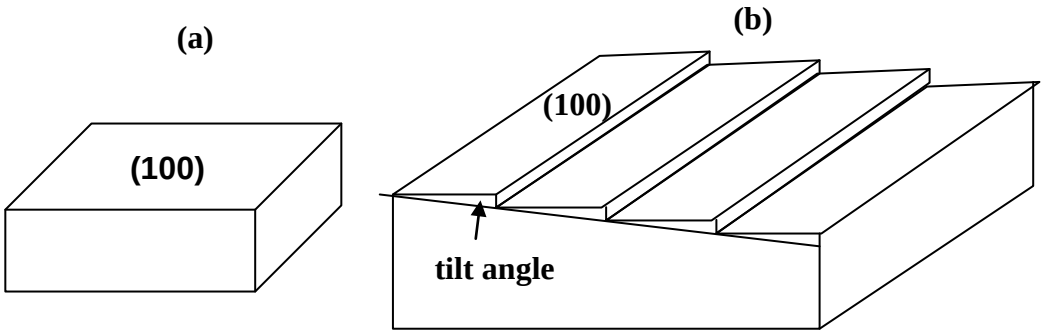

Figure 3.3 Sketch illustrating the tilted substrate surface. (a) a nominal (100) surface. (b) a vicinal substrate with an angle of tilt off the (100) plane toward the [011] direction. The tilt angle is named with respect to the (100) plane. Atomic steps can be seen in such a surface.

3.2.2 Si surface cleaning

The starting Si wafer surface, which serves as the interface between the GaAs epilayer and the substrate, plays a most important role in the GaAs on Si growth. It is the initial nucleation stage and growth mode at this interface that mostly determines the GaAs film quality. For example, when GaAs growth is initiated, the As atoms have no first-order preferential nucleation sites on a clean Si surface. However, if there are

contaminants present, due to energy consideration, Ga or As atoms may pile up on or around the contaminants and form structural defects and antiphase domains. For the epitaxial growth to be successful, it is mandatory to have an atomically clean starting surface.

In general, a clean wafer surface needs to satisfy the following requirements: particle free, metallic contamination free, organic impurity free, moisture molecule free, native oxide free, surface micro-roughness free, charge free, etc [15]. Most of the contaminants can be removed by wet cleaning at room temperature. The biggest problem for low temperature processing is the native oxide removal. In traditional GaAs-on-Si surface preparation process, the Si wafer native oxide is first etched by HF and then a thin fresh oxide layer is intentionally formed to passivate the surface. This passivation oxide is later desorbed in the growth chamber right before GaAs epitaxial growth is initiated. Multiple approaches have been studied to obtain an oxide-free surface. These include: high temperature thermal desorption; Ar ion beam sputter cleaning [16]; oxide reduction by incident beams of Si [17], Ga [18] and In [19], or Ge [20]; reaction with reactive gases such as silane [21] and germane [22]; NF_3 gas etching [23], surface bombardment with hydrogen plasma [24] and other particles [25]; and electron beam irradiation [26, 27], etc. But for complete removal of the chemically-stable oxide layer in these approaches, either the desorption temperature is still high (above 700 °C), or other energy sources are needed.

To lower the surface cleaning temperature, the chemical bonding for the passivation layer should not be as stable as SiO_2. Based on this idea, a class of methods targeting hydrogen passivation of the Si surface gained popularity [28-35]. By using HF acid etching as the last wet-clean step, a hydrogen-terminated Si surface can be obtained. The hydrogen atoms can prevent the surface from oxidation and maintain surface cleanliness by reducing the sticking coefficient of contaminants. It has been shown that the H-terminated Si (100) surface is stable for several hours in vacuum and at least several tens of minutes in air [30]. Some study on HF-dipped wafer storage even indicated that the thickness of a monolayer of SiO_2 (3 Å) was only reached after 15-20 days of storage in air [34].

Considering different approaches, we decided to use hydrogen-passivation to lower the Si surface *in situ* cleaning temperature before growth. The substrates were chemically cleaned in a class-100 clean room at Stanford University Center for Integrated Systems, using a modified RCA cleaning method. Wafers were first immersed into a 4:1, H_2SO_4: H_2O_2 solution at 90 °C for 10 minutes to remove trace organics. For removal of trace metal ions, samples were submerged into a 5:1:1, H_2O : H_2O_2 : HCl solution at 70 °C for 10 minutes. A 30 seconds dip in a 50:1, H_2O : HF solution was done for oxide etching. A final quick dip into a low concentration HF solution was done immediately before loading the wafers into the MBE loadlock chamber to achieve hydrogen passivation.

To have a rough idea of the surface cleanliness after this step, a heated X-ray Photoelectron Spectroscopy (XPS) analysis was performed on a Si wafer chemically cleaned with above procedure. Our MBE system doesn't have an XPS system attached and the XPS analysis chamber is located in a non-clean room environment. The Si wafer was vacuum sealed in a desiccator after being cleaned in the clean room, and then transported and loaded into the XPS chamber with a nitrogen glove bag. It is expected that this process adds some amount of additional contamination to the wafer surface. The wafer was heated up to 400 °C in the XPS chamber. Complete survey scans found only small amounts of residual carbon and oxygen, as shown in Fig. 3.4. We believe the carbon and oxygen on the hydrogen-passivated surface are due to exposure to air and the wafer handling process. In Fig. 3.4 (b), the signal is enlarged by 100 times for a clear examination of the contamination evolution with temperature. It is obvious that the carbon peak quickly decreases to be indistinguishable with the baseline. The oxygen peak also drops quickly with temperature. Unfortunately, further heating is limited by the XPS chamber. Since the heating experiment is rarely done, although we pre-baked the chamber overnight, the XPS chamber still started to outgas heavily by itself. Further heating only built more contaminations onto the wafer surface. We will observe further surface development in the MBE chamber with RHEED.

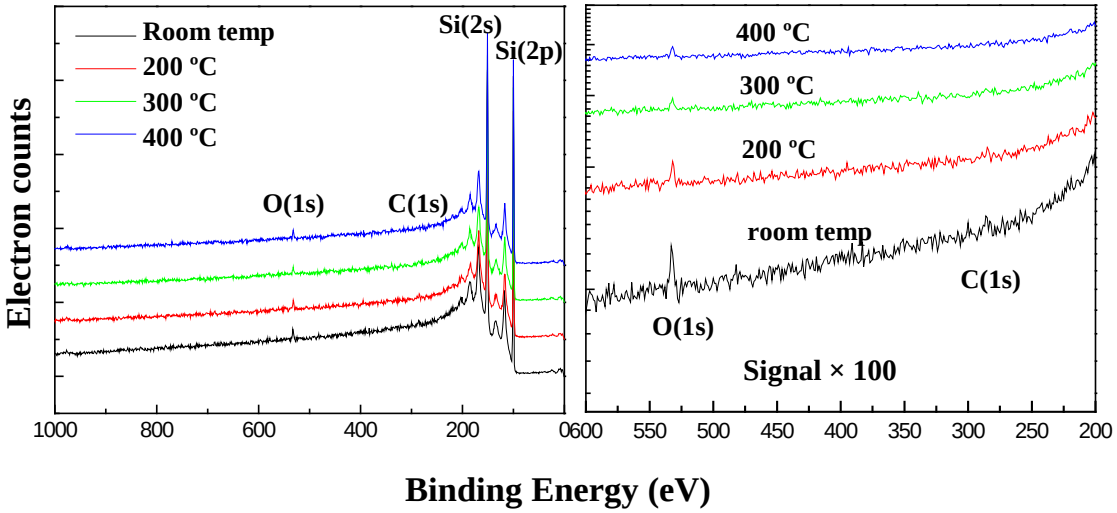

Figure 3.4 XPS survey scan of a Si wafer surface after being wet-cleaned with the procedure described in the text above. (a) full range survey scan of the surface. (b) zoom up around the C and O peak energies. The signal in (b) is enlarged by 100 times compared to (a).

3.2.3 *In situ* Si surface clean and GaAs film growth

After the *ex situ* chemical clean described above and a final HF dip, wafers were loaded into the MBE loadlock chamber and baked at 200 °C for 1 hour to remove moisture and gases. Then they were loaded to the growth chamber via the transfer tube. Following the LT-GaAs on GaAs study, all samples were grown in a solid source Varian Gen II MBE system. The gallium flux was supplied by a thermal effusion cell and dimeric arsenic (As_2) was provided through a valved thermal cracker. For the wafers investigated here, a ~ 0.5 μm thick layer of GaAs was grown at a rate of 0.2 μm/hr with an As_2/Ga beam-equivalent-pressure (BEP) ratio of 6.

In situ RHEED was used to monitor the surface cleaning and the surface condition at each stage of film growth. During the heat cleaning step to desorb the passivating hydrogen atoms and any residual surface oxide, the Si surfaces typically start to exhibit a streaky 2 × 1 reconstruction pattern at temperatures as low as ~ 450 °C (Fig. 3.5), indicating a clean smooth surface. To obtain a thoroughly cleaned surface, samples were then subsequently baked at ~ 550 °C for 20 minutes (although the RHEED pattern at ~ 480 °C was almost the same as that seen at ~ 550 °C) and

then cooled down to the growth temperature (~ 250 °C) with exposure to an As flux to avoid any further contamination from the chamber during the cooling process. The As flux serves both as a contamination protection and a pre-layer for the purpose of anti-phase domain (APD) suppression. The Residual Gas Analyzer (RGA) monitoring shows that the hydrogen desorption peak is ~ 510 °C. This is consistent with the literature [36, 37] that the desorption peak maxima were 510 °C for monohydrides and 402 °C for dihydrides on a Si (100) surface. Thus by holding for a longer time, this cleaning temperature could be further lowered when growing on wafers with completed CMOS circuits. This pre-growth substrate preparation temperature of 550 °C is 50 °C – 100 °C lower than the claimed lowest silicon surface cleaning temperature reported to date [33, 38].

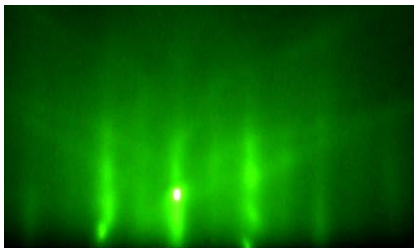

Figure 3.5 Si surface RHEED shows a 2×1 reconstruction at as low as ~ 450 °C.

A two step growth process was usually used in traditional GaAs-on-Si growth [2]. The so called two step growth means to first initiate the growth at low temperatures and then subsequently increase to a higher growth temperature. The low initial temperature usually leads to good surface morphology but the film quality is not good due to high density of stacking faults, micro-twins, and point defects. But the second, higher temperature growth step has an annealing effect upon the initial buffer layer to reduce or eliminate the defects. Therefore both good morphology and crystal quality can be achieved by using this two step process.

A modified two-step growth process incorporating migration enhanced epitaxy (MEE) was used in our study. The LT-GaAs growth was initiated with 10 migration-

enhanced-epitaxy (MEE) cycles with 5 seconds exposure to Ga and As flux respectively and 5 seconds pause in between. During MEE, the As/Ga BEP ratio is dropped to 3× to minimize As residue during Ga exposure period. The benefits of using MEE have been described above. Following the LT-GaAs layer growth, the samples were annealed at ~ 600 °C for 10 minutes either in the MBE growth chamber under an As overpressure or in a rapid thermal annealing (RTA) chamber under N_2 ambient. During RTA annealing, the samples were covered with a protective GaAs wafer to prevent As desorption. A local area laser annealing technique could also be used to avoid this high temperature anneal on the whole wafer area when growing on real CMOS chips, or the new surface laser anneal technology (for example, the DSA technology from Applied Materials, Inc. or other millisecond laser anneal technology) could be used to lower the thermal budget to the underlying circuits.

After the MEE cycles, the RHEED pattern became dim and spotty (Fig. 3.6 (a)), indicating initial island formation and three-dimensional growth. During growth, the RHEED pattern changed and the LT-GaAs layer grown on Si became 1 × 1 (Fig. 3.6 (b)). Depending on growth conditions, the LT-GaAs patterns could be 1 × 1 or 2 ×

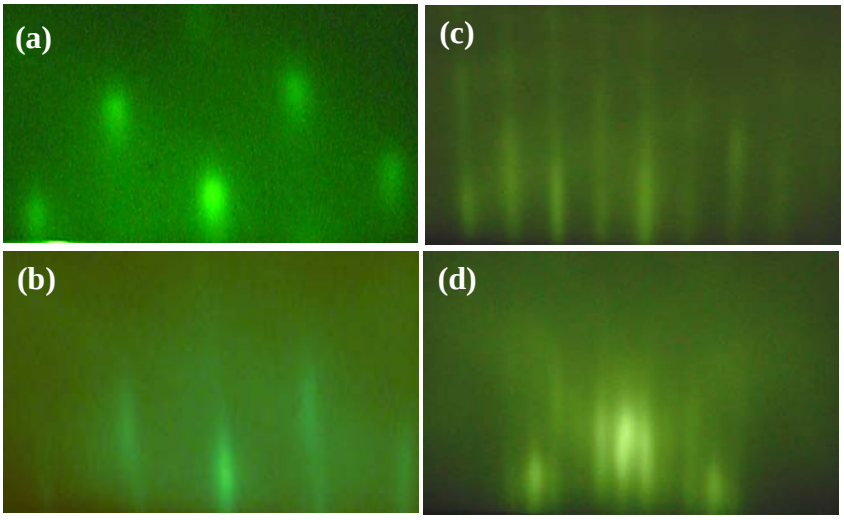

Figure 3.6 RHEED patterns for various stages of LT-GaAs on Si growth. (a) Typical pattern after exposure to arsenic and MEE cycles. (b) After LT-GaAs growth. (c) [011] azimuth after in-chamber annealing. (d) $[0\bar{1}1]$ azimuth after in-chamber annealing.

2. This behavior is similar to LT-GaAs grown on a GaAs substrate. Upon *in situ* annealing, the RHEED patterns exhibited a streaky 2 × 4 reconstruction (Fig. 3.6 (c) and (d)), indicating high quality single domain GaAs layer with a smooth surface. All samples appear specular and featureless to the naked eye and under an optical microscope after removal from the MBE system.

3.3 LTGaAs-on-Si film characterization

3.3.1 AFM study

The roughness of the film surface was observed using Atomic Force Microscopy (AFM). Several 2 μm × 2 μm area scans were done. As shown in Fig. 3.7, for 0.5 μm thick LT-GaAs grown on a nominal (100) Si substrate, the root-mean-square (rms) roughness was ~ 1.0 nm. For the same thickness LT-GaAs layer grown on a vicinal (100) Si substrate (4° miscut toward [011] direction), the rms roughness was ~ 0.5 nm. The AFM section analysis on the same imaging areas showed the peak-to-peak variation across the surface was ~ 6 nm for the film grown on the nominal (100) substrate and ~ 3 nm for the mis-oriented substrate. This roughness is approximately an order of magnitude smaller than the best previously reported data [39]. The starting Si wafer roughness was measured after being cleaned using the

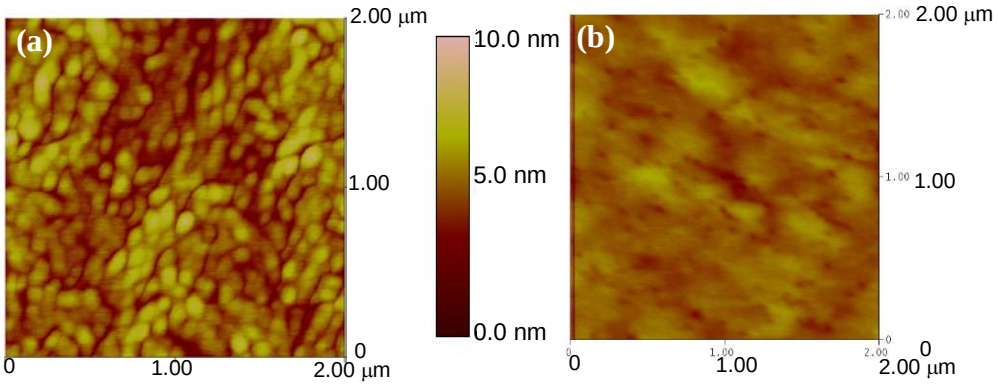

Figure 3.7 2 μm × 2 μm AFM scan images. (a) 0.5 μm thick LT-GaAs layer grown on a nominal (100) Si substrate. Rms roughness is ~ 1.0 nm and peak-to-peak variation is ~ 6 nm. (b) 0.5 μm thick LT-GaAs layer grown on a vicinal (100) Si substrate 4° misoriented toward [011] direction. Rms roughness is ~ 0.5 nm and peak-to-peak variation is ~ 3 nm.

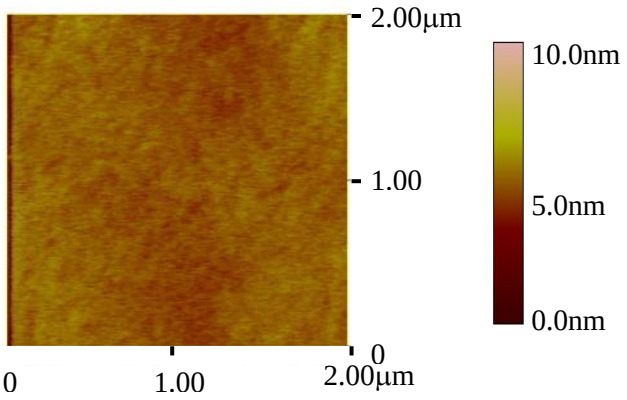

Figure 3.8 2 µm × 2 µm AFM surface scan on blank reference nominal Si (100) wafer after wet cleaning. Image rms = 1.047 nm.

same method (Fig. 3.8.) The rms roughness was 1.047nm. The films grown with our technique are obviously very smooth when compared to the roughness of the blank Si substrate.

As a side note to this topic, the GaAs on Si nucleation mode depends strongly on growth parameters and substrate temperature is one of the most important factors. It was reported [40] that two-dimensional-like nucleation of GaAs on Si could be obtained when growth is initiated at room temperature. We also briefly studied room temperature initiation of the LT-GaAs on Si. Fig. 3.9 shows the RHEED pattern evolution during the process. Fig. 3.9 (a) shows the starting 4° off-axis (100) Si surface chemically cleaned *ex situ* and thermally cleaned *in situ* as above. After ~ 20 Å GaAs was deposited on the substrate at room temperature (~ 30 °C), RHEED indicated a completely amorphous layer (3.9 (b)). As the film was being annealed, RHEED monitored the surface change. It shows that spots started to show at above 150 °C and gradually change to short streaks (3.9 (c)). Above 400 °C, the normal 2×4 surface reconstruction started to appear (3.9 (d)). This indicated a solid-phase epitaxy process happening in this thin initial layer. Subsequently, the temperature was dropped to LT-GaAs growth temperature at ~ 250 °C and ~ 0.5 µm thick layer was grown. Fig. 3.10 shows the 2 µm × 2 µm AFM surface scan for the LT-GaAs grown using the

above procedure. The image rms roughness is ~ 0.45 nm and the peak-to-peak variation is less than 3 nm. Due to time limitations, no further study was done on room temperature nucleation. However, the good surface morphology obtained by this method is potentially useful for epi-film property engineering.

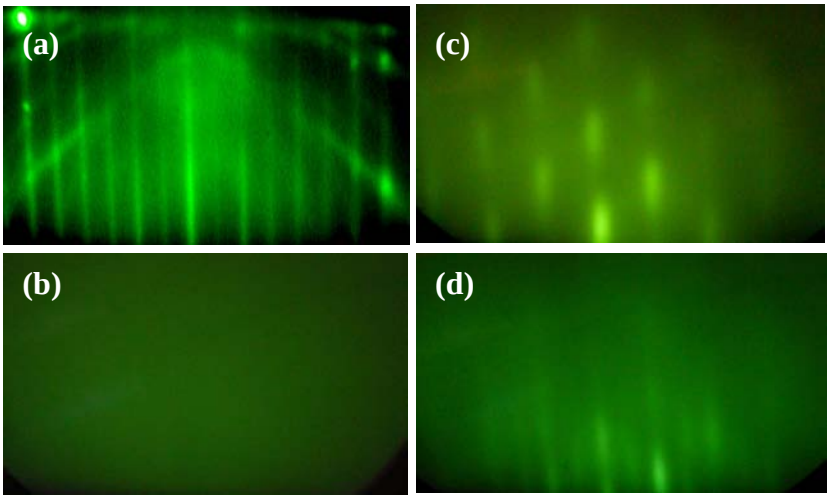

Figure 3.9 RHEED patterns for different stages when LT-GaAs on Si growth was initiated at room temperature. (a) Starting clean Si substrate surface. (b) After 20 Å GaAs deposition at 30 °C. (c) Spots appear at > 150 °C. (d) Weak reconstruction appears at > 400 °C.

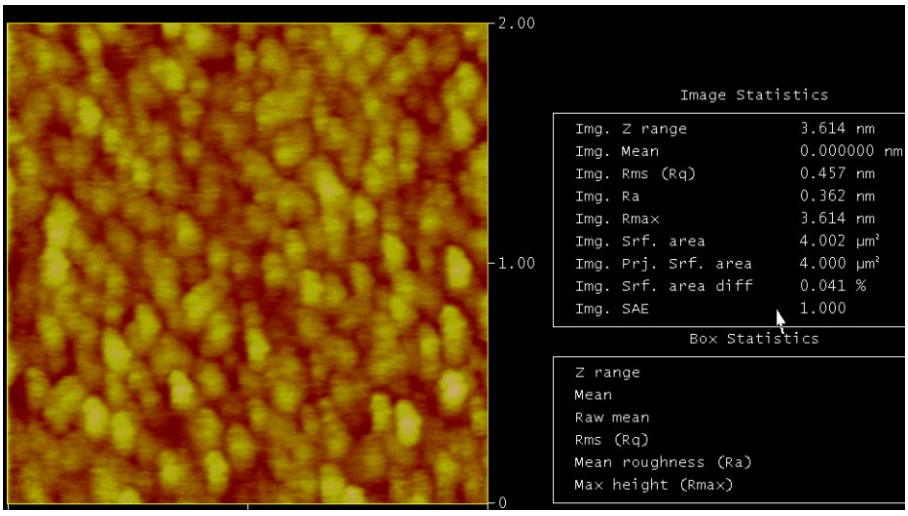

Figure 3.10 2 µm × 2 µm AFM surface scan for 0.5 µm LT-GaAs grown on 4° off-axis (100) Si substrate. The image rms = ~ 0.45 nm, the peak-to-peak variation is less than 3 nm.

3.3.2 XRD study

APDs are important crystal defects to be considered when growing GaAs films on Si (100) substrates. There are various experimental techniques to detect the presence and size of antiphase domains. These include: anisotropic etch, x-ray diffraction, Raman scattering, TEM, RHEED, and p-n GaAs-Si junction, etc [2]. Each technique has its unique advantages and limitations. In addition to the capability of detecting the APDs, X-ray diffraction (XRD) is a powerful tool in evaluating the overall thin film properties. Therefore, the LT-GaAs film quality was studied by high-resolution (0.0001°) X-ray diffraction (XRD).

In XRD, the structure factor (F) of GaAs is composed of the Ga atomic form factor (f_A) and the As atomic form factor (f_B). Due to the difference between f_A and f_B, some peaks that would have been annihilated for non-polar crystals, such as Si, appear, such as (002), (006) …. These peaks are called superstructure reflections. The basic peaks a Si crystal would exhibit such as (004), (008) … are called fundamental reflections. [2, 41]

The fundamental reflection intensity is

$$I_F = \frac{1}{2}\frac{(f_A + f_B)^2 \sin^2 \pi NQ}{\sin^2 \pi Q} \tag{3.1}$$

and the superstructure reflection intensity is

$$I_S = (f_A - f_B)^2 \frac{N}{\gamma^2 + (\pi \Delta Q)^2} \tag{3.2}$$

where f_A and f_B are Ga and As atomic form factors, N is the number of atoms in a crystalline direction parallel to the scattering vector Q, where $Q=(4\pi/\lambda)\sin\theta$, λ is the x-ray wavelength and θ is the scattering angle, γ is the probability for the formation of an APD between any two lattice sites.

The equations above demonstrate the difference between the two types of peaks. The fundamental reflections are due to the lattice structure and they provide crystal information, such as lattice parameters, residual strain, and film quality, etc. The superstructure reflections arise because of the ordering of Ga and As atoms. Therefore, the GaAs (002) superstructure reflection is very sensitive to APDs, while

the (004) fundamental reflection is not affected by APDs. In XRD, many factors can contribute to the peak broadening, for example, inherent Bragg reflection width, instrumental resolution, film stress, stacking faults, defects, such as APDs, etc. However, the only factor that selectively broadens the superstructure reflection is the antiphase domain [2, 41]. Therefore the (002) peak broadening is a good indication of APD information. To experimentally determine if APDs exist in an ordered crystal like GaAs, the widths of the superstructure and fundamental reflections should be compared.

Fig. 3.11 is the XRD spectrum for a LT-GaAs on Si sample. The ratio between the GaAs (002) peak intensity and the GaAs (004) peak intensity is comparable to that of a conventional GaAs homoepitaxy reference wafer. The FWHM (full-width-at-half-maximum) of the (002) and (004) peaks for LT-GaAs grown on both nominal and vicinal Si samples are summarized in Table 3.1. It is clear that for growth on both substrates, the (002) superstructure peak is not broadened compared to the (004) fundamental peak. This indicates that the APD density is below the detection limit of XRD [2, 41]. In addition, a decrease in FWHM of both peaks was observed when growing on the vicinal substrate compared to the nominal (100) substrate.

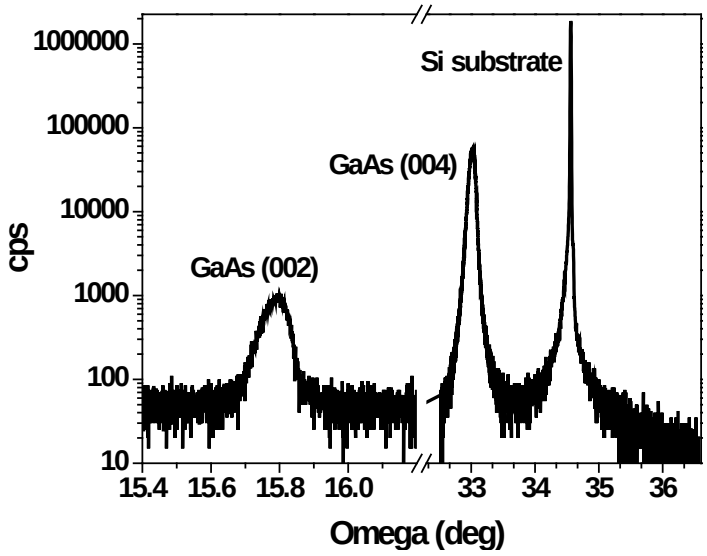

Figure 3.11 XRD spectrum for an annealed LT-GaAs sample grown on a nominal (100) Si substrate.

Table 3.1 GaAs peak FWHM comparison for LT-GaAs films grown on different Si substrates.

	GaAs (004) peak FWHM	**GaAs (002) peak FWHM**
on nominal (100) substrate	396 arcsecs	331 arcsecs
on vicinal (100) substrate	357 arcsecs	276 arcsecs

3.3.3 MSM switch characterization

In our study, we care most about the switch performance made with the LTGaAs-on-Si film. Using the materials grown with above procedure, MSM photoconductive switches were made. The design and fabrication is the same as described in chapter 2. Switches with an interdigitated pattern were fabricated by depositing titanium/gold contact metal on the LT-GaAs epi-layers through a standard lift-off process. Devices with different finger spacings and finger widths were patterned in a ~ 20 μm × 20 μm area, the approximate optical spot size used for characterization. The switches were placed in the middle of coplanar waveguide transmission line structures for high-speed characterization. The same time-resolved electro-optic sampling technique described in chapter 2 was used to measure the ps transient in the switches.

An output waveform from a photoconductive switch made from LT-GaAs on a vicinal (100) Si substrate is shown in Fig. 3.12. As we already know, the amplitude and width of the signal depend on sample growth conditions, anneal conditions, switch pattern, and testing parameters, etc and there is always a tradeoff between the switch responsivity and speed. The dependence of the switch responses on applied bias, optical pulse energy and switch pattern was similar to that observed for devices made from LT-GaAs grown on GaAs substrates as we have shown in chapter 2 and won't be repeated here. The main purpose of this study is to demonstrate the possibility of direct growth of LT-GaAs on Si at low temperatures as an alternative to flip-chip bonding MSM switches made from LT-GaAs on GaAs material onto Si chips. Therefore, the reference we choose for comparison is the LT-GaAs on GaAs wafer

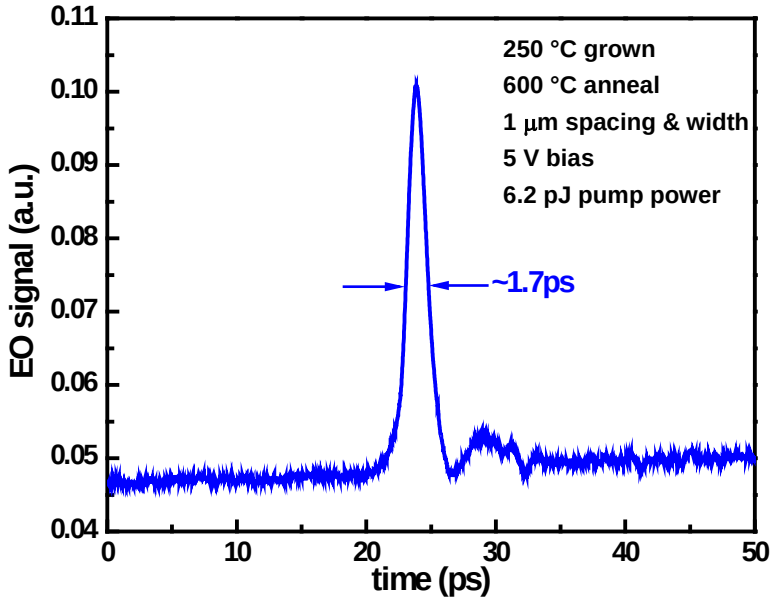

Figure 3.12 An output waveform characterized using electro-optic sampling technique for a photoconductive MSM switch made from LT-GaAs on a vicinal (100) Si substrate. The switch has 2 μm finger width and 1 μm finger spacing, tested under 6.2 pJ optical energy and 5 V bias voltage.

that we actually used for the two-channel prototype ADC which exhibited excellent performance. FWHM of the signal varies around 2 ps for both samples grown on nominal and vicinal Si (100) and the reference LT-GaAs on GaAs sample, depending on testing conditions.

Fig. 3.13 shows a comparison of the photocurrent as a function of optical pump power for switches made from a LT-GaAs film on a vicinal Si substrate and the reference homoepitaxial wafer. It shows that the responsivity of the switch slowly saturates with increasing pulse power, as expected. The remarkable feature of this plot is that the responsivity of these switches is quite comparable for LT-GaAs on Si versus LT-GaAs on GaAs, although presumably, a high density of dislocations exists in the material grown on Si. Here, the reference LT-GaAs on GaAs wafer is the one we actually used for the two-channel prototype ADC which exhibited excellent performance as shown in chapter 2. Both switches have 1 μm finger width. Fig. 3.13 also indicates that the responsivity increases with decreasing finger spacing, at the cost of device capacitance, which also increases for smaller finger spacing. This is another tradeoff in choosing appropriate device size.

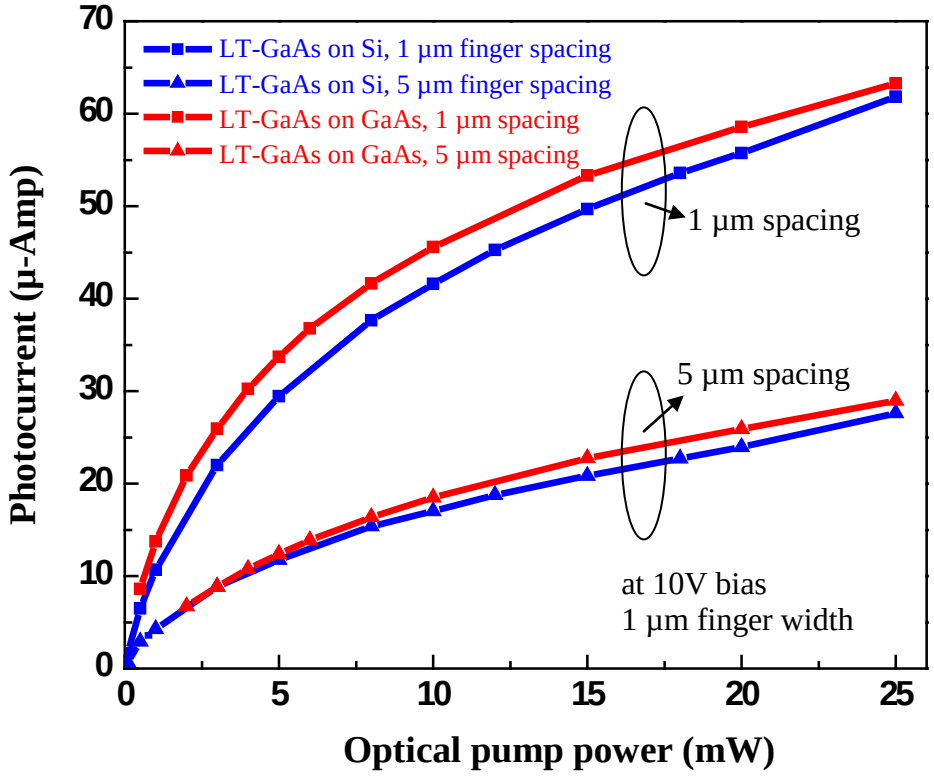

Figure 3.13 A comparison of the photocurrent as a function of optical pump power for switches made from LT-GaAs films on vicinal (100) Si substrates and the reference LT-GaAs on GaAs wafer. The reference wafer is used in the demonstrated prototype two-channel ADC in chapter 2. Both types of switches have 1 µm finger width and the data shown were taken at 10V bias voltage.

The dark current is a primary concern for device applications. Fig. 3.14 shows that the dark current of LT-GaAs on Si switches is reasonably low, in the sub µAmp level, although it is approximately three orders of magnitude higher than the reference LT-GaAs on GaAs wafer. The switch made on a thicker (1 µm) LT-GaAs film exhibits lower dark current by moving farther from the defective Si-GaAs interface. To further reduce the dark current, we can incorporate an AlGaAs barrier layer between the GaAs and contact metal, or choose another contact material, such as WSi_x [42]. These features should be tested in future research.

By optimizing the material quality and switch pattern, LT-GaAs grown directly on Si presents a promising alternative to bonding LT-GaAs on GaAs material to Si circuits.

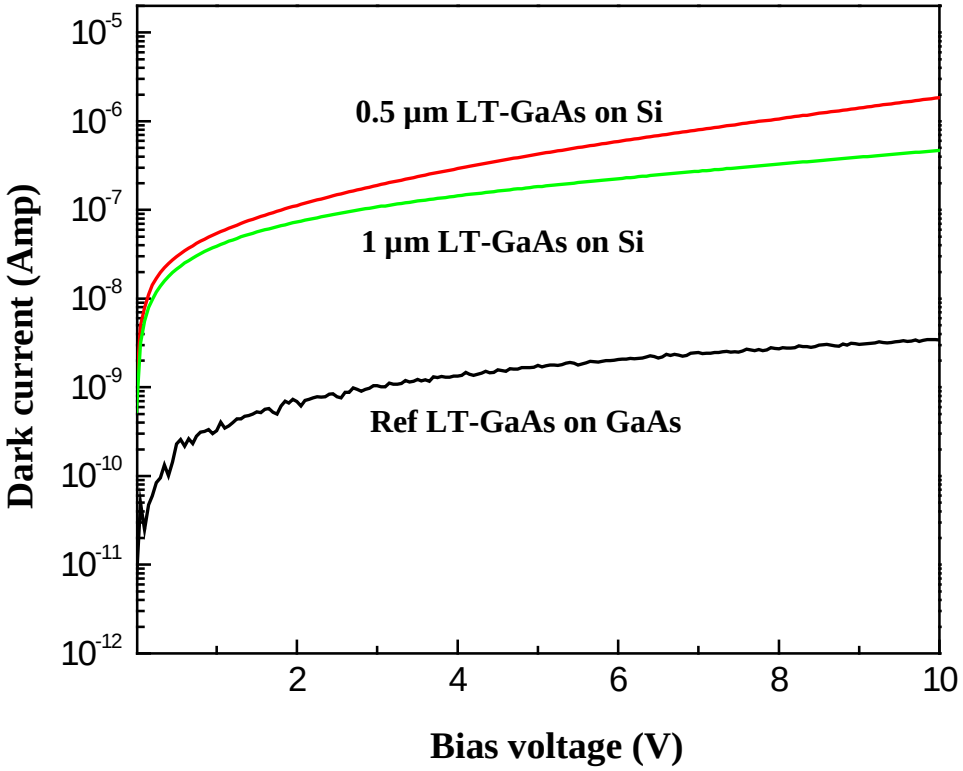

Figure 3.14 Dark current of switches made from different materials. The two LT-GaAs on Si materials with different thickness were grown on vicinal (100) substrates under the same conditions. The LT-GaAs on GaAs is the reference wafer used in the prototype ADC described in chapter 2.

3.4 Summary

In summary, we have grown GaAs directly on Si substrates at low temperatures (~ 250 °C). Both the wafer cleaning and film growth temperatures are lower than the Si-Al eutectic temperature and safe for finished CMOS circuits with Al metal contacts. *In situ* RHEED patterns showed a clean, reconstructed Si surface before growth, and a reconstructed GaAs film after post-growth annealing. The film is specular and AFM measurements reveal less than 1 nm rms roughness. XRD measurements indicate good film quality and negligible APD density. Time-resolved electro-optic sampling characterization shows that a full-width at half-maximum

(FWHM) switching time of ~ 2 picoseconds was achieved and the performance of LT-GaAs switches on a Si substrate is comparable to its homoepitaxy counterpart which was used in our prototype ADC with demonstrated outstanding performance. The successful low-temperature growth of GaAs on Si substrates promises the possibility of monolithic integration of ultra-fast LT-GaAs switches with fabricated Si CMOS circuits.

3.5 Bibliography

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Chapter 4

Photoconductive Switches Made from Polycrystalline GaAs Grown on SiO_2

GaAs was directly grown on SiO_2-coated Si substrates at low temperatures (~ 400 °C). All the temperatures involved are safe for completely finished CMOS circuits. XRD and TEM analyses show the polycrystalline nature of the films and columnar grain structure. Time-resolved electro-optic sampling characterization shows that the performance of the poly-GaAs MSM switches is comparable to or exceeds its homoepitaxy counterpart on a GaAs substrate. These results make it completely practical to realize on-chip monolithic integration of GaAs switches with a finished Si chip.

4.1 Motivation

As described in chapter three, the growth of LT-GaAs on Si substrates was successful. The next natural evolution is to directly grow LT-GaAs on completely finished Si circuits, as we proposed. It is quite doable if in the first place, we designed the CMOS chip with this in mind and leave appropriate areas in the chip specifically for the later processing steps related to the integration of LT-GaAs devices. In practice, there are some process intricacies involved. After a chip is fabricated with multi-layers of interconnects, in order to grow LT-GaAs on Si, the window areas of the chip need to be etched all the way down to the Si substrate to expose the Si surface. Since modern ICs usually have six or more layers of metal interconnects, if suitable areas were not intentionally left for this specific purpose, the deep etching will involve both dielectrics and metals in alternate layers. This will require multiple etching steps and makes the process quite complicated. Also, even if the Si windows are available for GaAs growth, filling these deep trenches potentially creates significant step coverage problems.

As we mentioned in chapter one, there are various techniques to achieve picosecond photoconductivity. In addition to our choice of low temperature growth of GaAs films, deposition of polycrystalline or amorphous semiconductors has been demonstrated as well to have a response time in the picoseconds range [1, 2]. To simplify the processing and avoid the complexities mentioned above, we studied direct growth of GaAs at relatively low temperatures on SiO_2.

In our study, growing GaAs on amorphous SiO_2 at around 400 °C results in polycrystalline GaAs (poly-GaAs). Similar to LT-GaAs where excess As related defects are used to reduce carrier life times, the grain boundaries in poly-GaAs also act to make this material “fast”. Polycrystalline materials are usually modeled as single crystallites joined together with grain boundaries. The grain boundaries are composed of disordered atoms and therefore contain large concentration of defects due to incomplete atomic arrangement and bonding. These defects form trapping centers and immobilize free carriers. Therefore a polycrystalline material has high mobility

regions within each grain and effective trapping and recombination centers at the grain boundaries. An electron-beam-induced-current (EBIC) study showed that, for 1-2 μm grains in poly-GaAs, the carrier diffusion lengths are equal to bulk diffusion lengths in single crystal materials, but high recombination states exist at the grain boundaries and the recombination velocity is inversely proportional to the grain size [3]. When the grain size is small, most excited photocarriers can be quickly trapped at the grain boundaries because the distance of the recombination states surrounding the small grains (grain size) is less than the diffusion length. The carrier lifetime (τ) depends on the bulk (τ_B) and surface lifetime (τ_S) through equation [3]:

$$\frac{1}{\tau} = \frac{1}{\tau_B} + \frac{s}{V/A} \tag{4.1}$$

where V is the grain volume and A is the grain surface area, s is the surface recombination velocity, $\tau_S = (V/A)/s$ is the surface lifetime, reflecting recombination in the volume of the grain due to the states in its surface area.

During the last three decades the recombination at grain boundaries in semiconductors has been studied extensively because of its technological importance in increasing fields of applications. For example, due to the application of poly-Si and poly-GaAs in solar cell development, the grain boundary recombination and its influence in the electrical properties of devices attracted considerable investigation [4, 5].

Our simple growth structure is shown in Fig. 4.1 where poly-GaAs is directly grown on top of the SiO_2/Si_3N_4 passivation layer of Si circuits. Dielectrics such as SiO_2 and/or Si_3N_4 are almost always available on top of completed circuits as the final passivation. If poly-GaAs grown at low temperatures on passivation dielectric layers

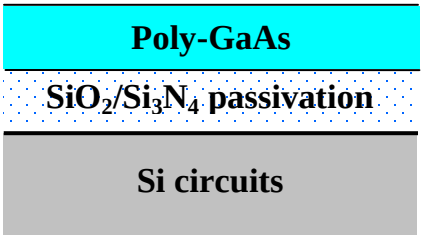

Figure 4.1 Film structure of poly-GaAs on top of a finished chip.

can be successfully used to make ultrafast photoconductive switches, this approach will open a whole new world of applications and have much greater impact than our study here. In addition, despite the practical success of using off-axis substrates to eliminate antiphase domains, as we have shown in chapter 3, using vicinal substrates does require process modifications in Si-IC fabrication and the circuits made on off-axis wafers have some undesired characteristics, therefore this is a rather unwelcome approach by the device designers. Since growing GaAs on dielectrics instead of on Si surface removes the concern of forming antiphase domains, we do not need to use off-axis Si wafers, which is applaudable by the IC community.

4.2 Film growth and characterization

4.2.1 Film growth

To simulate the actual surface of Si chips with dielectric passivation, we first need to have SiO_2 films on top of Si (100) wafers. In our experience, either thermal growth of 800 nm thick SiO_2 films at 1100 °C in a furnace tube or PECVD depositing 500 nm thick SiO_2 films at ~ 350 °C did not make much difference in the final poly-GaAs film properties.

The same Varian Gen II MBE system was used for the GaAs film growth. The SiO_2-coated Si wafers went through the same loading procedure as described in previous chapters into the MBE loadlock chamber and baked at 200 °C to remove moisture and gases. After being loaded into the MBE growth chamber, various thicknesses (0.5 – 1.5 μm) of GaAs were grown at different temperatures (350 – 500 ^oC). We started the growth with an As prelayer and 10 MEE cycles, followed by regular GaAs growth at an As_2/Ga BEP ratio of 10. The grain size is a strong function of growth temperature and film thickness, and largely determines the carrier dynamics.

4.2.2 TEM

Transmission Electron Microscopy (TEM) images were taken to observe the grain structure. Fig. 4.2 (a) is a TEM diffraction pattern taken on a cross-sectional sample of a 0.5 μm thick GaAs film grown at 400 °C on SiO_2. It clearly indicates that the material has polycrystalline nature, with {111} grains being the most abundant. Fig. 4.2 (b) and (c) are a pair of bright field and dark field cross-section images taken of the same area of the same sample. The dark field image was taken by placing the aperture in the {111} diffraction beam. It shows that the eventual grains are columnar, with average grain size in the range of 0.1 to 0.2 μm. Typically the poly-GaAs average grain size is relatively small when deposited on an amorphous substrate, because there are no preferential nucleation sites and therefore the nucleation takes place randomly. This is shown in the pair of TEM images by observing the GaAs/SiO_2 interface and the initial growing thickness. The grain size is inversely proportional to nucleation density and typically the nucleation density is a function of the substrate materials and surface morphology [6]. Neighboring grains coalesce and form larger columnar grains during growth.

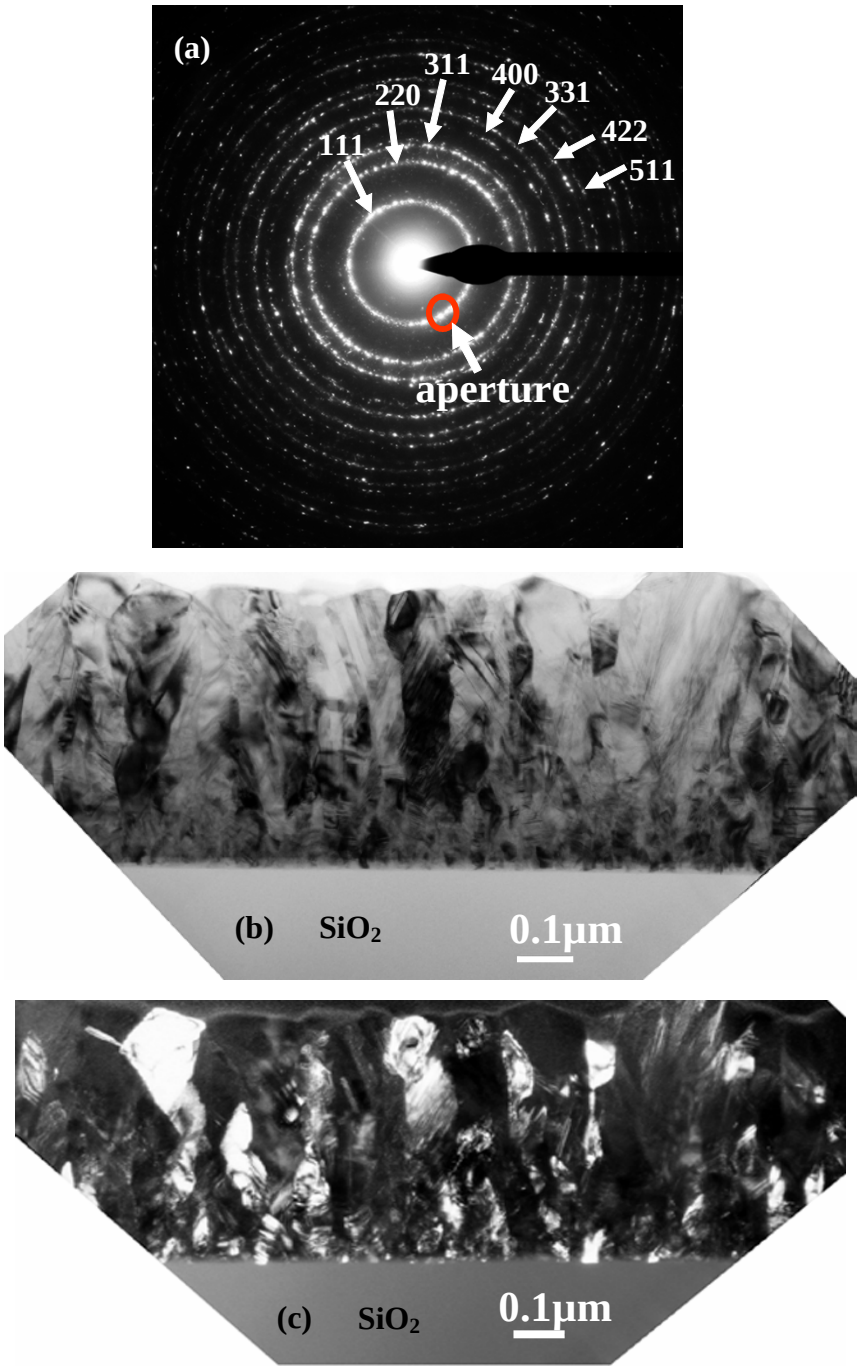

Figure 4.2 (a). TEM diffraction pattern of a 0.5 µm thick poly-GaAs cross-sectional sample grown at 400 °C on SiO_2. The aperture shown in the picture indicates the condition under which the dark field image (c) was taken. (b). Bright field TEM cross-section image. (c). Dark field image taken of the same area under (111) diffraction.

4.2.3 XRD

Poly-GaAs films were grown at different substrate temperatures with various thicknesses. X-ray Diffraction (XRD) was done to analyze the film structures. Fig. 4.3 shows the XRD spectra for poly-GaAs films grown at temperatures ranging from 350 °C to 500 °C. Fig. 4.4 shows XRD spectra for 400 °C grown poly-GaAs with different thicknesses. In these XRD spectra, all the peaks are assigned to GaAs atomic planes, implying the near stoichiometric composition. There is no evidence of As crystallites which are sometimes present in poly-GaAs films obtained by annealing amorphous GaAs [7] due to As segregation. The data show that {111} grains become more dominant as the film thickness increases, which matches the TEM images that show grain coalescence with increasing thickness. At lower growth temperature (350 °C), {111} grains prevail. With increasing temperature, the grain orientations seem to average out, indicating more uniform and random nucleation. Then the {111} grains re-establish their dominance as the growth temperature increases.

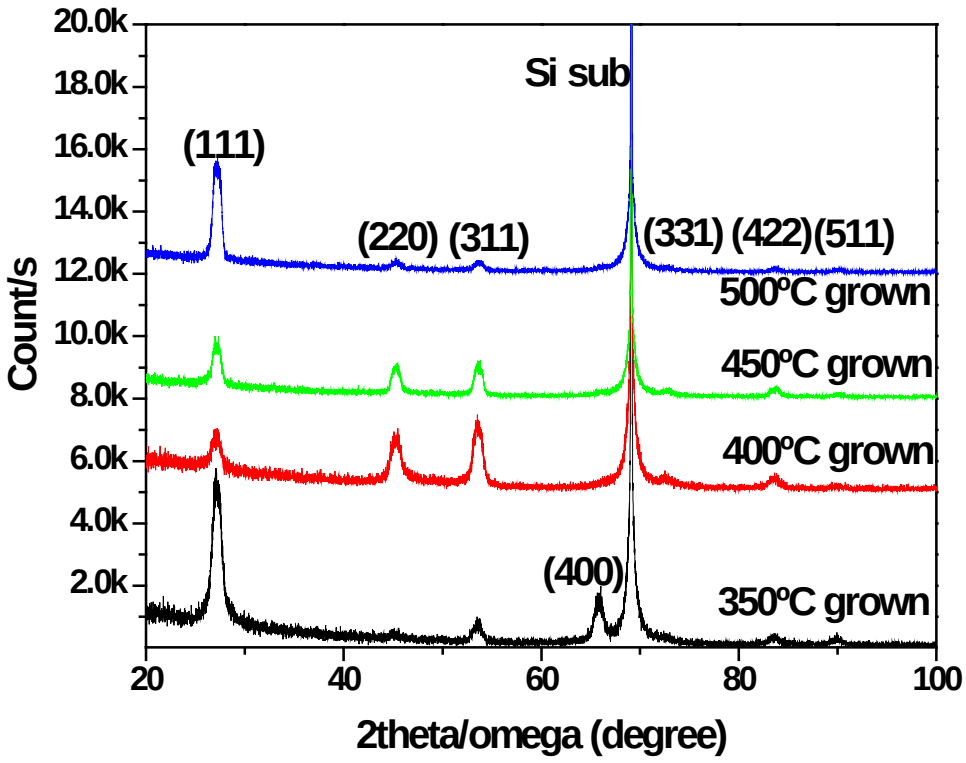

Figure 4.3 X-ray diffraction spectra of poly-GaAs films grown at different substrate temperatures. All films are 1 μm thick except the 500 ºC sample (0.5 μm).

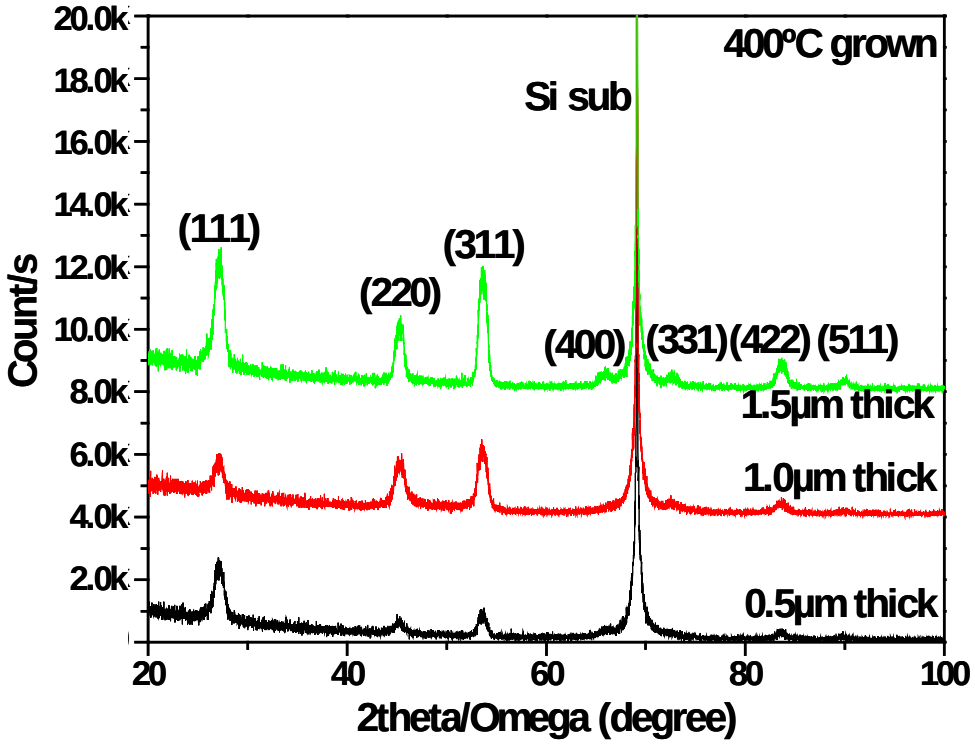

Figure 4.4 X-ray diffraction spectra of poly-GaAs films grown at 400 °C with different thicknesses.

4.2.4 MSM switch characterization

Using the same methods described in previous chapters, we made MSM photoconductive switches with the poly-GaAs materials, and characterized the switch performance using electro-optic sampling and current-voltage (I-V) curve measurements.

4.2.4.1 Switch temporal response

Fig. 4.5 shows a comparison of switch response measured using the electro-optic sampling on two different switches made from a LT-GaAs film on Si and poly-GaAs film on SiO_2, respectively. It shows that the poly-GaAs MSM switches have very similar switching response to those made from LT-GaAs on GaAs and LT-GaAs on Si materials. The FWHM can also be made to be around 2 ps. Similar to the LT-GaAs on GaAs and Si substrates, variations in film growth conditions, switch patterns, and measurement parameters, changed the signal shape for the poly-GaAs switches similar to that observed for these materials. We examined the dependence of the poly-GaAs switches on bias voltage and pump pulse energy, the trends are similar to those described in chapter two. Therefore these are not repeated here.

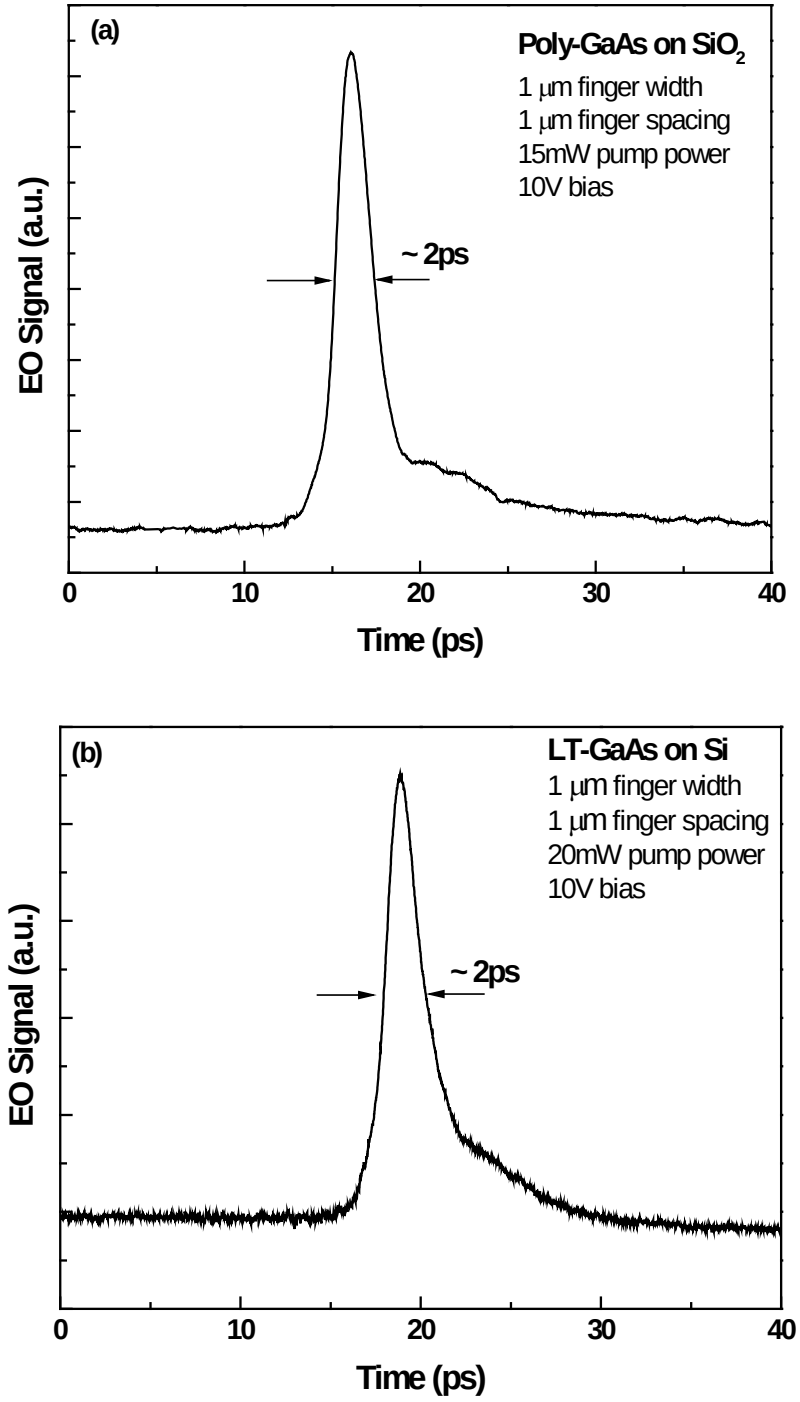

Figure 4.5 A comparison of two typical results of electro-optic sampling measurement of photoconductive switch response. (a) switch made from poly-GaAs film on SiO_2; (b) switch made from LT-GaAs on Si. Depending on different switch pattern, different measurement parameters, the signal shape varies.

4.2.4.2 Responsivity

In Fig. 4.6 we compare the photocurrent vs. optical pump power behavior for switches made from poly-GaAs films grown on SiO_2 with that of the reference switches made from LT-GaAs grown homoepitaxially on GaAs substrates. The responsivity dependence on the switch geometry is also shown in the same plot. In this figure, all the switches have 1 μm finger width and different finger spacings. The reference LT-GaAs on GaAs switches are the ones that were used in the prototype A/D conversion system. The poly-GaAs film was grown at 400 ºC and has a thickness of 1 μm. The measurement was done with 10 V DC bias. The photocurrent values shown are taken from the I-V curves at 10 V.

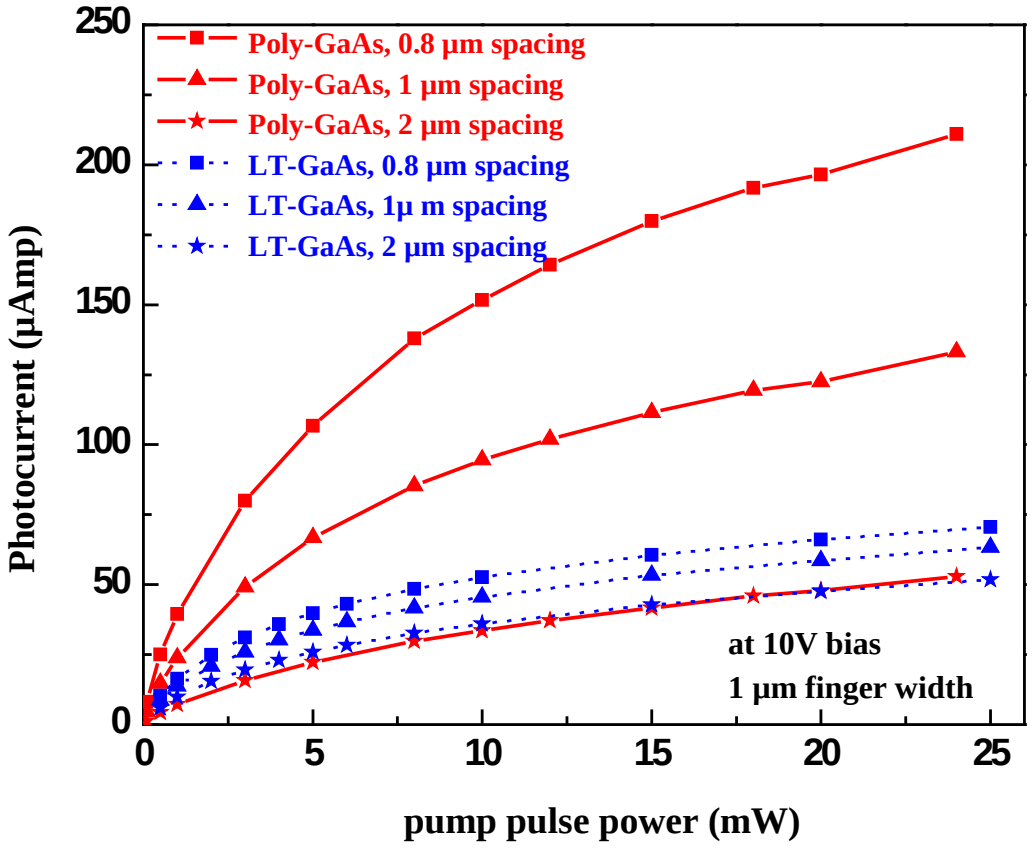

Figure 4.6 Responsivity comparison of switches made from poly-GaAs grown on SiO_2 and the reference LT-GaAs used in the prototype ADC system. The photocurrent dependence on switch finger spacing is also show. The dotted lines are for LT-GaAs reference. The photocurrent values are taken under 10V bias voltage. All switches have 1μm finger width.

The photocurrent vs. pump pulse energy relationships in this figure are similar to those switches made form LT-GaAs on GaAs and LT-GaAs on Si. Surprisingly, for this growth condition, the responsivities of the poly-GaAs switches are much higher than those of the reference LT-GaAs switches. One possible reason is due to the defective nature of the whole LT-GaAs film everywhere, but the good crystal quality within each grain of the poly-GaAs film. The carrier mobility of the LT-GaAs is almost uniformly low. In the case of poly-GaAs films, other than the disordered grain boundary areas, the carriers move with high mobility within each high quality grain. Another explanation can be from a device point of view. In contrast to the LT-GaAs films which are grown on GaAs substrates, the poly-GaAs films are electrically isolated from the underlying Si substrate due to the existence of the dielectric SiO_2 layer. Therefore, all the photo-carriers are generated within a thin high-field poly-GaAs layer. The effective high electric field assists the carrier capture into the switch electrodes.

4.2.4.3 Dark current

Fig. 4.7 compares the dark currents of switches made from three “fast photoconductive materials” we have studied so far: the above poly-GaAs film, the reference LT-GaAs film on GaAs, and the LT-GaAs film on Si shown in chapter 3. The dark current of the reference LT-GaAs on GaAs switch is the lowest and LT-GaAs on Si is the highest. The dark current of poly-GaAs switch is between the two. However, it is still quite low, in the nano-amperes range.

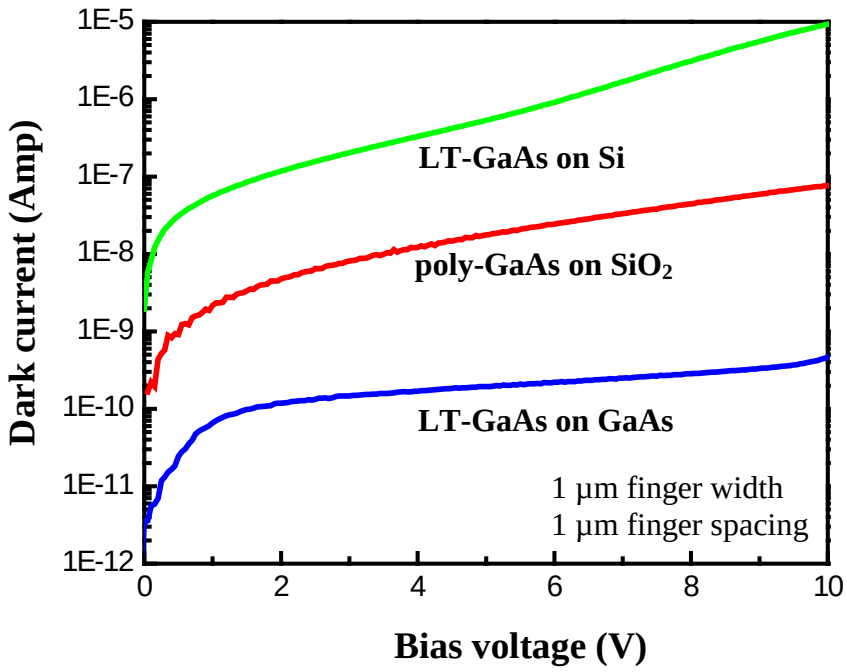

Figure 4.7 Dark current comparison of switches made from different material. All switches have 1 μm finger width and 1 μm finger spacing.

4.2.4.4 Switch frequency response

Extensive EO sampling on various poly-GaAs switches shows that the higher responsivity is not bought by a sacrificing speed. Fig. 4.8 shows the frequency response of a poly-GaAs MSM switch. The poly-GaAs film was grown at 400 ºC. The inset is the temporal response measured by electro-optic sampling for this switch. The MSM switch has 1 μm finger width and 0.8 μm finger spacing. The measurement was done under 1 V bias voltage and with 12.4 pJ optical pump pulse energy. The FWHM of the pulse is ~ 1.65 ps. The 3 dB bandwidth of this switch was found to be 270 GHz by performing a Fourier transform on the temporal waveform. Responsivity is calculated to be 80 mA/W for this testing condition.

In the literature, the most quoted “best” result for high-speed photodetectors has 100 mA/W responsivity and a bandwidth of 375 GHz [8]. In table 4.1 we compared the performance of our poly-GaAs switch with this best quoted switch. The quoted data were obtained from a LT-GaAs MSM photoconductive detector with 0.2 μm finger spacing. The responsivity was calculated with 4 μW pump pulse power.

Our switch has 0.8 μm finger spacing and we used 100 μW pump pulse power because we cannot conveniently further attenuate the pulse energy in our experimental setup.

From previous figures showing the photocurrent vs. switch finger spacing relationships, we have seen that the responsivity increases rapidly with decreasing finger spacing due to higher electrical field. Also from the photocurrent vs. pump power relationships, we know that by decreasing pump power, the calculated responsivity is much higher and the switch turn-off speed is faster. In contrast, our poly-GaAs switch spacing is 4 times larger and we used 25 times more pump pulse energy. Considering the effect of these testing factors, the performance of our poly-GaAs switch is very likely comparable to or higher than the record data. The point is, at this moment, we are not trying to compete for the fastest device. Our goal was to achieve a good enough switch which could be integrated with a finished CMOS chip

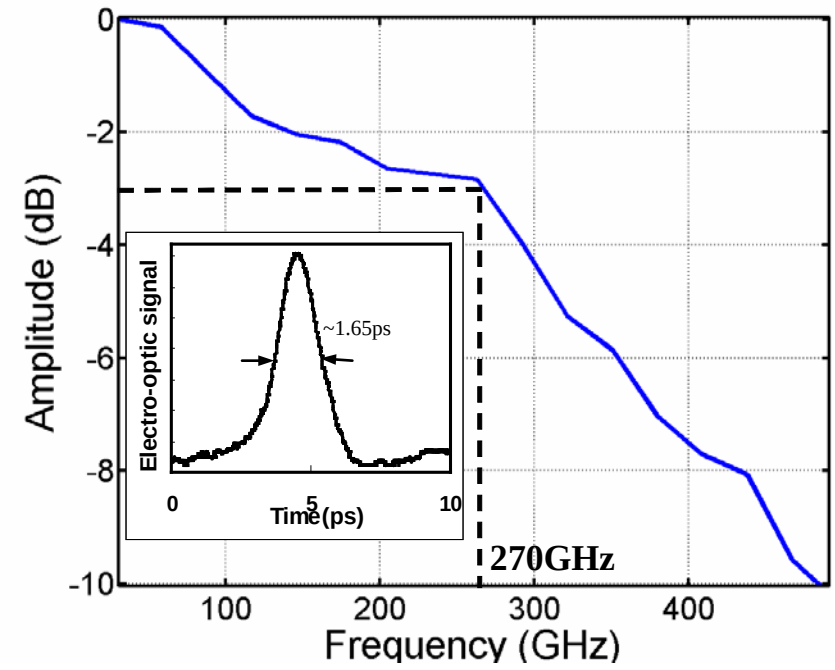

Figure 4.8 Frequency response of a poly-GaAs MSM switch. Poly-GaAs was grown at 400 ºC. The inset is the temporal response measured by electro-optic sampling for this switch. The FWHM is ~ 1.65 ps. The 3dB bandwidth of this switch is 270 GHz by performing a Fourier transform on the temporal waveform. The MSM switch has 1 μm finger width and 0.8 μm finger spacing. The inset response was tested under 1 V bias voltage and 12.4 pJ pulse energy using electro-optic sampling technique. Responsivity is calculated to be 80 mA/W for this switch.

to produce an ultra high-speed ADC. This was achieved. Also, the poly-GaAs material used in this switch was certainly not optimized in this study and there are almost certainly improvements to be made in the device performance.

Table 4.1 Comparison of this work with the best quoted result.

	best quoted result	**this work**
Switch	LT-GaAs MSM	poly-GaAs MSM
Bandwidth	375 GHz	270 GHz
Responsivity	100 mA/W	80 mA/W
Switch spacing	0.2 μm	0.8 μm
Pump power	4 μW	100 μW

4.3 Summary

GaAs films were directly grown at chip-safe temperatures on top of simulated finished-chip surfaces – SiO_2 coated Si substrates. XRD and TEM results show the films have polycrystalline nature and columnar grain structures. Time-resolved electro-optic sampling showed a switch with performance comparable to the best reported results [8]. In summary, the direct growth of polycrystalline GaAs on SiO_2 presents us a very promising and much simpler alternative for the monolithic integration of ultra-fast GaAs photoconductive switches with finished CMOS circuits.

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Chapter 5

On-Chip Fully Monolithic Integration of GaAs MSM Switches with Completely Fabricated Si CMOS Circuits

We monolithically integrated polycrystalline GaAs metal-semiconductor-metal (MSM) photoconductive switches with a completely fabricated Si-CMOS amplifier and obtained a properly functional optical receiver, without altering the Si circuit performance. To our knowledge, this is the first time a fully monolithic on-chip integration has been achieved.

5.1 Introduction

While Si-CMOS circuits with ever higher density and speed dominate most high-performance electronics, III-V semiconductor optoelectronics still dominate high-bandwidth regimes, such as telecommunications, optical communications, military applications, and high-frequency instrumentation. As both technologies quickly advance, more applications could benefit from coupling Si-ICs with III-V optoelectronic components and high-speed circuits. As Si-ICs become ever more powerful and complex, fundamental limitations, such as signal skew, clock jitter, maximum clock frequency, high-speed I/O, pin count, and power dissipation are all identified as significant barriers to continued progress. Optical interconnects have been an attractive candidate to alleviate many of these problems and enable optical transmission of inter- and intra-chip signals. Despite recent progress in silicon optoelectronic devices, the technology is still far behind that of compound semiconductors in its ability to produce useful, integrated optical links. There are many applications where integration of compound semiconductor devices with Si circuits could dramatically improve performance and functionality.

In chapter two we combined high-speed LT-GaAs switches with a CMOS ADC chip using a flip-chip bonding hybrid integration technique and successfully demonstrated a high bandwidth, two-channel prototype ADC system with less than 80 fs aperture uncertainty [1, 2]. Monolithic integration is generally considered advantageous in order to minimize circuit parasitics. This chapter describes our study on monolithic integration of GaAs MSM detectors on completely fabricated Si CMOS circuits, which is an important alternate integration technique in our development of high-speed ADC system [3].

As we mentioned in the previous chapters, the common approach for monolithic integration is to grow the compound semiconductor device layers onto the Si CMOS wafer prior to final level metallization and then finish the metallization after the growth of the compound devices. This causes cross-contamination concerns and creates fabrication complications due to the mismatch between the different tool sets

used for Si circuits and GaAs devices. In prior work of monolithic integration of GaAs on Si, the final level of metallization was completed after growing the GaAs films at high temperatures. One severe problem in achieving the integration was the use of different lithography tools for GaAs and Si devices, and hence stitching differences between the two sets of tools made circuit yield suffer and the performance was seriously compromised [4]. Since our MSM switches with short switching aperture time are achieved by shortening carrier lifetime utilizing engineered material defects, we have explored the possibility of directly growing GaAs films at low temperatures on top of **completely fabricated** Si CMOS chips to enable on-chip, fully-monolithic integration. With this simplified approach, all the problems described above are avoided.

The most critical issue in our approach is to prevent any modification of the characteristics of the underlying Si circuits from the GaAs film growth and processing steps. Novel low-k dielectric materials have been introduced and are becoming routine for back-end-of-line (BEOL) applications in modern Si ICs. In front-end-of-line (FEOL) steps, the scaling of the technology nodes and the adoption of new materials also imposes strict requirements on the thermal budgets. These all create severe limitations in the process temperatures for subsequent deposition and treatment steps. This restriction is strongly influenced by the choice of the technology nodes, low-k films and different processing schemes. In general, a safe upper temperature limit is around 400 ºC and the trend is to go even lower.

In previous chapters we investigated fast photoconductive materials on Si and SiO_2 as alternate candidates to that of LT-GaAs on GaAs material. The MSM switches made from LT-GaAs on Si showed ~ 2 ps switching time and the responsivity was comparable to its counterpart on a GaAs substrate. However, modern ICs usually have six or more metal layers. In order to grow GaAs on the Si surface, deep etching through these interconnect layers is required to expose the Si surface. This creates deep trenches and causes metal step coverage problems. To avoid these problems and simplify the processing, we boldly studied direct growth of GaAs on SiO_2 or Si_3N_4 at low temperatures. At around 400 ºC, growing GaAs on amorphous dielectrics results

in polycrystalline GaAs. The grain boundaries act as trapping and recombination centers, resulting in short carrier life time, which have a similar effect to the point defects in LT-GaAs that we previously used to achieve high-speed switching [5, 6]. Using 1 μm thick poly-GaAs films grown on SiO_2 at 400 ºC, we made MSM switches with 1 μm finger width and 0.8 μm finger spacing. FWHM switching window of ~ 1.65 ps was obtained under illumination of a 12.4 pJ (100 μW) Ti/sapphire mode-locked laser short pulse and with 1 V DC bias voltage. A Fourier transform of the measured pulse response indicated a ~ 270 GHz 3-dB bandwidth. The responsivity was as high as 80 mA/W under the above testing conditions.

In this chapter, we demonstrate the realization of a real on-chip monolithic integration using the poly-GaAs material described above and in chapter 4.

5.2 Experiments and results

5.2.1 Completely fabricated Si amplifier IC chip

It would have been ideal if we could have used the same ADC chips used in our prototype system to realize the on-chip monolithic integration and to compare their performance. Unfortunately, all the chips were consumed in the hybrid integration study and making new chips was going to take an enormous effort and an extremely long delay. Therefore, a suitable high-speed ADC CMOS chip was not available to demonstrate our on-chip integration for the ultrahigh-speed ADC system. For a proof-of-concept demonstration, we used a moderate speed (300 MHz) optical receiver Si IC chip that was available [7]. The chip was fabricated by National Semiconductor Inc. with its 0.24 μm CMOS technology. As long as we could achieve a fully functional integrated system without degrading the Si circuit performance, this would be sufficient to prove the validity of this integration approach.

The chip was originally designed to be flip-chip bonded with a pair of detectors for another research project. Fig. 5.1 (a) is the circuit schematic of the receiver chip. Without the MSM switches (inside the dotted lines), it is a two-stage amplifier with a buffered input stage and a differential gain stage. The pair of MSM switches (shown outside of the dotted line boundary) were to be integrated at the input nodes of this finished CMOS chip. Fig. 5.1 (b) is a micrograph picture of the original completely fabricated CMOS chip before integration. It shows the surface topology. The receiver was fabricated at National Semiconductor Inc. on an 8" wafer and diced into approximately 2 mm by 2 mm size die. It has six layers of metallization and is passivated with SiO_2/Si_3N_4 dielectric stacks. Fig. 5.1 (c) illustrates the cross-sectional structure of the chip. The topmost metal layer is Al + 0.5% Cu. The regularly patterned white squares shown in the picture are arrays of approximately 20 μm square and 2 μm deep glass cuts that were made originally for flip-chip bonding purpose. The white color we see in the picture is the color of the final metal layer because the passivation films are transparent. Using this chip, we planned to grow a poly-GaAs film on top, make the MSM switches on GaAs, and then connect MSM switches to the underlying Si circuits through the glass cut areas.

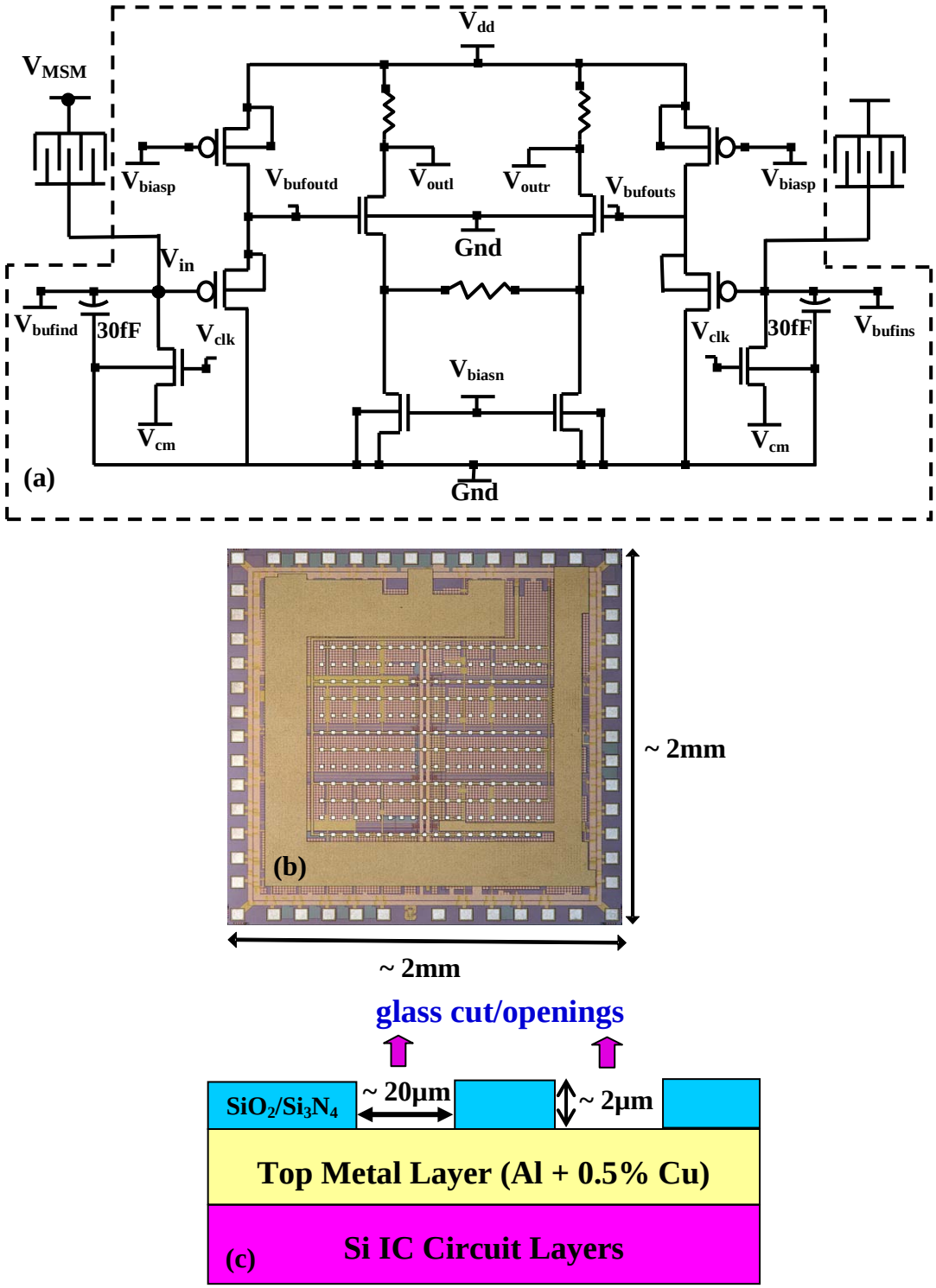


Figure 5.1 (a) Inside the dotted lines is the circuit schematic of the CMOS receiver chip. The differential pair of the polycrystalline GaAs MSM switches is integrated at the receiver input nodes, as shown outside of the dotted lines. (b) Picture of the completely fabricated CMOS receiver chip, before integration. Size is ~ 2 × 2 mm^2. (c) Cross-sectional illustration of the chip structure.

5.2.2 Chip cleaning and GaAs film growth

Surface cleanliness is crucial for high quality GaAs epitaxial growth during GaAs/Si monolithic integration. Typically, the cleaning/native oxide desoprtion of the Si surface is done at temperatures higher than 600ºC, which is not acceptable for a finished chip. Since we are targeting high-speed applications and controllable defects are required to shorten the carrier lifetime, the temperature requirement is relaxed to some extent.

In our particular situation, the fact that the chip was already diced into small pieces (2mm × 2mm) created a considerable level of complexity for mounting the sample in the MBE system for GaAs film growth and subsequent processing. This was purely due to handling difficulties from the small chip size. In order to grow GaAs films on such small chips, we first had to mount the chip onto a 3” carrier Si wafer. This was done by placing the chip on a hot plate in the cleanroom and applying a minimal amount of MBE-grade indium on the back of the chip to solder the chip onto the clean Si carrier wafer. Due to the small size of the chip and the large surface tension of In, special attention had to be given to avoid In migration onto the edge and the top surface of the Si chip which would short the circuits. If the integration was done for a full wafer, extra efforts in handling and processing due to the small chip size would not have been required.

Chips were carefully cleaned by using multiple solvents: PRS1000, Shipley microposit remover 1165, PRX127, acetone, methanol and isopropanol, in this order. PRS1000 is an organic solution used as a photoresist stripper where “PRS” stands for Positive Resist Stripper. It is used as a metal cleaning agent to remove organics and gross surface contaminants on metallized wafers. PRX127 cleans resist stripper, but does not attack metals provided it is anhydrous. Other solvents mentioned above are all generally used in semiconductor wafer cleaning to obtain particle-free and residue-free surfaces.

After cleaning, the chip (on the carrier 3” Si wafer) was loaded into the loadlock chamber of our MBE system and baked at 250 ºC for 30 minutes to remove moisture and gases before it was moved to the transfer tube.

GaAs films were grown in the same solid source Varian Gen II MBE system described in previous chapters. Gallium flux was supplied by a thermal effusion cell and dimeric arsenic (As_2) was provided through a valved thermal cracker. A ~ 1 μm thick layer of undoped GaAs was grown at 400 ºC substrate temperature (thermal couple reading) with an As_2/Ga beam-equivalent-pressure (BEP) ratio of 6. The GaAs growth was initiated with 10 migration-enhanced-epitaxy (MEE) cycles and the wafer rotated at 10 rpm throughout the growth. Growing GaAs on dielectric layers and at this low temperature rendered the film polycrystalline as we have shown in chapter 4. Because MBE growth is not selective, the poly-GaAs film covers the entire chip surface, including the glass cut areas. The properties of the poly-GaAs film grown under this condition were described in chapter 4.

5.2.3 Integration Process

If we discount the extra difficulties caused by the very small size of the diced chip, the process is quite simple, which is exactly the beauty of this approach.

Fig 5.2 illustrates the detailed integration process steps. The highest temperature step was the poly-GaAs film growth in MBE chamber, 400 ºC, which is safe for almost all modern IC fabrication processes, including circuits using Al interconnects and low-k dielectric materials.

Step 0 shows the starting chip, with SiO_2/Si_3N_4 dielectric stack passivating the top surface, and arrays of glass cuts made to expose the top metal layer for later contact. The top metal is aluminum with small amount of Cu added to prevent the electrical migration.

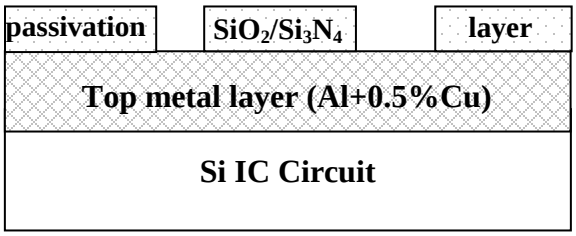
In the first step, the chip was cleaned using the methods described above and then loaded into MBE chamber. Due to the non-selective nature of MEB growth, a 1 μm thick poly-GaAs film was then grown at 400 ºC over the entire chip surface, including the glass cut areas.

Next in step two, the MSM photoconductive switches were patterned on the top poly-GaAs film. Eight switches (four differential pairs) with an interdigitated pattern were fabricated by depositing titanium/gold contact metal on the poly-GaAs layer through a standard lift-off process. To achieve higher responsivity, we decided to use smaller finger spacing compared with our previously studied switch geometry. E-beam lithography was used to define the MSM pattern for the switches with 0.8 μm and 0.6 μm finger spacings and ~ 15 μm finger width. Further reducing the finger spacing is desired for high-speed switching performance, however, this requires more effort in developing the e-beam litho process. For our test of concept purpose, that can be reserved for a future study.

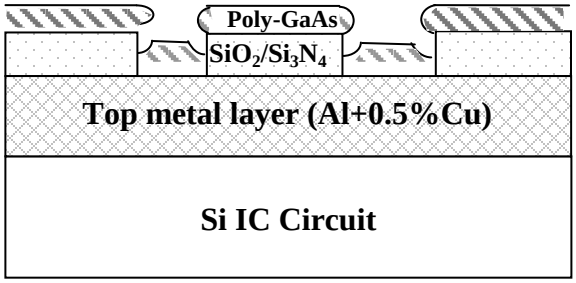
In order to connect the GaAs switches with the Si circuits, the poly-GaAs grown inside the glass cut area had to be removed to expose the top metal layer of the Si chip. Step three shows this procedure. With photoresist protecting the already patterned switch areas, the unwanted poly-GaAs in the glass cuts was wet etched in citric acid, which is highly selective between GaAs and Al so that GaAs can be completely removed without hurting the Al contacts.

Step four is critical. Considering the complexity of the metal deposition for a completed circuit and the modest technology available in Stanford processing lab, the final metal contact was applied using angled evaporation from both sides to ensure good step coverage because there were many steps on the surface at this point. We first deposited 150 Å Cr + 850 Å Cu + 500 Å Au vertically to make the initial contact flat. Au is the dominant metallization on GaAs circuits. Cr and Cu were used to avoid the Au_2Al “purple plague” intermetallic compounds [8]. Then in the first oblique deposition, 200 Å Cr + 1000 Å Au were evaporated at a 60º angle from one side. This is followed by a second evaporation of the same thickness layers at the same angle, but from the opposite side. This kind of multi-direction deposition insured conformal coverage of the contact metal.

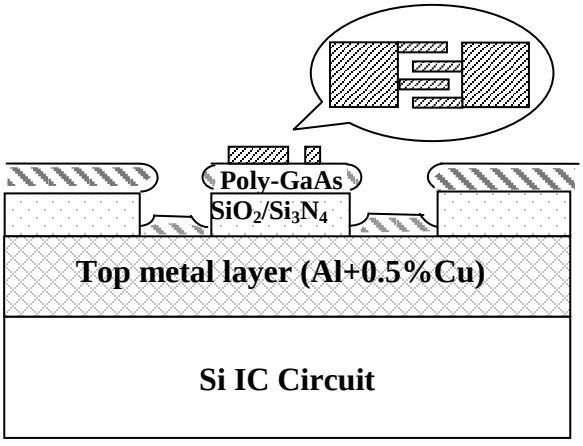
Step 0. Starting chip



Step 1. Poly-GaAs film growth



Step 2. MSM patterning



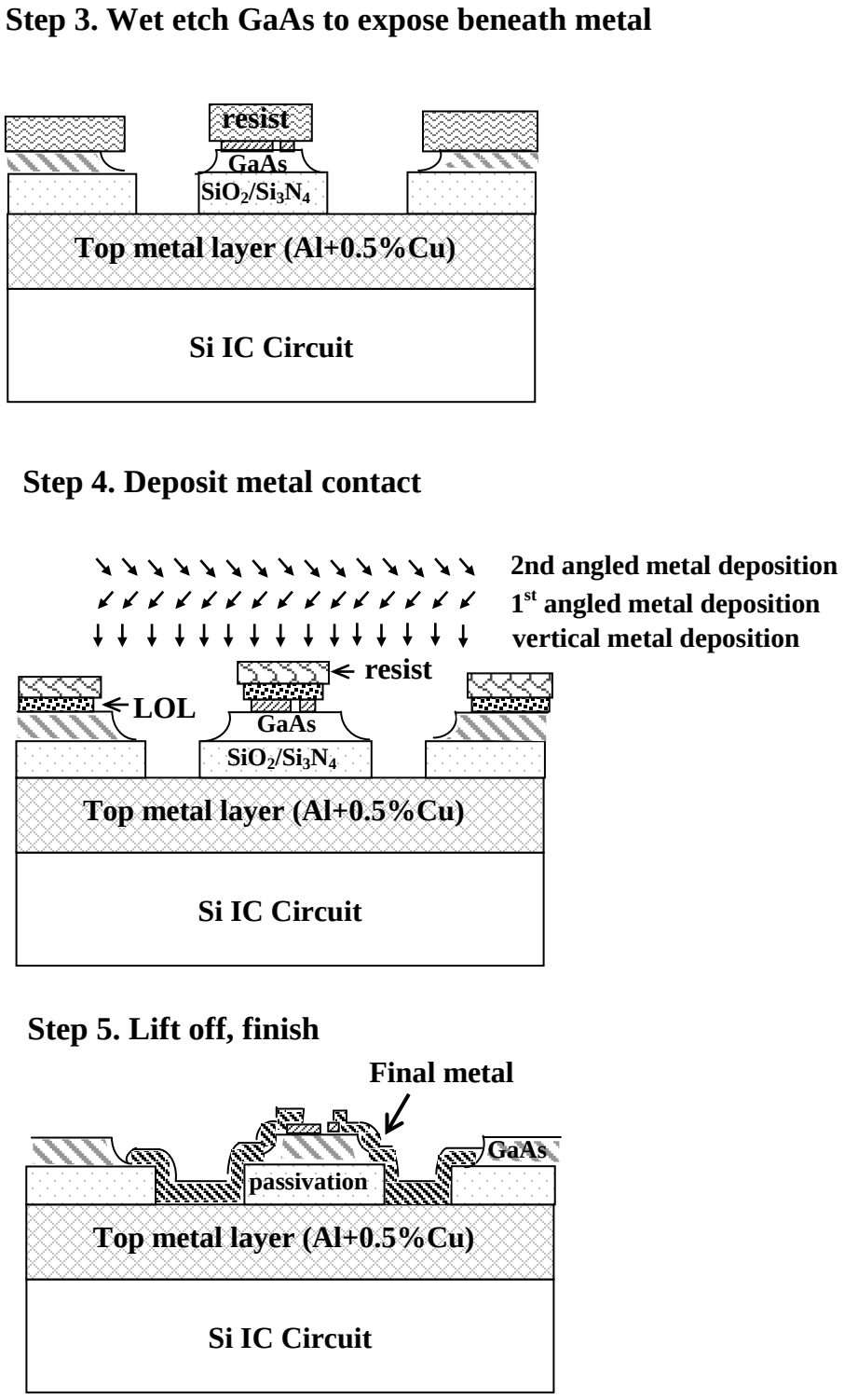


Figure 5.2 Monolithic integration process to fabricate GaAs MSM switches directly onto completely finished Si amplifier chip and achieve an integrated optical receiver system. The schematic is not drawn to scale. Each step has self-explanatory sub-titles.

Metal deposition from different angles potentially makes the lift-off process very difficult, if not impossible. We used a LOL2000 dual layer resist lift-off process [9] to get around the possible non-lifting problem. LOL2000 is a non-UV-sensitive liquid polymer, which can be etched away with most standard developers (weak bases). LOL2000 was first spun on the wafer and baked, then standard photoresist was spun on and soft-baked. The photoresist was exposed and developed in the normal manner. During development, the standard developer cleared the exposed photoresist, and also etched away some LOL2000, depending on how long it was in contact with the developer. This leads to undercutting of the photoresist and this overhang prevents LOL sidewall deposition of metal films in the angled evaporation and created an air gap for the lift-off to be followed. The resist was lifted-off using microposit 1165 and acetone. Because the overhang profile is caused by undercutting the resist, care must be taken to avoid completely undercutting (and therefore lifting off) the very narrow geometries of the MSM fingers.

After lift-off (step five), the integration was complete. MSM switches were now connected to the underlying Si circuits through the glass cut areas and an integrated optical receiver system was obtained.

5.2.4 Monolithically Integrated Optical Receiver

5.2.4.1 Integrated Receiver

Fig. 5.3(a) is a micrograph of the fully integrated optical receiver achieved through the integration method described above. The gray areas are where GaAs film was grown. Four pairs of differential poly-GaAs switches are shown in the picture that connect to the input nodes of the Si receiver circuit.

Fig. 5.3(b) is a zoomed-in picture showing the details of one such pair. The large rectangular metal pads connect the MSM switches with the underlying Si amplifier circuit.

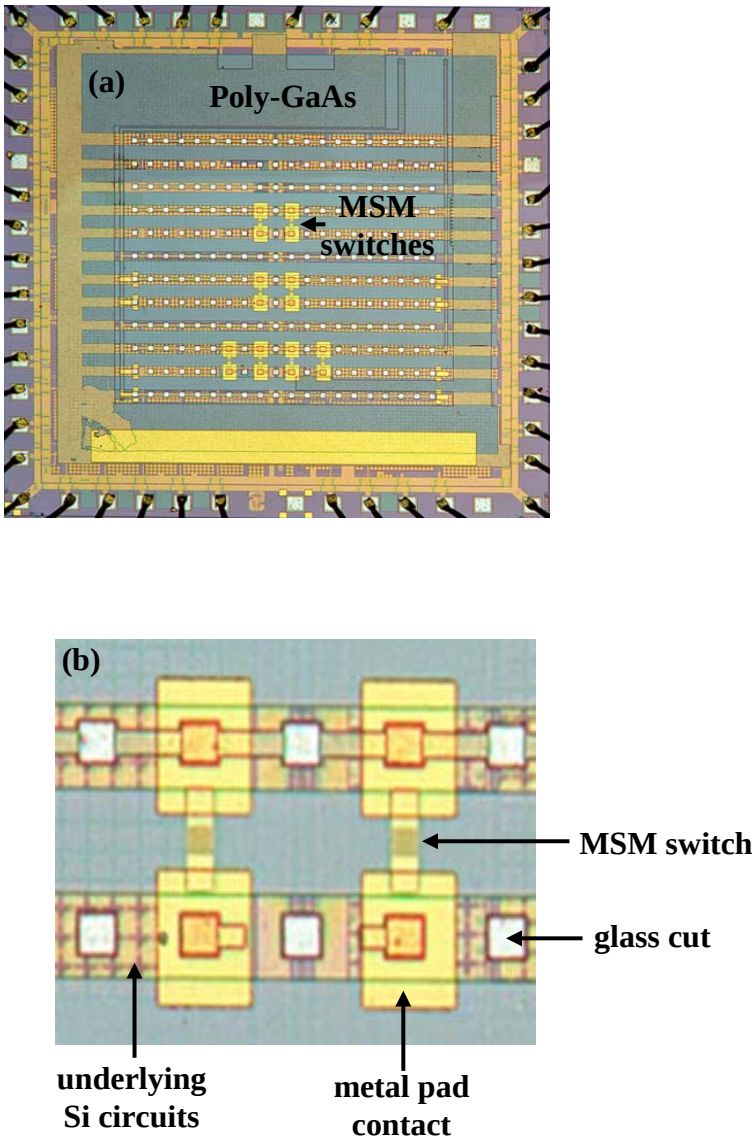


Figure 5.3 (a) Micrograph of the optical receiver after integration. Gray areas are poly-GaAs film. Eight golden devices are MSM switches. (b) Enlarged picture shows the details of a pair of MSM switches. The large rectangular metal pads connect the MSM switches with the underlying Si amplifier circuit.

5.2.4.2 Optical Receiver Testing

5.2.4.2.1. Transfer function

In chapter four, we characterized the MSM switches made from 1 μm thick poly-GaAs film grown on SiO_2 under the same conditions and achieved 270 GHz 3 dB switching bandwidth and 80 mA/W responsivity. Since the optical receiver chip was not designed for high-speed applications, we were not able to directly characterize the high-speed switching performance for the integrated system. Instead, to prove the soundness of our monolithic integration approach, we tested the DC characteristics of the integrated receiver with the MSM switches to verify if it was functional as designed.

Fig. 5.4 shows the DC characteristics of the optical receiver. With a constant continuous-wave (CW) laser power triggering the switch, the MSM bias voltage (V_{MSM}) was varied to indirectly change the input node voltage (V_{in}) of the receiver (see Fig.5.4(b)). The corresponding output voltage (V_{out}) was recorded to obtain the DC transfer function. Changing the laser power, a different photocurrent and therefore another transfer function was generated. The MSM switch is clearly photo-sensitive to different optical power. In this experiment, we indirectly measured the transfer function of the integrated receiver and demonstrated that after integration, we achieved a properly functioning optical receiver with typical input-output characteristics.

5.2.4.2.2. Step response

It is very important that the integration process does not affect the original Si circuit performance. We fed the amplifier with two differential electrical signals, and measured the output step response in order to compare the AC characteristics of the amplifier (without MSM switches) before and after the integration. Fig. 5.5 shows the testing result for the original Si receiver (a) and for a receiver after the on-chip MSM integration is completed (b). This confirms that the step response is not changed at all.

The rise times of the amplifier before and after integration are both ~ 11 ns (11 ns and 11.2 ns). The 0.2 ns difference is within chip to chip variation. The amplifier gain is

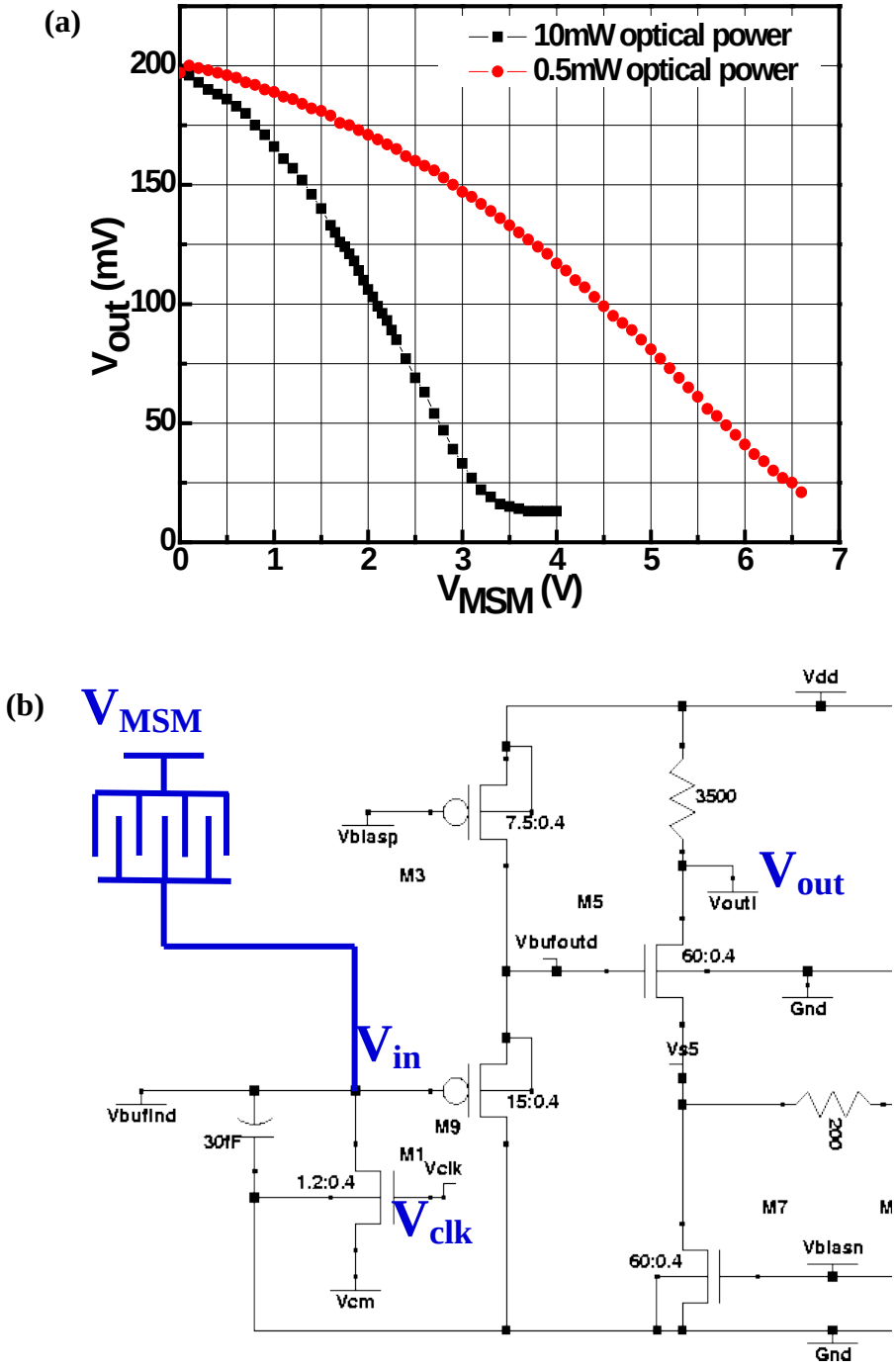


Figure 5.4 (a) Input-output characteristics of the integrated optical receiver with MSM switches. CW laser wavelength λ = 850 nm. (b) Schematics showing where the input and output voltage were taken.

measured to be 3 for both chips before and after integration. In addition, the circuit biasing points stay exactly the same. The result that the bandwidth, gain, and biasing points of the Si amplifier stay the same after the GaAs integration clearly proves that our approach is completely safe for a finished Si CMOS chip with metallization.

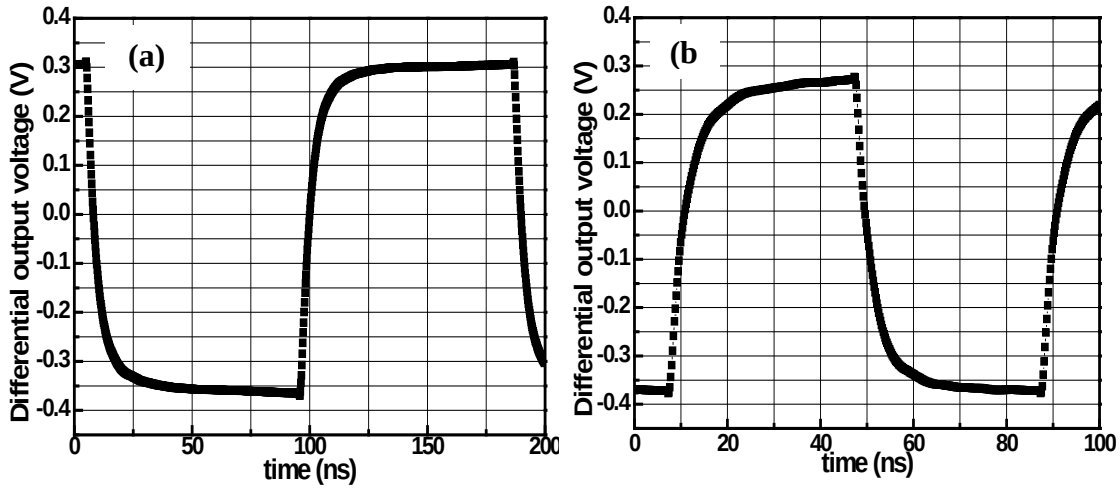


Figure 5.5 Step response of the Si amplifier before (a) and after (b) the GaAs MSM switch integration. The 10% to 90% rise time in (a) is 11 ns and in (b) is 11.2 ns. The amplifier gain is both 3. Circuit biasing conditions for testing are: V_{dd} = 2.5 V; Vclk = 0.66 V; Vcm = 0 V; Vbias,n = 0.79 V; Vbias,p = 1.9 V (refer to Fig. 5.1 circuit schematics for voltage positions).

5.3 Integration methods comparison

We have described several different integration approaches for combining GaAs devices and Si CMOS circuits. There are two major categories: hybrid integration (such as the flip-chip bonding method we used in chapter two) and monolithic integration. For monolithic integration, we explicitly mean that the GaAs devices are grown and processed on the Si wafer before the Si IC chip is finished fabrication. Our new approach successfully integrated GaAs MSM photoconductive

switches to a completely finished Si chip. Table 5.1 compares the advantages and the shortcomings of each of these methods.

Table 5.1 Comparison of different GaAs and Si integration methods.

	Hybrid Integration	**Monolithic Integration**	
	Flip-chip bonding	GaAs **before** metallization	GaAs **after** metallization
Minimal parasitics	no	**yes**	**yes**
Process complexity	medium	most complicated	**simple, minimal perturbation**
Substrate cost	high	**no cost**	**no cost**
Vicinal Si substrate	**no**	yes	**no**
Alignment with Si-IC	poor	**good**	**good**
Compact integration	no	**yes**	**yes**
Large scale integration	difficult	**easy**	**easy**
Applications needing high crystal quality	**yes**	maybe	no
Film uniformity	**good**	**good**	maybe poor

Compared to hybrid integration, the monolithic approaches have minimal parasitics. Within the monolithic integration category, comparing to the common approach of growing GaAs before metallization, the most significant virtue of our new approach is its simplicity and minimum process complexity. In our approach, no bulk GaAs wafer is needed and there is no requirement on the Si substrate orientation. Our new approach can achieve large scale, compact integration, with better alignment to Si circuits. Due to the polycrystalline nature of the GaAs film used in the new approach, the material property is not as uniform as single crystalline materials and its applications are limited to areas where relatively defect dominated materials are favored.

5.4 Summary

We have monolithically integrated polycrystalline GaAs MSM switches with a **completely fabricated** CMOS amplifier IC chip and obtained a properly functional optical receiver without modifying the underlying Si circuit performance. The GaAs film growth, integration process and the electrical and optical testing of the integrated system have been described in detail. The beauty of this integration approach is its simplicity, minimum fabrication disturbance, limited entirely to tail-end Si processing, and greater applicability for much broader areas, such as optoelectronic interconnects for very-high-density, very-high-speed CMOS circuits.

In addition to minimizing parasitics, in contrast to hybrid integration methods such as flip-chip bonding, the monolithic integration avoids the use of bulk GaAs and therefore substrate removal. High cost GaAs material is saved, and it is much more suitable for mass-production.

For suitable niche applications, our approach can achieve very large scale compact integration, with much better alignment with Si circuits. Another benefit is that, for optoelectronic systems, by covering the chip surface with a layer of GaAs, the potential of scattered light affecting the CMOS circuit is greatly reduced.

Previous studies reported integration of GaAs devices with partially-fabricated Si circuits [10, 11]. The process sequence for this is described in Appendix. To our knowledge, this is the first time a fully monolithic on-chip integration has been successfully achieved.

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Chapter 6

Summary and Suggestions for Future Research

6.1 Summary

In summary, we studied three material systems targeting a high-speed photoconductive switch application. First, for LT-GaAs films grown on GaAs substrates, we significantly improved the MSM switch performance by systematic optimization of LT-film growth and annealing conditions according to design-of-experiments (DOE) principles. The switches made with our optimized process conditions demonstrated high frequency sampling capability and were successfully used to implement a two-channel prototype high bandwidth photonic A/D conversion system.

To enable monolithic integration of GaAs devices with finished Si IC chips, we studied low temperature growth of GaAs films, both on Si substrates and on SiO_2 films. We performed all the experiments, including film growth, annealing and device processing, at temperatures safe for completed IC chips with final metallization and

passivation layers. Testing results showed that the switch performance was comparable to or exceeded the reference LT-GaAs switches made on GaAs wafers which were used to fabricate the prototype ADC system.

As a final proof of concept, we successfully integrated GaAs switches monolithically on a completely fabricated CMOS amplifier and achieved a functional optical receiver without modifying the Si circuit performance. The beauty of this approach is its simplicity, minimum fabrication disturbance and greater applicability into other areas. We believe this to be the first successful demonstration of monolithic integration of GaAs devices on a fully completed Si chip, and most importantly, demonstrating fully functional and un-degraded performance.

6.2 Suggestions for future research

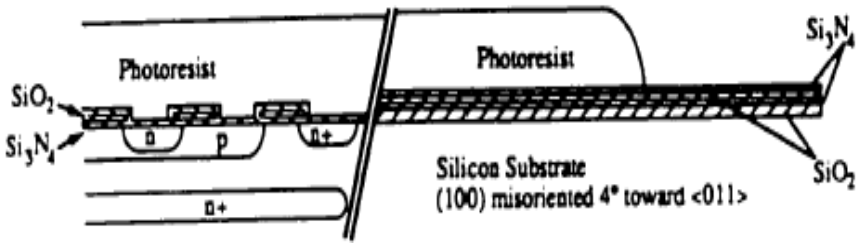
The responsivity of MSM photodetectors with the simple design used in this thesis has some improvable shortcomings. First, some electron-hole pairs (the amount depends on the excitation light wavelength) recombine at the GaAs surface, before reaching the electrodes. Second, a significant amount of (~ 30%) incident phonons are reflected back at the surface (GaAs/air interface). If another carefully designed layer is deposited on top of the LT-GaAs layer, these two problems can be solved to a significant extent. For example, if a non-absorbing AlGaAs layer is deposited on top of the LT-GaAs layer to interface with the air, by choosing appropriate aluminum fraction, it can serve both as an effective antireflection and surface passivation layer to alleviate the loss of absorbed photo-energy and surface recombination. Another improvement would be to provide AlGaAs layers on both sides of the GaAs photoconductive layer to confine all of the carriers nearer to the electrode fingers. Using e-beam nano-imprint lithography to fabricate smaller structures is also expected to improve the overall performance.

APPENDIX:

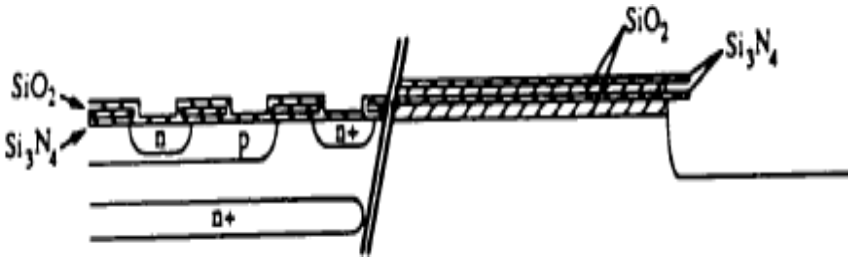
An example of the traditional monolithic integration process of GaAs on Si circuit

As a reference, we copy the process steps of a previous student's work to monolithically integrate GaAs with Si [1]. In this work, GaAs MSM photodetectors were to be integrated to a Si bipolar transistor. The first level metal contacts were already defined. Interested parties are referred to ref. [1] for details. This process is shown below in eight steps. However, each step contains multiple process procedures. The detailed run sheet of this process has 17 steps and 9 pages of description. Compared to this process, our new approach is extremely simple.

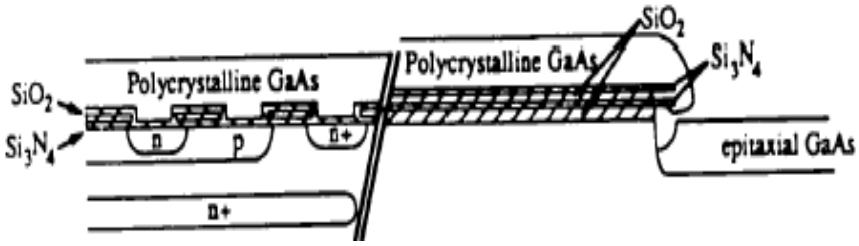
Step 1. Etch contacts, deposit Nitride, define GaAs/Si regions.



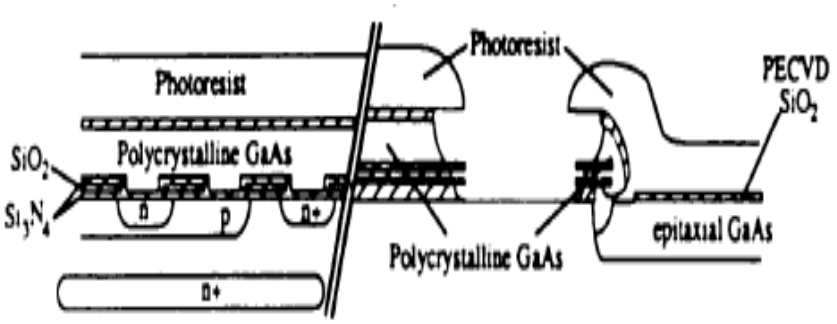
Step 2. Etch nitride, etch and undercut oxide, etch Si using RIE.



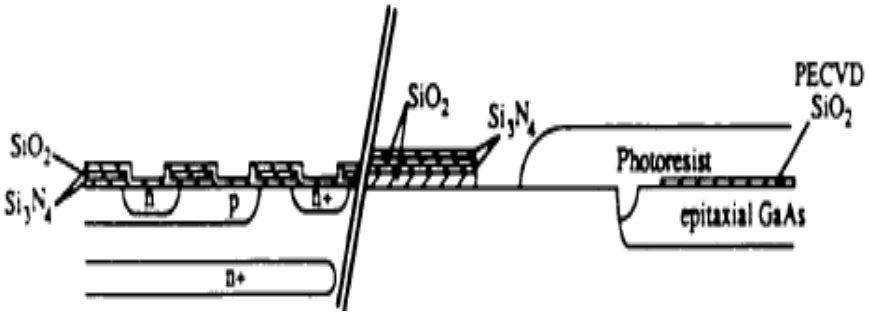
Step 3. Grow GaAs/Si using MBE



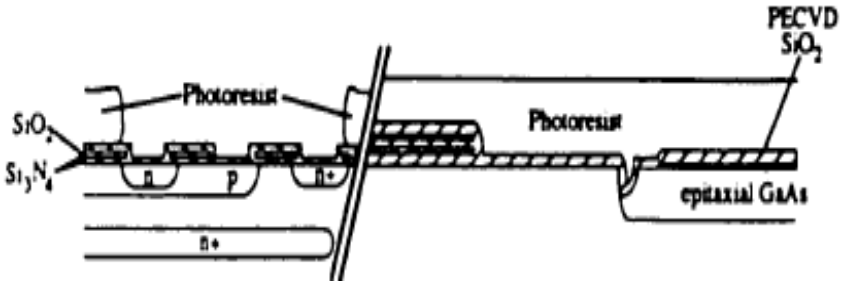
Step 4. Deposit PECVE oxide, pattern etch PECVE oxide, poly-GaAs, nitride, undercut oxide to liftoff poly-GaAs.



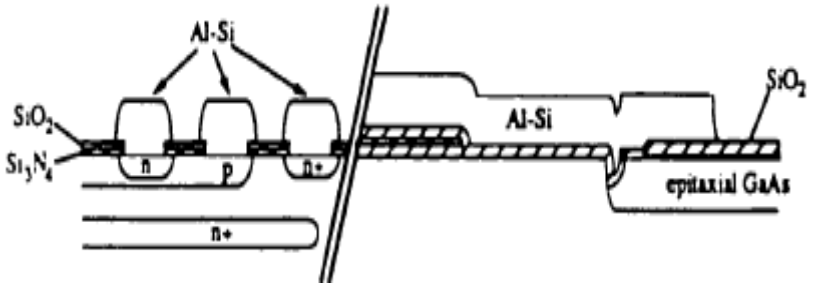
Step 5. Remove nitride overhand, protect epitaxial GaAs with photoresist, etch PECVD oxide and poly-GaAs.



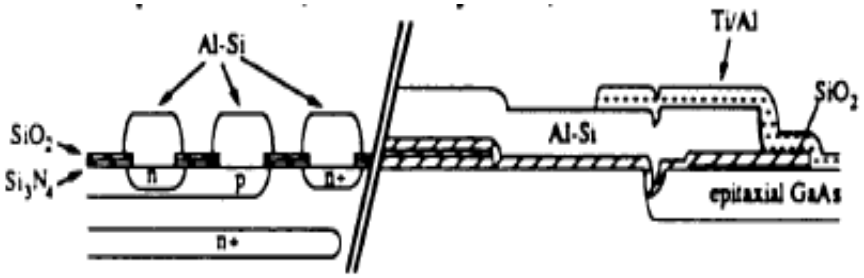
Step 6. Deposit PECVD oxide, define oversize contact areas, etch PECVD oxide.



Step 7. Selectively etch nitride, deposit and pattern Al-Si.



Step 8. Open contacts to the GaAs, evaporate Ti/Al (patterned by liftoff)



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