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High electron mobility transistors built on MBE grown InAlAs/InGaAs/InP heterostructures

Pao, Yi-Ching, Ph.D.

Stanford University, 1991

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HIGH ELECTRON MOBILITY TRANSISTORS BUILT ON MBE GROWN

InAlAs/InGaAs/InP HETEROSTRUCTURES

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

By

Yi-Ching Pao

December 1990
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I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

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Approved for the University Committee on Graduate Studies:

[Signature]

Dean of Graduate Studies
To my father
Abstract

Molecular Beam Epitaxial (MBE) growth of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ high electron mobility transistor (HEMT) structures was studied and optimized under various growth conditions. The ability to grow consistent, lattice matched epitaxial layers has led to improved two dimensional electron gas (2DEG) properties. However, the high frequency performance of an InP based HEMT depends not only upon the epitaxial material quality, but the HEMT surface structural design as well.

The fundamental charge control model for the idealized HEMT structure has failed to reveal the physical origin of the high output conductance observed in short channel $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HEMTs. The investigation of different HEMT structural designs, supported by analytical and experimental results, has achieved better understanding of the HEMT operation. This study has demonstrated, that the modulation of channel peak electric field through various surface layer conductance designs, is a crucial consideration in pursuing optimum device performance. Through the use of two-dimensional device simulation, the low conductance drain (LCD) design approach has been developed to improve the 2DEG carrier confinement, thus obtaining better HEMT output characteristics. The model of premature current saturation (PCS) has also been proposed for the first time, based on real-space transfer of hot electrons, to explain qualitatively the physical phenomenon of high output conductance observed in short channel $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HEMTs. This development has led to the achievement of various state-of-the-art device and circuit results, and has significantly advanced the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ on InP HEMT technology for ultra high frequency applications.
Acknowledgements

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monolithic integrated circuit designs. In particular, Mr. Cliff Nishimoto for his experienced knowledge in device processing; Dr. Cindy Yuen, Dr. Reza Majidi-Ahy and Dr. Majid Riaziat for their excellent works in MMIC designs and characterizations; and Dr. Chris Webbs, and Dr. Steve Bandy for useful discussions.

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<tr>
<td>HEMT</td>
<td>High-Electron Mobility Transistor</td>
</tr>
<tr>
<td>MESFET</td>
<td>Metal-Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>MODFET</td>
<td>Modulation-Doped Field Effect Transistor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide-Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>HBT</td>
<td>Heterojunction Bipolar Transistor</td>
</tr>
<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>2DEG</td>
<td>Two-Dimensional Electron Gas</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
</tr>
<tr>
<td>RHEED</td>
<td>Reflection High Energy Electron Diffraction</td>
</tr>
<tr>
<td>AlGaAs</td>
<td>Aluminum Gallium Arsenide</td>
</tr>
<tr>
<td>GaAs</td>
<td>Gallium Arsenide</td>
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<td>InGaAs</td>
<td>Indium Gallium Arsenide</td>
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<tr>
<td>InAlAs</td>
<td>Indium Aluminum Arsenide</td>
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<tr>
<td>InP</td>
<td>Indium Phosphide</td>
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<tr>
<td>AlSb</td>
<td>Aluminum Antimonide</td>
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<tr>
<td>GaSb</td>
<td>Gallium Antimonide</td>
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<tr>
<td>InAs</td>
<td>Indium Arsenide</td>
</tr>
<tr>
<td>PMMA</td>
<td>PolyMethylMethAcrylate</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscopy</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma Enhanced Chemical Vapor Deposition</td>
</tr>
<tr>
<td>LTB</td>
<td>Low Temperature Buffer</td>
</tr>
<tr>
<td>LCD</td>
<td>Low Conductance Drain</td>
</tr>
<tr>
<td>PCS</td>
<td>Premature Current Saturation</td>
</tr>
<tr>
<td>MSG</td>
<td>Maximum Stable Gain</td>
</tr>
<tr>
<td>MAG</td>
<td>Maximum Available Gain</td>
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<tr>
<td>MMIC</td>
<td>Microwave (Millimeter)-Wave Monolithic Integrated Circuit</td>
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Chapter 1

Introduction

1.1 Background

Since its first invention in 1978 [1] and demonstration in 1980 [2], the High Electron Mobility Transistor (HEMT), also known as MOdulation-Doped Field Effect Transistor (MODFET), has been developed into a key component in modern military and communication electronics. Over the past decade, intensive work on AlGaAs/GaAs based HEMTs has demonstrated its speed and noise superiority over competing high speed devices, such as the GaAs MEtal Semiconductor Field Effect Transistor (MESFET) and AlGaAs/GaAs Heterojunction Bipolar Transistor (HBT). As the name HEMT implies, the principle characteristic upon which the device is based, is the formation of a quasi-two-dimensional electron gas (2DEG) through the presence of heterojunction confinement. Since the electron in the 2DEG are physically separated from their host ionized impurities by the heterojunction band gap discontinuity, the electrons suffer less scattering in drifting in the transverse direction, hence achieving a higher electron mobility. Because the electrons move faster in an undoped channel region than a conventional MESFET channel, for which the channel is doped moderately ($10^{17}$ cm$^{-3}$), higher switching speed and higher current gain cut-off frequency are expected for HEMT devices. Also the noise performance is better with HEMT due to less ionized impurity scattering with the conducting electrons.

During the past decade, rapid advances in the development of microwave and millimeter wave HEMTs may be broadly separated into two major categories. The first is exploitation of advanced device fabrication techniques to achieve quasi-ballistic effects in submicrometer device structures. This effort emphasizes, among others, better contact metallization, ultra short gate geometry, advanced gate profiles (e.g.,
mushroom gate) and self aligned gate structures. The second category is exploitation of heterojunction structures, principally in optimizing the HEMT material and heterostructures for higher 2DEG sheet charge, higher electron mobility and saturation velocity. These materials and structure investigations include: atomic planar doping (i.e., delta-doping) HEMT [3], lattice mismatched pseudomorphic HEMT [4], double or multiple channel HEMT [5] and advanced heterojunction materials systems such as, In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP. This materials system offers superior device properties to those of the AlGaAs/GaAs or the pseudomorphic AlGaAs/InGaAs/GaAs systems [6].

The In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP system presents a unique combination of high electron mobility, large conduction band discontinuity $\Delta E_C$, high peak saturation velocity, and large enough In$_{0.53}$Ga$_{0.47}$As bandgap (i.e., 0.7 eV) for normal room temperature operation. In order to utilize these advantages offered by this new materials system, one must be able to prepare the optimum HEMT structures with adequate materials qualities. This is done by using Molecular Beam Epitaxy (MBE), which is an ultra high vacuum epitaxial growth process with atomic scale control over the epitaxial layer thickness and alloy composition. Since this material system is relatively in its infancy, a considerable effort was made to investigate MBE growth of device quality In$_{0.52}$Al$_{0.48}$As and In$_{0.53}$Ga$_{0.47}$As heterostructures on InP. Further, in pursuing an optimum HEMT structure for higher two-dimensional electron gas (2DEG) density, which is essential for better device performance, various HEMT structures with uniform and planar doping were compared for their 2DEG sheet charge density and electron mobility. The systematic study of the MBE growth of In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As and its HEMT structure has generated a strong knowledge base and technical confidence in fabricating state-of-the-art In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT discrete devices and integrated circuits.

1.2 Motivation and objective
The potential advantages of using $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ system for high frequency HEMTs are obvious from the fundamental materials properties, as stated earlier. However, the world is never perfect, at least in the first beginning; high output conductance and high gate leakage current were the major problems associated with $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ based HEMTs. These undesirable phenomena were quite detrimental to HEMT high frequency performance [7, 8], and there was no satisfactory solution to solve these troublesome problems. The initial attempts at reducing the HEMT output conductance concentrated on the unintentionally doped epitaxial buffer material, since it was the most logical excess current path. This intuition led to the use of highly insulating, low temperature grown $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffers (i.e., LTB) [9, 10]. Though the LTB reduced the output conductance dramatically, it degraded the high frequency performance as well, which contradicts the expectation from an improved HEMT output conductance [7].

In order to gain the necessary knowledge on the basic HEMT operation, both analytical and computer simulations were used to acquire fundamental understanding of the HEMT characteristics. The use of a numerical two-dimensional device simulator has demonstrated tremendous value in pursuing the nature of technology-dependent device operation. To verify correlations between device behavior and the structural parameters, a PISCES-IIIB simulator, which solves the two-dimensional Poisson's and Continuity Equations, was used in this study to provide fundamental insight into the underlying device physics. The simulated results, based on the physically measured HEMT parameters, have shown excellent agreement with experimental observations.

From both numerical simulation and carefully executed experimentation, the high output conductance of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HEMTs has been determined to be due to a "2DEG carrier deconfinement" process, which causes the drain current to saturate prematurely. This is a direct consequence of the rapidly increasing 2DEG channel electric field under high drain to source bias. Based on this understanding, a new HEMT structural design approach was taken for reducing the peak 2DEG channel electric field, and the proposed structure was also demonstrated for the first time. This
approach employees a Low Conductance Drain (LCD) structure, which modulates the electric field distribution under the gate, hence limiting the maximum electric field below the threshold of the 2DEG carrier deconfinement process. This HEMT structure has achieved not only largely improved In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT output conductance, but greatly advanced the high frequency performance as well. State-of-the-art HEMTs and millimeter-wave monolithic integrated circuits (i.e., MMICs), which were developed based on the better understanding of the device physics and the LCD HEMT design approach, have been demonstrated.

1.3 Outline of thesis

Chapter 2 contains basically three major topic. The first describes basic HEMT operation and defines figures of merit for judging high frequency, high performance FETs. The second topic is an investigation of the In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP material system, to verify its superior electron transport characteristics and heterojunction properties, as well as its limitations which create problems with high output conductance in short channel In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMTs. This is followed by the third topic, the suggested Low Conductance Drain concept, which was deduced from a simple assumption of the substrate conduction contribution to excess drain current. The main objective in Chapter 2 is to provide comprehensive background materials for detailed discussions in later chapters. Chapter 3 concentrates on the PISCES two-dimensional simulation. This provides fundamental insight and demonstration of the device physics behind the LCD surface undoped HEMT structure. Chapter 4 describes the MBE growth of In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As on InP, and the optimization of the HEMT structure for higher 2DEG sheet charge density as well as higher electron mobility. This Chapter is particularly important since the starting material quality and structure integrity are the key issues for developing state-of-the-art HEMT devices. Chapter 5 provides information on device fabrication and process.
considerations, where ohmic contact and E-beam gate formation are the major issues. Chapter 6 presents HEMT device results from well designed and executed experiments to demonstrate the advantages of LCD surface undoped structure design. Both DC and microwave data between conventional highly doped and LCD undoped surface HEMTs were compared and discussed. Also presented in this Chapter are the latest (i.e., highest $f_t$) transistor and three record setting MMICs. These results are all based upon the LCD undoped surface HEMT structure. Chapter 7 probes further into details of the physical origin of the high output conductance in In$_{0.52}$Al$_{0.48}$As/ln$_{0.53}$Ga$_{0.47}$As/lnP HEMTs. A model for premature saturation of the drain current due to 2DEG carrier deconfinement is proposed for the first time. Chapter 8 summarizes the results of the present thesis, and provides suggestions for future work.
Chapter 2

InP based HEMT Technology

2.1 Introduction

In this chapter, we discuss some background materials and specific reasoning for approaches taken to advance the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HEMT technology. The subjects discussed in this chapter include basic HEMT operation, the figures of merit for high performance millimeter-wave HEMTs, the advantages of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ system for HEMT applications, the performance limitations of conventional HEMT design for short channel InP based HEMT, and finally, approaches to improve $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HEMT operation. These subjects provide comprehensive background information for more detailed discussions in the subsequent chapters, where specific developments in advancing HEMT technology are addressed.

2.2 High Electron Mobility Transistor (HEMT) operation

Figure 2.2.1 shows the basic band structure of a heterojunction HEMT, which consists a N-doped high band gap semiconductor and a narrower band gap semiconductor. The presence of an electron sheet charge accumulation layer located at the interface of some heterointerfaces was predicted [1] and first demonstrated in an $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ heterojunction [2]. Because the narrow band gap material has a higher electron affinity, electrons are attracted and accumulated in the narrow bandgap material at the heterointerface. This arrangement leads to reduced Coulombic scattering of accumulated electrons by the host donor impurities, hence preserving high drift mobility for mobile electrons.
The main principle of HEMT device operation is similar to that of a Si MOSFET, and the basic analytical charge control model for HEMTs has been described in earlier papers [11, 12]. In order to assist later discussion, some important concepts and equations are quoted and presented in this section. We start from the assumption of a quasi-constant electric field, $E$, in the triangular potential well of the HEMT energy band diagram shown in Figure 2.2.1, the 2DEG sheet charge density is expressed as [12]:

$$Q_s(x) = \frac{\varepsilon (V_G - V_{off} - V_C(x))}{(d + \Delta d)}$$

(2.2.1)

where $\varepsilon$ is the semiconductor permittivity, $V_G$ is the applied gate voltage, $V_C(x)$ is the channel voltage under the gate and $V_{off}$ is equal to $\Phi_m/q \cdot \Delta E_C/q \cdot qN_D/2\varepsilon d_d^2$. $d = d_d + d_i$ and $\Delta d = \varepsilon a/q$, where $d_d$ is the doped layer thickness, $d_i$ is the undoped spacer layer thickness and $a$ is equal to $0.125 \times 10^{-12}$ V.cm$^2$ [11]. From the 2DEG electron transport properties in compound semiconductor, one can separate the HEMT current-
voltage characteristics into two regions; (A) a linear region where the electron travels at relative constant mobility, hence the electron velocity is proportional to the conducting channel transverse electric field, and (B) a saturation region where electron travels at a constant velocity. Based on the charge control model, the channel current expression at position $x$ is:

$$I = Q_s(x) \cdot Z \cdot \nu(x),$$

(2.2.2)

where $Z$ is the gate width and $\nu(x)$ is the electron velocity at position $x$. $\nu(x)$ is equal to $\mu[\Delta V_c(x)/\Delta x]$ in the linear region and equal to $\nu_{sat}$ in the saturated region. In the linear region, the drain current $I_{ds}$ is equal to $[(\mu \cdot Z \cdot \varepsilon \cdot V_{ds} / L) \cdot (V_G - V_{off} - V_{ds})]$. While at velocity saturation, $V_{ds} = \varepsilon \cdot C \cdot L \cdot \nu_{sat} = \mu \cdot \varepsilon \cdot C$, where $\varepsilon \cdot C$ is the characteristic electric field for electron velocity saturation and $L$ is the gate length. The $I$-$V$ characteristics at the onset of current saturation can then be expressed as:

$$I_{dss} = \frac{Z \cdot \varepsilon \cdot \nu_{sat}}{d + \Delta d} (V_G - V_{off} - V_{ds}),$$

(2.2.3)

In short channel devices, the effective gate length modulation beyond current saturation is important to characterize the $I$-$V$ behavior. The channel potential $V_c(x)$ is obtained from the basic Poisson's equation as [12]:

$$\frac{\partial^2 V_c(x)}{\partial x^2} = \frac{I_{ds}}{Z \cdot \Delta d \cdot \nu_{sat}},$$

(2.2.4)

with the boundary conditions of $V_c(x=0) = V_{DS} - I_{ds}R_d$, and $V_c(x=\Delta L) = V_{DS} - I_{ds}R_d$, where $V_{DS}$ is the drain voltage when saturation occurs, and $R_d$ is the drain resistance.

The intrinsic transconductance, $g_m$, is defined as $\Delta I_{ds}/\Delta V_G$, and from Equation 2.2.3, the peak $g_m$ can be expressed as:

$$g_m, \text{ peak} = \frac{Z \cdot \varepsilon \cdot \nu_{sat}}{d + \Delta d},$$

(2.2.5)

As long as the space charge in the depleted large bandgap material remains constant, the variation of the 2DEG density, $Q_s$, is given by the gate capacitance $C_{gs}$ [13]:

$$C_{gs} = \frac{\Delta Q_s}{\Delta V_G} = \frac{\varepsilon \cdot Z \cdot L}{d + \Delta d},$$

(2.2.6)

The intrinsic current gain cut-off frequency, $f_t$, is then equal to:

8
\[ f_t = \frac{g_{m,\text{peak}}}{2\pi \cdot C_{gs}} = \frac{V_{sat}}{2\pi \cdot L} \tag{2.2.7} \]

It is clear from Equation 2.2.7 that the most important material parameter for high speed devices is the 2DEG electron saturation velocity, and the most critical HEMT structural parameter is the gate length. Thus seeking either a heterostructure or a new material system which gives the highest 2DEG saturation velocity are the primary research topics.

2.3 High frequency figures of merit

While the parameters defined in the previous section define the performance for the HEMT, various parasitic parameters, such as; output conductance, source resistance and gate feedback capacitance must be included in a complete HEMT model. Two figures of merit, the extrinsic current gain cut-off frequency, \( f_t \), and the maximum frequency of oscillation, \( f_{\text{max}} \), are typically used to give meaningful evaluation of the high frequency performance of HEMT. Both \( f_t \) and \( f_{\text{max}} \) are measured and extracted from microwave S-parameter measurements, which are typically performed with a HP8510 network analyzer with a Cascade on-wafer microwave probe station. In practical microwave frequency range, these parasitic parameters are neither negligible nor completely avoidable.

The intrinsic current gain cut-off frequency, \( g_m/2\pi C_{gs} \), is readily used in simplified or ideal case discussions, however a more rigorous derivation is needed to provide an adequate approximation of the extrinsic \( f_t \) [8]:

\[ f_t = \frac{g_m}{2\pi (C_{gs}+C_{gd})} \left[ 1+(R_s+R_d)g_0 \right], \tag{2.3.1} \]

where \( C_{gd} \) is the gate feedback capacitance, \( R_s \) and \( R_d \) are the source and drain resistances, respectively, and \( g_0 \) is the HEMT output conductance. It is clear that the extrinsic \( f_t \) is affected by parasitic elements of \( C_{gd}, R_s, R_d \) and \( g_0 \). The maximum
frequency of oscillation, \( f_{\text{max}} \), is even more strongly influenced by these parasitic effects. The expression for \( f_{\text{max}} \) derived from the HEMT equivalent circuit model shown in Figure 2.3.1, is [7]:

\[
 f_{\text{max}} = \frac{f_i}{\sqrt{4g_0(g_mR_iR_{s+R_g}) + \frac{4C_{gd}}{C_{gs}}(1 + \frac{2.5C_{gd}}{C_{gs}})(1 + g_mR_s)^2}} 
\]

(2.3.2)

where \( R_g \) is the gate metallurgical resistance and \( R_i \) is the gate input resistance. In evaluating HEMT millimeter-wave performance, \( f_{\text{max}} \) appears to be a better indicator to characterize the device, due to its comprehensive inclusion of all the major parasitic parameters. These elements become a far more severe issue for HEMTs when they are operated at millimeter-wave frequencies. This is especially important in ultra short gate length, small geometry HEMT devices designed for the highest frequency applications.

![Small signal equivalent circuit model of a short channel](image)

Figure 2.3.1: Small signal equivalent circuit model of a short channel

\( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP} \) HEMT.

2.4 \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP} \) material system

Figure 2.4.1 shows the energy gap versus lattice constant for most III-V compounds.
Since only binary compound (GaAs, InP, GaSb, InAs, etc.) substrates are available, there are only three lattice matching heterojunction material systems being studied for HEMT devices; namely AlGaAs/GaAs, AlSb/InAs/GaSb and InAlAs/InGaAs/InP.

![Diagram showing energy gap versus lattice constant at 300 K for compound semiconductors.](image)

**Figure 2.4.1:** Energy gap versus lattice constant at 300 K for compound semiconductors.

The AlGaAs/GaAs system has been studied extensively and it is regarded as the baseline for comparison of any new materials systems. Although the AlSb/InAs/GaSb system shows good promise for high speed HEMT operation, it has serious limitations because of the relatively high intrinsic carrier concentration, $n_i$, associated with the small band gap of InAs (i.e., 0.36 eV) [14] and the GaSb substrate. The high $n_i$ and narrow bandgap in InAs make it difficult to form useful Schottky barrier gates and avoid low voltage impact ionization breakdown at room temperature [15]. The high value of $n_i$ in GaSb also precludes the reduction in parasitic capacitances realized through use of a wider bandgap (e.g., GaAs, InP) semi-insulating substrate.

The InAlAs/InGaAs/InP system, on the other hand, posses unequaled properties for optimizing the 2DEG properties [16]. The advantages of the lattice matched
In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As alloy for high frequency HEMTs include the following:

1. High, low-field mobility. Using thick spacer of 100 Å HEMT structure, the room temperature 2DEG mobility can reach values as high as 13,700 cm$^2$/V.s, compared to approximately 8,200 cm$^2$/V.s for the AlGaAs/GaAs system.

2. Large conduction band discontinuity, $\Delta E_C$, between the lattice matched In$_{0.52}$Al$_{0.48}$As and In$_{0.53}$Ga$_{0.47}$As alloys. The larger the value of $\Delta E_C$, the deeper the quantum well and, thus the higher the 2DEG sheet charge density, $n_{SS}$. The $\Delta E_C$ for In$_{0.52}$Al$_{0.48}$As and In$_{0.53}$Ga$_{0.47}$As is 0.52 eV compared to only 0.23 eV for Al$_{0.3}$Ga$_{0.7}$As/GaAs [17]. The higher values of $n_{SS}$ yield superior current handling capability and higher HEMT transconductance, both of which are essential for high frequency and high power gain applications.

3. High peak saturation velocity. The peak electron velocity in In$_{0.53}$Ga$_{0.47}$As is 2.8x10$^7$ cm/s compared to 2.0x10$^7$ cm/s in GaAs for submicrometer distance samples [18]. Hence, for equal gate length FET or HEMT devices, the lattice matched In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT is potentially superior for ultra high frequency performance.

4. Larger value of $\Delta E_{\Gamma-L}$ (i.e., energy difference between the minima of the $\Gamma$ and L valleys). For submicrometer gate length FETs, the frequency response is inversely proportional to the transit time of conducting electrons, which is inversely proportional to $\mu\Delta E_{\Gamma-L}$ [19], where $\mu$ is the low field mobility and $\Delta E_{\Gamma-L}$ is the intervalley energy separation. For In$_{0.53}$Ga$_{0.47}$As, the value of $\mu\Delta E_{\Gamma-L}$ is 4760 cm$^2$/s compared to only 1520 cm$^2$/s for GaAs [19]. This figure of merit also indicates the superiority of the In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As lattice matched to InP system for higher frequency operation.
(a) Wave vector

(b)

Figure 2.4.2: Energy-band structures of (a) GaAs and (b) In$_{0.53}$Ga$_{0.47}$As.

(5) Greater velocity overshoot. Figures 2.4.2 (a) and (b) show the band structures associated with GaAs and In$_{0.53}$Ga$_{0.47}$As, respectively. Because of the larger intervalley separation, $\Delta E_{\Gamma-L}$, for In$_{0.53}$Ga$_{0.47}$As (i.e., 0.55 eV) compared to GaAs (i.e., 0.31 eV) [20], it is also expected that the electrons traveling in In$_{0.53}$Ga$_{0.47}$As will experience greater velocity overshoot. This property is particularly important in short channel HEMTs [21, 22]. Figure 2.4.3 illustrates the higher calculated current gain cut-off frequency of short gate length devices in In$_{0.53}$Ga$_{0.47}$As compared to GaAs, resulting from the higher electron saturation velocity and overshoot effects [19].
Figure 2.4.3: Computed performance of FETs, including velocity overshoot effect on Si, GaAs and InGaAs materials.

In summary, the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ system presents the most unique and the best combination of high electron mobility, large conduction band discontinuity, high peak and saturation velocities and large $\Gamma$-$L$ valley energy difference which combine to produce the highest frequency, lowest noise HEMT devices operating at room temperature.

2.5 Short channel $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HEMTs

As the E-beam direct write lithography technology has matured in recent years, the gate length of high performance HEMTs has been drastically reduced to a sub-half or even sub-quarter micron scale for higher frequency applications. This lithography
advancement has been applied to the In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT structure with amazing success, achieving greatly improved device performance at higher frequency compared to AlGaAs/GaAs based HEMTs [23, 24]. However, one rather troublesome issue has been the relatively high output conductance, $g_0$, which always appears in these sub-half or sub-quarter micron, ultra short channel In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMTs. This high output conductance severely limits the optimal device performance which could be achievable from this new heterojunction materials system.

Output conductances of over 50 mS/mm are typical for quarter micron gate length In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMTs [23, 24]. This high excess drain current (i.e., high output conductance, $g_0$), seriously degrades both $f_{\text{max}}$ and $f_t$ for high frequency HEMTs as shown in Equations 2.3.1 and 2.3.2. Figure 2.5.1 shows typical current-voltage characteristics, with a relatively high output conductance for a quarter micron gate length In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT.

![Drain Voltage (Volt)](image)

**Figure 2.5.1:** Typical short channel HEMT I-V characteristic, showing output conductance with two possible current sources; channel length modulation ($J_{\text{cm}}$) and substrate conduction ($J_{\text{sub}}$).
Based on the studies of Si MOSFETs and GaAs MESFETs, excess drain current beyond saturation (i.e., \( g_O \)) is traditionally related to two major mechanisms; namely channel length modulation (i.e., shrinkage of effective gate length) and substrate conduction [25]. Figures 2.5.2 (a) and (b) graphically illustrate the channel length modulation under two different drain biases and the conduction of excess drain current through the substrate, respectively.

(a) Channel length modulation

(b) Substrate conduction

Figure 2.5.2: Physical illustrations of (a) channel length modulation and (b) substrate conduction.

In the case of sub-half micron, ultra short gate length devices, the conducting channel electric field reaches its critical value \( \vec{E}_C \) (i.e., the value of electric field where the electron velocity saturates) quickly at relatively low drain to source bias, and the
position of the critical field, $\vec{E}_c$, becomes relatively insensitive to the incremental value of $V_{ds}$. This result suggests that the channel length modulation effect is not the major cause for the high output conductance, $g_O$, in short channel lattice matched In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMTs. The conduction of excess current through the substrate became the more likely reason thus responsible for the high excess drain current, especially since the background doping behavior for both In$_{0.52}$Al$_{0.48}$As and In$_{0.53}$Ga$_{0.47}$As epitaxial layers was not well understood.

In order to determine the possible solutions to this high output conductance problem, it was natural to first examine the field distribution obtained from solving the fundamental Poisson's equation (in one dimension for simplicity). Assuming the substrate is unintentionally doped or charge injected from doped channel, with a uniform net carrier concentration of $N_{sub}$, Poisson's equation is then expressed as:

$$\frac{\partial \vec{E}}{\partial x} = -\frac{q N_{sub}}{\varepsilon},$$

with boundary conditions of $V(L) = \int_0^L \vec{E}_c(x) \, dx = V_{ds}$, and $\vec{E}_c(0) = 0$. Integrate Equation 2.5.1 once and letting $U(x) = U_{sat}$ for short channel devices, one obtain from charge control model (i.e., $J = q N_{sub} U_{sat}$) the following expression:

$$J_{sub} = \frac{2 \varepsilon U_{sat} V_{ds}}{L^2} \alpha \frac{V_{ds}}{L} = \frac{<\vec{E}>}{L},$$

this shows that the substrate conduction current is directly proportional to the electron saturation velocity, $U_{sat}$, in the substrate, and the average substrate electric field, given by $<\vec{E}_c> = V_{ds} / L$. This simplified calculation provides two useful hints toward minimizing the substrate conduction; one approach is to reduce $U_{sat}$ in the substrate region, the other is to minimize the artificial substrate average electric field, $<\vec{E}_c>$. The approach of reducing the substrate $U_{sat}$ has been achieved by using a very low growth temperature MBE In$_{0.52}$Al$_{0.48}$As buffer layer [9, 10], which dramatically reduces both the electron mobility and saturation velocity, freezing out (i.e., deactivating) the background impurities. Though the use of low temperature buffer (LTB) has achieved large success in reducing the HEMT output conductance, it has
simultaneously degraded the transconductance, $g_m$, saturation drain current, $I_{dss}$, and the high frequency performance of the devices [10]. Figure 2.5.3 shows the inferior high frequency current gain performance of the LTB HEMT compared to the normal growth temperature buffer HEMT. This result contradicts the predictions of Equation 2.3.1 and 2.3.2, which suggest that the lower $g_o$ should improve both $f_t$ an $f_{max}$. The physical reason for this inconsistency between theory and LTB HEMT performance will be discussed in Chapter 7.

![Graph showing current gain vs. frequency for different buffer conditions](image)

**Figure 2.5.3:** Short circuit current gain ($I_{h21}$) measurements of 0.2 µm In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMTs with different buffers [10].

Due to the obstacles encountered by reducing the substrate electron saturation velocity through heavy damage or compensation of the substrate (i.e., LTB buffer), the average substrate electric field $\langle E_c \rangle$ was pursued as an alternate potential solution to reduce the In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT output conductance.
2.6 Low Conductance Drain design approach

The most straightforward way to reduce the average substrate electric field is by lowering the active layer conductance on the drain side of gate edge. This extends the distance over which the drain-source potential drops, hence achieving a lower $<\vec{E}_c>$. This approach has been named, by us, the Low Conductance Drain (LCD) design approach [26], which is analogically similar to the lightly doped drain (LDD) structure used in advanced Si MOSFETs [27].

To illustrate how the LCD design reduces both the peak channel electric field and the average substrate electric field, let us consider the basic recessed gate HEMT device structure shown in Figure 2.6.1.

![Diagram of recessed-gate HEMT](image)

*Figure 2.6.1: Schematic cross sectional view of a recessed-gate In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As on InP HEMT.*

Because the gate electrode is well defined through direct write E-beam lithography and the gate recess is very shallow (e.g., typical recess depth is 200 to 400 Å), the
recess edges of point A and B are extremely close to the gate of within couple hundred angstroms, revealed by scanning electron microscopy. If the recessed \( \text{In}_0.53\text{Ga}_0.47\text{As} \) cap layers are highly doped and conductive, it is reasonable to assume that the potential at point A is clamped close to the value of the drain potential (i.e., \( V_{ds} \)), since the potential drop from the drain electrode to point A is minimized by the low resistance of the highly doped surface cap layer. The potential at point B is, by the same argument, clamped close to ground potential since the source electrode is grounded. On the other hand, if the surface cap layer is undoped and highly resistive, then the potentials at point A and B will depart from the drain and source potentials, respectively, and vary as functions of the drain-to-source bias. Since the potential drop occurs primarily near the drain side of gate electrode, Figure 2.6.2 shows the ideal structure for a Low Conductance Drain (LCD) HEMT, where the recess length between gate and recess edge, \( L_{dc} \), is regarded as the optimizing parameter. This parameter is easily measured by SEM. However, other parameters, including the conductance of the surface cap layer (i.e., doping and thickness), the quantum well \( \text{In}_0.53\text{Ga}_0.47\text{As} \) channel thickness and buffer layer thickness are all relevant and should be treated as secondary parameters for LCD design as well.

![Figure 2.6.2: Schematic cross-sectional structure between the gate the drain electrodes. The recess distance of \( L_{dc} \) is used as design parameter to demonstrate the LCD design approach.](image-url)
Though the initial idea of LCD structure is aimed at reducing the substrate current, it is concluded in later chapters that the real $g_0$ reduction mechanism is most likely due to the elimination of 2DEG deconfinement induced premature current saturation, and not by the substrate conduction of excess current as initially speculated. This latter mechanism is also strongly dependent upon the peak electric field near the drain side of the gate, thus the LCD structure still provided a solution to the high $g_0$ problem.
Chapter 3

PISCES Simulation

3.1 Introduction

Since there are no two-dimensional heterojunction Poisson equation solvers available, we have adapted PISCES-IIB for homojunction to provide qualitative correlations between the HEMT structural parameters and the conducting channel electric field. Two-dimensional PISCES-IIB [28], which solves Poisson's and Current continuity equations, has been developed at Stanford over the past twenty years and is widely used in universities and industry. Because of the deficiency of PISCES to handle the heterojunction band discontinuity and quantized phenomena at the present time, the key assumption in the simulation is that we can create a homojunction, "quasi-HEMT" structure which will yield a meaningful electric field distribution between the gate and drain. PISCES takes input parameter values, such as; carrier concentration, electron mobility and saturation velocity of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layers, and the constituted 2DEG electrical properties from physical measurements, however, no consideration was given to the heterojunction band discontinuity. The main focus of this chapter is to illustrate, qualitatively, the channel electric field spreading effect due to design variations in highly conductive cap layer, hence providing an understanding of the underlying HEMT physics.

3.2 PISCES-IIB simulation Parameters

There are two categories of parameters used in the PISCES simulation, one is materials parameters, the other is structural parameters. Since the PISCES simulation allows for rectangular mesh generation, the creation of the recess gate structure is
straight forward in getting realistic representation of the HEMT cross section. The basic cross sectional structure used in the PISCES simulation is similar to Figure 2.6.1. The structural parameters were a gate length of 0.3 \( \mu \text{m} \), drain to source spacing of 1.0 \( \mu \text{m} \), gate to source spacing of 0.25 \( \mu \text{m} \) and gate to drain spacing of 0.45 \( \mu \text{m} \). The position of the gate recess edge is used to provide adjustment of the drain side active layer conductance, and changes in the distance between gate electrode and recessed edge (denoted as \( L_{dc} \)) are varied to examine the channel electric field spreading effect, where the drain side active layer conductance is reduced by extending \( L_{dc} \) farther toward the drain electrode.

The quasi-HEMT structure used in the PISCES simulation consists the following layers: a 1200 \( \AA \) buffer layer, a 200 \( \AA \) channel layer, a 300 \( \AA \) surface layer and a 300 \( \AA \) highly doped cap layer. Since PISCES-IIIB does not support parameters of \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) and \( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \), \text{GaAs} was used to give non-user defined material parameters, such as; effective density of states, dielectric constants, etc. Those parameters which can be defined directly by the PISCES user, were specified according to either published results [14], or experimental values acquired from layer thickness, Hall and C-V measurements on \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP} \) HEMTs. The 2DEG carrier is specified with a electron sheet charge density of 2.5\times10^{12} \text{ cm}^{-2} with room temperature mobility of 10,000 \text{ cm}^{2}/\text{V}.\text{s} and average saturation velocity of 2\times10^{7} \text{ cm/s}. The surface and buffer layers (i.e., \( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \)) were unintentionally doped N-type to 5\times10^{14} \text{ cm}^{-3} with mobility of 1000 \text{ cm}^{2}/\text{V}.\text{s}, while the N+ cap layer (i.e., \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \)) has a fixed doping concentration of 4\times10^{18} \text{ cm}^{-3} with mobility of 4000 \text{ cm}^{2}/\text{V}.\text{s} and saturation velocity of 1.2\times10^{7} \text{ cm/s}. The work function of the Schottky gate was chosen to be 4.6 eV for \( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \), as derived from barrier height measurement [29], and the dielectric constant of all layers is held constant at 13.

An example of the input file for a two-dimensional PISCES primitive simulation of \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP} \) quasi-HEMT structure is given in Appendix A.

3.3 Results and Discussions
As previously stated, the emphasis of this simulation was to qualitatively demonstrate the electric field spreading effect due to reduction of the surface cap layer conductance near the gate edge on the drain side. In practical HEMT devices, due to the existence of isotropic gate recess in the lateral direction, a $L_{dc}$ of 200 Å is used as the base line for conventional HEMT structures. Since the emphasis is on the drain side gate edge, where the channel electric field is most affected by the structural parameter, $L_{dc}$, it is adequate to show the detailed electric field distribution only in that particular region, as illustrated in Figure 2.6.2. Figure 3.3.1 (a) and Figure 3.3.1 (b) show the equipotential contour plots for the doped surface structure (a), with $L_{dc}$ of 200 Å (conventional HEMT design) and the undoped surface structure (b), with $L_{dc}$ of 2000 Å (LCD HEMT). This latter structure is essentially an ideal double recessed gate structure. Both structures are under the same drain-to-source bias of 3 Volts with the gate electrode grounded. It is clear from Figure 3.3.1 (a) and (b) that the equipotential contours are compressed by the highly doped N+ cap layer, resulting in higher electric field under and near the drain side gate edge. The comparison of channel electric field distribution between conventional (i.e., $L_{dc}$=200 Å) and LCD (i.e., $L_{dc}$=2000 Å) structures is shown in Figure 3.3.2, where the mid-channel electric field under and beyond the gate electrode is plotted as a function of distance (at a $V_{ds}$ of 2 Volts). The reduction of maximum electric field at the gate edge and the extension of electric field outside the gate region are indeed, in qualitative agreement with the argument stated earlier in Section 2.6. This comparison has also provided us a clearer picture of why the surface cap layer conductance affects the basic device operation. The high transverse electric field (parallel to the current flow), presented in the conventional HEMT structure with $L_{dc}$ of 200 Å, tends to reduce the electron confinement in the 2DEG quantum well, thus altering the current saturation characteristics of the In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT. The improvement in output conductance was first intuitively speculated to be achieved by reducing the carrier injection into the buffer, however the details of the device physics is not so straightforward as stated
here. Nevertheless, the reduction of the channel peak electric field provides insight into the device operation, thus providing a foundation to achieve full understanding of the physics behind the high output conductance issue.

Figure 3.3.1: Equipotential contour plots of the (a) doped surface structure ($L_{dc}=200 \text{ Å}$) and (b) LCD undoped surface structure ($L_{dc}=2000 \text{ Å}$).
Figure 3.3.2: The electric field distribution at the middle of the conducting channel, biased at $V_{ds}=2V$ for both doped surface ($L_{dc}=200\text{Å}$) and LCD undoped surface ($L_{dc}=2000\text{Å}$) structures.

Figure 3.3.3 (a) and (b) show the maximum mid-channel electric field as functions of the drain to source bias voltage near current saturation and pinch-off conditions, respectively. It is clear that the difference of maximum electric fields between conventional and LCD structures is more significant in the near saturation condition, due to the larger portion of drain voltage drop in the ungated region with higher drain current. This implies a greater output conductance improvement in the high drain current situation (near saturation) compared to a low current case (near pinch-off), which is indeed true, as will be shown in the experimental data (Figure 6.2.2).
Figure 3.3.3: The comparison of doped surface and LCD undoped surface HEMT peak channel electric fields versus $V_{ds}$ (drain to source bias) near (a) saturation current and (b) pinch-off conditions.
3.4 Summary

Because of the deficient modeling capabilities of heterojunction confinement in PISCES simulation, it is difficult to develop a detailed quantitative model for the 2DEG carrier distribution in the HEMT structure, or to compute accurate HEMT I-V characteristics based on our limited ability to include all the physical properties. It is however, possible to utilize a "quasi-HEMT" model in the PISCES simulation to demonstrate the important effects of the surface cap layer conductance on the conduction channel electric field. This model gives us some fundamental understanding of the underlying device physics. The concept of the Low Conductance Drain (LCD) design approach has been successfully demonstrated in our two-dimensional PISCES simulation; the 2DEG channel electric field, as well as the average electric field under the gate, are indeed influenced and modulated by the ungated active layer conductance where the recessed gate spacing, $L_{dc}$, is varied in the LCD design.
Chapter 4

Molecular Beam Epitaxial Growth

4.1 Introduction

The ternary compound, In$_{0.53}$Ga$_{0.47}$As, lattice matched to InP has attracted increased attention in recent years because its superior to GaAs electron transport properties for ultra high speed operation, as stated in Chapter 1. Although considerable progress has been realized toward better device performance, the fundamental growth processes of these ternary compounds is still not well understood. The focus of this chapter is to determine the critical growth conditions, which are peculiar to the MBE growth of In$_{0.53}$Ga$_{0.47}$As and In$_{0.52}$Al$_{0.48}$As lattice matched to InP.

During the MBE growth of GaAs, in order to obtain smooth and atomically abrupt interfaces, the cation surface migration is often enhanced so that the two-dimensional MBE growth process is promoted. This process is evident by observing the oscillation in the reflection high energy electron diffraction (RHEED) pattern [30]. However, in the case of ternary compounds, such as; Al$_x$Ga$_{1-x}$As and In$_{0.53}$Ga$_{0.47}$As, this enhancement of cation surface migration does not yield the same improvement, possibly due to preferential cation clustering [31]. The growth conditions which give good RHEED oscillations do not produce smooth and featureless surface morphology, thus disconnecting the correlation between growth front smoothness and the growth conditions set by the initiation of RHEED oscillation [32].

Earlier efforts using As$_2$ and optimizing the growth conditions have yielded considerable progress in producing higher quality In$_{0.52}$Al$_{0.48}$As and In$_{0.53}$Ga$_{0.47}$As layers [32, 33, 34, 35]. However, a comprehensive study of the various growth conditions on various In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT structures has yet to be carried out. In this Chapter, a comparative study of As$_2$ and As$_4$ growth of 0.5 μm
\( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \) and \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) epitaxial layers is presented. The resulting 2DEG properties of the \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP} \) HEMT structures with both uniform and atomic planar doped structures under optimized growth conditions are also discussed. While this work covers only a small part of the parameter space for \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP} \) MBE growth, the resulting materials and device properties suggest it is certainly near the optimum conditions.

4.2 MBE growth and composition control

The MBE growth of lattice-matched \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) epitaxial layers and 2DEG heterostructures was performed in a modified Varian MBE GEN-II system with two-inch non-indium bonded semi-insulating InP substrates. Molecular Beam Epitaxy (MBE) is a single crystal growth technique based upon precisely controlled evaporation of constituent elements in an ultra high vacuum environment [15]. Thermal molecular beams, which are controlled by the source temperature, are evaporated from effusion cells onto a heated substrate. Figure 4.2.1 shows a schematic diagram of a MBE growth chamber. The formation of ternary compound \( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \) and \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) epitaxial layers from molecular beams is based on the process of two-dimensional growth kinetics, which in general consists three steps to initiate MBE growth:

- **Step 1:** Physical adsorption of the constituent atoms and molecules on the growth substrate surface.
- **Step 2:** Surface migration of the adsorbed atoms to favorable sites (i.e., step ledges) and dissociation of the adsorbed molecules.
- **Step 3:** Chemical incorporation of the atoms to the lattice sites of the substrate, resulting in nucleation and monolayer growth.

On the bases of two-dimensional nucleation, the single-scattering reflection high energy electron diffraction (RHEED) technique and monolayer growth controlled RHEED oscillation process [30] are then used to provide in-situ atomic scale growth
information, such as, layer composition and monolayer growth rate, which are essential to MBE growth process optimization. The ternary compound composition was determined by using the RHEED oscillation technique on separate growths of (In)GaAs and (Al)GaAs on GaAs substrates to determine the partial growth rates of Ga, In and Al. By calculating the adatoms' arrival rate, one can precisely set the composition of ternary compounds of In$_{0.52}$Al$_{0.48}$As and In$_{0.53}$Ga$_{0.47}$As at the growth surface.

![Diagram](image)

**Figure 4.2.1:** Schematic diagram of a typical Molecular Beam Epitaxy system (courtesy of W. S. Lee).

Figure 4.2.2 shows some RHEED oscillation data taken during the growth of In$_{0.52}$Al$_{0.48}$As and In$_{0.53}$Ga$_{0.47}$As on InP. These data show that the specular beam intensity damps faster in the case of As$_2$ compared to As$_4$ for both In$_{0.52}$Al$_{0.48}$As and In$_{0.53}$Ga$_{0.47}$As growth, indicating reduced cation diffusion on the growth front with As$_2$ coverage [30]. The RHEED technique was utilized throughout this study to gain precise MBE growth control of the ternary compound composition, and to optimize the
growth parameters for better epitaxial film quality.

Figure 4.2.2: RHEED intensity oscillations of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ with $\text{As}_2$ and $\text{As}_4$ sources.
4.3 MBE growth of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ HEMT

The typical MBE growth rate used in this research was 0.3 μm per hour for both $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. The substrate temperature was varied from 300 to 490 °C to study the growth process. After the growth of various epitaxial structures, the epitaxial surface morphology was first studied by Nomarski phase contrast microscopy. Hall measurements were then used to provide electrical characterization of the net carrier concentration (e.g., 2DEG sheet charge density) and electron mobility. The basic HEMT structure used in this study was as follows: a 2500 Å $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ undoped buffer; a 320 Å undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer to form the 2DEG channel; a 30 Å $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ undoped spacer; either a uniform or pulse planar Si-doped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer, where the doped sheet charge or/and pulse layer thickness were varied to study the resulting electrical properties; a 250 Å undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer and a 30 Å undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface layer. The last layer was grown to reduce oxidation and prevent any surface depletion effect on the 2DEG electron properties.

Figure 4.3.1 shows the surface morphology of 0.5 μm thick, moderately Si-doped (mid $10^{17}$ cm$^{-3}$) $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ epitaxial layers grown with $\text{As}_4$ (Figures 4.3.1a and 1b) and $\text{As}_2$ (Figures 4.3.1c and 1d) sources, under the same group V to group III flux ratio of 14. There was almost no difference in either surface morphology or electron mobility (~ 410 cm$^2$/V.s at 300 K) between the dimeric and tetramermeric arsenic growth. The typical background doping concentration for $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ is approximately $6 \times 10^{14}$ cm$^{-3}$, N-type. Further increase of the $\text{As}_4$ or $\text{As}_2$ V/III flux ratios showed little change in either surface morphology or electrical properties of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ epitaxial layers.
Figure 4.3.1: Epitaxial surface morphology and particle related growth defects on \( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \) grown under \( \text{As}_4 \): (c) surface morphology, (b) growth defect and \( \text{As}_2 \): (c) surface morphology, (d) growth defect.

However, in the case of \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \), the situation was quite different. Figure 4.3.2 shows how the growth morphology of \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) is influenced by the arsenic species and its strong dependence on the V/III flux ratio with \( \text{As}_4 \) growth. The poor surface morphology of figure 4.3.2 (a) occurred at a relative low V(\( \text{As}_4 \))/III flux ratio of 16, however, this is the same flux ratio used for the layer shown in Figure 4.2.2, where pronounced RHEED oscillations were observed during the growth of
In$_{0.53}$Ga$_{0.47}$As. If the As$_4$ flux is increased further, the In$_{0.53}$Ga$_{0.47}$As surface morphology improves, as shown in Figures 4.3.2 (b) and 4.3.2 (c). This is a clear indication that the MBE growth of the In$_{0.53}$Ga$_{0.47}$As is vulnerable to cation (i.e., Ga and In) surface segregation, which is strongly affected by the cation surface mobility and is mainly controlled by the surface arsenic coverage. Since the surface texture in Figures 4.3.2 (a) and 4.3.2 (b) is not microscopically uniform throughout the surface, it is not likely that the poor surface morphology is due to As-vacancies or their related defect complexes as had been intuitively speculated.

Figure 4.3.2: Epitaxial surface morphology of In$_{0.53}$Ga$_{0.47}$As layers grown under different arsenic conditions; (a) As$_4$ with V/III ratio of 16, (b) As$_4$ with V/III ratio of 26, (c) As$_4$ with V/III ratio of 36, (d) As$_2$ with V/III ratio of 14.
Figure 4.3.2 (d) shows a smooth epitaxial surface of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ achieved with $\text{As}_2$ growth, even at the relatively low V/III flux ratio of 14.

After recognizing the influence of arsenic species on thick ternary compounds of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, the next step was to examine the influence of arsenic species on 2DEG structures. Figure 4.3.3 shows the planar doped 2DEG electron sheet charge density and mobility as a function of spacer layer thickness, with the doped sheet charge held constant at $5 \times 10^{12}$ cm$^{-2}$. The major difference in 2DEG properties between $\text{As}_2$ or $\text{As}_4$ growth appears to be in the 77 K electron mobility, where a substantial increase (30-50%) in mobility is obvious with $\text{As}_2$ growth.

![Graph showing the comparison of 2DEG mobility and sheet charge density as a function of spacer layer thickness for $\text{As}_4$ and $\text{As}_2$. The graph shows distinct trends for each material, with $\text{As}_2$ showing a higher mobility at 77 K compared to $\text{As}_4$.]

Figure 4.3.3: Comparison of the planar doped 2DEG electron sheet charge density and electron mobility as functions of the spacer layer thickness and arsenic species. The Si sheet doping density was constant at $5 \times 10^{12}$ cm$^{-2}$. 

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Since the 2DEG sheet charge densities are almost identical, the most reasonable explanation is that the heterointerface of the 2DEG quantum well is microscopically smoother with As$_2$ growth. This is consistent with our earlier discussion on surface morphology and the RHEED data.

Another parameter which can strongly influence the 2DEG properties is the manner in which doping is placed in the wide bandgap barrier layer. We investigated the 2DEG properties of both uniformly doped and atomic planar doped structures. The energy diagram of these two structures are illustrated in Figures 4.3.4 (a) and (b). Table 4.3.1 gives the measured 2DEG results by varying the doping structure from a three-dimensional uniformly doped layer to a two-dimensional, planar pulse doped layer. The sheet doping densities were kept constant at $5 \times 10^{12}$ cm$^{-2}$ and As$_4$ was used as the arsenic species.

![Figure 4.3.4: Band structures of uniformly doped and atomic planar doped (i.e., delta-doped) HEMT structures.](image)

(a) Uniformly doped HEMT

(b) $\delta$-doped HEMT
Planar versus Uniform Doping

<table>
<thead>
<tr>
<th>SI Type</th>
<th>Doping level/thickness</th>
<th>Spacer</th>
<th>Sheet Charge</th>
<th>Mobility</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uniform</td>
<td>$2 \times 10^{18}$ cm$^{-3}$/250 A</td>
<td>30 A</td>
<td>$2.35 \times 10^{12}$ cm$^{-2}$</td>
<td>10,100 cm$^{2}$/V.s</td>
</tr>
<tr>
<td>Uniform</td>
<td>$4 \times 10^{18}$ cm$^{-3}$/125 A</td>
<td>30 A</td>
<td>$2.72 \times 10^{12}$ cm$^{-2}$</td>
<td>10,500 cm$^{2}$/V.s</td>
</tr>
<tr>
<td>Planar</td>
<td>$5 \times 10^{12}$ cm$^{-2}$</td>
<td>30 A</td>
<td>$2.95 \times 10^{12}$ cm$^{-2}$</td>
<td>11,020 cm$^{2}$/V.s</td>
</tr>
</tbody>
</table>

Table 4.3.1: Comparison of 2DEG properties between uniformly and planar doped In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT structures.

It is evident from Table 4.3.1 that the 2DEG sheet charge increases as the doping pulse width decreases (thus increasing the heterointerface electric field). The electron mobility, on the other hand, increases gradually with increasing 2DEG sheet charge density, consistent with increased electron screening [36] of the Coulombic interaction (i.e., scattering) with the host impurities. This experiment showed definite advantages of the atomic planar doped structure over the uniformly doped structure. In order to acquire an even higher 2DEG sheet charge density with the planar doped structure, we undertook the experiment of increasing the planar doped Si doping density, where As$_2$ was used as the growth species since it offers superior 2DEG electrical properties as shown in Figure 4.3.3. Figure 4.3.5 shows that with further increase in Si dopant sheet density, the 2DEG sheet charge density increases continuously, without degrading the electron mobility. A 2DEG electron mobility of 11,080 cm$^{2}$/V.s at 300 K and 33,500 cm$^{2}$/V.s at 77 K, with a sheet charge of $3.9 \times 10^{12}$ cm$^{-2}$ was achieved. This is the best room temperature mobility with such high sheet charge density reported to date.
4.4 Summary

The MBE growth of In$_{0.52}$Al$_{0.48}$As/InP is relatively insensitive to either the arsenic species used or the V/III flux ratio. However, In$_{0.53}$Ga$_{0.47}$As is very strongly influenced by these parameters. The use of dimeric arsenic produces a superior epitaxial In$_{0.53}$Ga$_{0.47}$As surface morphology and higher low temperature 2DEG electron mobility. This improvement of low temperature 2DEG mobility is attributed to the microscopically smoother heterointerface obtained with As$_2$ growth. Due to the large $\Gamma$-L valley separation of the In$_{0.53}$Ga$_{0.47}$As channel layer, the room temperature 2DEG electron mobility remains relatively constant over a wide range of 2DEG sheet charge density, between 2.3 to 3.9 x $10^{12}$ cm$^{-2}$. A room temperature 2DEG mobility of
11,080 cm²/V.s at a very high corresponding sheet charge density of 3.9 \times 10^{12} \text{ cm}^{-2} has been demonstrated. These results show the excellent epitaxial quality of the MBE grown 2DEG structures achieved in this work, and they undoubtedly provide the foundation for state-of-the-art device and circuit performance.
Chapter 5

Device Fabrication

5.1 Introduction

It is not a trivial task to fabricate sub-half-micron HEMT devices, especially with the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ structures. The final HEMT performance and validity of the experimental comparison toward the HEMT structure improvement (i.e., LCD design) are directly related to the fabrication process. The short channel HEMT fabrication process to be discussed in this chapter focuses on two key issues: (1) Ohmic contact formation and its stability; (2) Sub-half-micron E-beam gate formation using a combination of E-beam lithography, gate recess and gate metallization. The process sequence is described early in this chapter to give some background information, and provide an overview to assist later detailed discussions. The basic E-beam lithography process was developed by Varian Associates, and it was adopted directly in this work without any change.

5.2 Process sequence

Though there are a number of choices in working with different processing steps, such as; photoresist types, exposure times, chemical etchants and metal thicknesses etc., the process sequence used in fabricating the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HEMTs is fairly conventional and straightforward, except for a few modifications. The fundamental process sequence is very much the same as for standard MESFETs [37], and the process steps are listed as follow:
(1) Mesa isolation
(2) Ohmic contact formation
(3) E-beam gate formation
    (i) E-beam lithography (ii) Gate recess (iii) Gate metallization
(4) Overlay metallization and dielectric passivation

From a practical point of view, only steps (2) and (3) are critical and sufficiently important for detailed discussion. Appendix B provides a complete process flow and actual process schedule for further reference.

5.3 Ohmic contact formation

The ohmic contact is a crucial process to minimize the parasitic resistances produced in the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HEMTs, and its formation is not readily compatible with the well established GaAs ohmic contact process for two major reasons: (1) the quality of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial layer degrades rapidly with prolonged heat treatment. A typical decrease of 30-40% in 2DEG mobility was observed when the structures were annealed at 350 C for 15 minutes, while the standard AuGe/Ni/Au contact for GaAs requires temperatures as high as 450 C; (2) The active layer used for 2DEG formation is extremely close to the surface (e.g., about 400 Å in total thickness), hence the alloyed ohmic metal penetration depth control is very important to minimize the overall contact resistance [38, 39]. Thus optimizing the sintering temperature and achieving reliable control of process parameters over the ohmic formation are important in these ultra thin, thermally sensitive structures.

Three types of ohmic metal schemes, Au/Ge/Ni/Au (400Å/100Å/125Å/1000Å), Ni/Ge/Au/Ni/Au (100Å/400Å/800Å/200Å/100Å) and standard eutectic AuGe/Ni/Au (500Å/125Å/1000Å), were experimentally compared for minimum contact resistance and thermal stability. A thin Ni layer is typically utilized as a good adhesion promoter, and a good wetting agent when eutectic metallization such as AuGe (88% Au and 12% Ge)
is used in the ohmic contact. Figure 5.3.1 shows the thermal stability comparison of these three metallizations, starting from their minimum contact resistance positions obtained after a 350°C, incremental alloying time process. It is clear that Au/Ge/Ni/Au gives the highest contact resistance with poor thermal stability, while Ni/Ge/Au/Ni/Au and eutectic AuGa/Ni/Au give a relatively similar value of specific contact resistance, $1.2-2.0 \times 10^{-5} \, \Omega \cdot \text{cm}^2$, with almost the same thermal stability. Because the eutectic AuGe/Ni/Au metallization is readily available, it was chosen as the standard ohmic contact for \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP} \) HEMTs. The typical alloy condition is 15 sec at 350°C by rapid thermal annealing or 30 sec at 350°C by furnace anneal, which is about 100°C below the ohmic formation temperature used in GaAs MESFET technology.

![Graph showing contact resistance as a function of anneal time for Au/Ge/Ni/Au, AuGe/Ni/Au, and Ni/Ge/Au/Ni/Au.](image)

Figure 5.3.1: Comparisons of minimum contact resistance and thermal stability of three different ohmic metal systems. Both AuGe/Ni/Au and Ni/Ge/Au/Ni/Au are similar in ohmic contact performance.
Although the specific contact resistance obtained from this process is adequate at the present time for device applications, it is still some distance away from the value required for ultra-small geometry, high speed devices where a contact resistance of less than $10^{-7}$ to $10^{-6}$ $\Omega \text{ cm}^2$ is definitely needed. There is thus still considerable room for improvement in contact resistance and its associated long term reliability.

5.4 E-beam gate formation

The sub-half-micron E-beam process utilized in this thesis was developed at the Varian Research Center (VRC). Early work was concentrated on a 0.3 um, standard triangular gate profile using a 9300 Å thick layer of KTI-496K PMMA (7.5% blend) resist. The exposure was performed at 20 kV with exposure conditions of 2nA, 200 kHz and 4 adjacent passes. Subsequently, because of the demand for reducing the sub-half-micron gate resistance for better gain and noise performance over the ordinary triangular gate profile, a tri-layer resist T-gate (i.e., mushroom gate) process was developed. A 3000 Å thick 496K PMMA is first applied. This layer has low E-beam exposure sensitivity, thus achieving the smallest possible footprint of the T-gate. The next layer is a P(MAA-MMA) copolymer, which has very high sensitivity to E-beam exposure, hence allowing the build up of a large gate cross sectional area, thus lowering the gate resistance. The top layer is a thin, 1000 Å thick layer of 496K PMMA resist to minimize the exposure dose adsorption, while allowing an overhang structure for clean liftoff of the gate metallization. Each of these layers is individually baked on a hot plate at 160 C, and the bottom PMMA layer is baked longer to decrease its exposure sensitivity and increase its adhesion to the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial surface.

The tri-layer E-beam resist is developed by spray development and is closely monitored by SEM. After development of the gate level resist, the exposed channel was shallow recessed by using a phosphoric acid and peroxide based etchant, which is used to avoid attacking the E-beam resist. After the gate recess etch achieves the desired drain current, a total of 4000 Å of Ti/Pt/Au metallization is then deposited by electron beam
evaporation to form the Schottky barrier gate. The reactive Ti is used to promote metal gate adhesion, while Pt is used as a Au diffusion barrier to prevent intermixing of different metal elements with the overlaying Au layer. Figure 5.4.1 shows the tri-layer, E-beam direct write T-gate structure after gate metallization and liftoff.

Figure 5.4.1: SEM photomicrograph of Varian quarter-micron T-gate structure with the tri-layer PMMA photoresist E-beam process.

After the gate liftoff, the discrete HEMT devices are ready for on wafer DC and microwave testing to measure their I-V and high frequency S-parameter characteristics. A Plasma Enhanced Chemical Vapor Deposition (PECVD) silicon nitride layer of 2000 Å is deposited before the HEMT chip is diced and separated. Figure 5.4.2 shows a SEM photomicrograph of a completed In0.52Al0.48As/In0.53Ga0.47As/InP HEMT with an air bridge connection for multiple gate pads. After the completion of all fabrication processes, the discrete HEMT is ready for various microwave evaluations. The characterization of microwave gain, current gain cut-off frequency, maximum
frequency of oscillation and noise figure are performed either with HEMT devices mounted on a 70-mil slot chip carrier or direct, on-wafer Cascade probing.

Figure 5.4.2: SEM photomicrograph of a completed quarter-micron gate length HEMT with air bridge interconnect.

5.5 Summary

The photolithography processes used in the fabrication of sub-half micron In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP HEMTs are in general similar to the processes used for GaAs MESFETs or AlGaAs/GaAs HEMTs. The major difference is the ohmic contact formation, which must be performed at a relatively low alloy temperature of 350 C. The sub-half micron E-beam process is undoubtedly the most important and
dominant processing factor in achieving good high frequency performance. By taking advantage of the well established E-beam process developed by the Varian E-beam center, the In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT fabrication process adopted in this thesis work is well controlled, reproducible and of excellent quality.
Chapter 6

Device results and applications

6.1 Introduction

The previous discussions defined the preferred In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As lattice matched to InP HEMT structure with the Low Conductance Drain (LCD) approach. Unfortunately, realization of this concept is not straightforward. Though the double recess gate structure is probably the best way to demonstrate the LCD concept, due to re-alignment constrains and inadequate control over sub-half-micron dimensions, it is not a practical approach at the present time. Because of this complication, the easiest approach to demonstrate the LCD structure is to go to the extreme case of making the characteristic length, $L_{dc}$, the same as the spacing between the gate and drain electrodes. This approach implies that the surface N+ cap layer can either be removed or replaced by a low conductance, undoped cap layer. While not necessarily optimum, this allow us to demonstrate the desirable effect of channel electric field spreading to improve the output conductance.

In this chapter, direct comparisons are presented of both DC and high frequency performance of conventional, highly doped surface structures with a short recess to gate spacing, and LCD undoped surface structures In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMTs [40]. The LCD undoped surface HEMT structures have achieved dramatic improvements in output conductance, and subsequently produced higher maximum stable gain (MSG) and maximum frequency of oscillation ($f_{\text{max}}$) [41]. These high frequency improvements reflect both the success of the new LCD device design as well as having access to state-of-the-art HEMT fabrication technology for microwave and millimeter wave monolithic integrated circuits (MMICs). Several examples of these results will be selectively presented in this Chapter to highlight the important impacts of the LCD
undoped surface HEMT structures.

6.2 Comparison of LCD and conventional HEMT designs

Figure 6.2.1 shows the basic $\text{In}_{0.52}\text{Al}_{0.48}\text{As/In}_{0.53}\text{Ga}_{0.47}\text{As/InP}$ HEMT structure used in comparison of the conventional, highly doped surface structure and LCD undoped surface structure HEMTs. The HEMT structures consist of the following layers: a 2500 Å $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ undoped buffer; a 320 Å $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer to form the 2DEG channel; a 30 Å $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ undoped spacer; a 250 Å, $2\times10^{18}$ cm$^{-3}$ Si-doped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer to provide the 2DEG sheet charge; a 150 Å undoped $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ Schottky enhancement layer, and; either a 100 Å, $2\times10^{18}$ cm$^{-3}$ Si-doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer (conventional doped surface) or a 30 Å undoped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ cap layer (LCD undoped surface). These layers were sequentially grown on (100) InP:Fe semi-insulating substrates.

![Diagram showing HEMT structure](image)

Figure 6.2.1: The basic HEMT structure used in comparison of doped surface and LCD undoped of doped surface designs. The only variable is the InGaAs cap layer conductance.
Hall measurement of this structure yielded a 2DEG density of $2.3 \times 10^{12}$ cm$^{-2}$, with an electron mobility of 9500 cm$^2$/V.s at 300 K. Since the In$_{0.53}$Ga$_{0.47}$As surface layer has no surface Fermi-level pinning [42], this thin but highly doped surface layer is not depleted as in the case of GaAs, whose surface Fermi level is typically pinned at the middle of the band gap [43]. This behavior has reflected on the decrease of overall sheet resistance when Si dopant was introduced into the thin surface In$_{0.53}$Ga$_{0.47}$As layer.

These structures were fabricated into 0.3x150 $\mu$m$^2$ HEMTs by the direct write E-beam processes described in Chapter 5. Figure 6.2.2 shows a comparison of typical I-V characteristics between (a) conventional doped surface and (b) LCD undoped surface HEMTs. The values of $I_{dss}$ were selected to be reasonably close to each other. This was accomplished through control of the shallow gate recess etch. It is clear from Figure 6.2.2 that the major difference in the I-V characteristics between these two structures is the output conductance (i.e., $g_O$). For the highly doped surface HEMT, the output conductance is approximately 50 mS/mm, with a maximum extrinsic $g_m$ of 500 mS/mm. Both $g_m$ and $g_O$ tend to increase at higher value of $V_{ds}$, however the shape of the $g_m$ versus $V_{gs}$ characteristic remains the same as $V_{ds}$ increases from 1 to 3 Volts. The LCD undoped surface HEMT, on the other hand, exhibits a low output conductance of 10-15 mS/mm, with a maximum extrinsic $g_m$ of 460 mS/mm. The maximum value of $g_m$ occurs at a relatively low value of $V_{ds}$ (i.e., 0.8-1.2 V), and decreases when $V_{ds}$ is increased. This characteristic is more dramatic on a device fabricated for higher $I_{dss}$, as illustrated in Figure 6.2.3, where the general shape of the $g_m$ versus $V_{gs}$ characteristic changes and the maximum value of $g_m$ decreases as $V_{ds}$ increases from 1 to 2.5 V. This behavior is believed to be due to the high electric field in the velocity-saturated region, which extends toward the drain in the ungated region between gate and drain at high drain bias. This effectively increases the velocity-saturated drift distance of the charged carriers, hence suppressing the $g_m$ under high $V_{ds}$. This behavior might seem to degrade device performance rather than improve it; however, since the electric field extension effect reduces the output conductance more dramatically than it degrades.
the transconductance, the voltage gain (i.e., $g_m/g_o$ ratio) is still improved by almost a factor of 3. Though the maximum value of $g_m$ varies with $V_{ds}$ as shown in Figure 6.2.3, the transconductance remains relatively constant with $V_{gs}$ at higher $V_{ds}$, which leads to improved power gain linearity as will be shown in Section 6.3.

![Graph](image)

Figure 6.2.2: Comparison of typical I-V characteristics between (a) doped surface and (b) LCD undoped surface, 0.3 micron gate length HEMTs.
Figure 6.2.3: Dependances of extrinsic transconductance of undoped surface HEMT on drain-source bias voltage. The suppression of $g_m$ at high $V_{ds}$ (i.e., above 2 volts) is absent for highly doped surface HEMT.
From Figure 6.2.2, one can observe that the output conductance near $I_{dss}$ is improved the most, while $g_o$ remained almost the same near pinch-off for the LCD design. This observation correlates well with the PISCES simulation results described earlier (Figures 3.3.3 and 3.3.4), where the changes of peak channel electric field between the conventional and LCD HEMTs exhibits a similar behavior trend. This correlation strongly suggests that the output conductance is directly related to the 2DEG peak channel electric field, which actually has little influence on with the charge control model used for analytical study of HEMT I-V characteristics. There must thus be some secondary effects to link $g_o$ and the peak channel electric field. This topic is discussed in more details in Chapter 7.

The best figure of merit for HEMT millimeter-wave performance, the maximum frequency of oscillation, $f_{max}$, was defined in Equation 2.3.2. This shows that $f_{max}$ is strongly affected by both $g_m/g_o$ and $C_{gd}/C_{gs}$ ratios. The improvement in the $g_m/g_o$ ratio obtained from the LCD undoped surface HEMT is expected to yield a higher value of $f_{max}$ based upon Equation 2.3.2. As for the ratio of $C_{gd}/C_{gs}$, $C_{gd}$ is typically very small and difficult to accurately extracted from S-parameter measurements, thus it is too subjective to make a good quantitative comparison at the present time. However, a 50% reduction of $C_{gd}$ was predicted by the model of a recessed gate MESFET [44]; thus a meaningful improvement of the $C_{gd}/C_{gs}$ ratio is also expected for the LCD undoped surface structure. The gate-to-source input capacitance has been measured using a 1-MHz static capacitance measurement. The values of $C_{gs}$ were 0.19 pF and 0.17 pF for the conventional doped surface and LCD undoped surface HEMTs, respectively. The slight decrease of $C_{gs}$ is reasonable, since the LCD structure inherently gives a lower fringing capacitance due to its smaller side wall electric field.

A comparison of the typical Ti/Pt/Au Schottky gate I-V characteristics is shown in Figures 6.2.4 (a) and (b) for the conventional and LCD structures, respectively. When the gate is reverse-biased to greater than 1 V, the conventional doped surface HEMT shows a much higher gate leakage current than the LCD undoped surface device. This
phenomenon is explained by the fact that the electric field associated with the Schottky gate is reduced when the surface layer is not highly conductive (i.e., with a highly doped cap layer).

![Figure 6.2.4](image)

**Figure 6.2.4:** Comparison of the gate Schottky characteristics between (a) doped surface and (b) LCD undoped surface HEMTs. Gate dimension is 0.3x150 μm².

Figure 6.2.5 shows a comparison of the maximum stable gain (MSG) versus frequency for 0.3 micron gate length conventional doped surface and LCD HEMTs. The
LCD undoped surface HEMT achieved a maximum gain of 19.2 dB at 18 GHz, due largely to the improved $g_m/g_o$ ratio. When the measured S-parameter are extrapolated at -6 dB per octave in frequency, both doped and undoped surface devices produced almost the same unity current gain cutoff frequency of 70 GHz. However, as shown in Figure 6.2.5, the extrapolated $f_{\text{max}}$ is 190 GHz for the LCD surface undoped HEMT compared to 120 GHz for the conventional highly doped surface HEMT.

![Graph showing microwave gains of conventional and LCD undoped HEMTs.](image)

**Figure 6.2.5:** Measured microwave gains of conventional surface and LCD undoped surface HEMTs. Both devices show similar current gain cutoff frequency of 70 GHz.

At 18 GHz, both the conventional doped surface and LCD undoped surface HEMTs achieved approximately the same minimum value of noise figure, 0.8-1.0 dB. Any difference in noise figure between the two devices was not obvious, and may possibly be
slightly worse for the undoped surface HEMTs due to slightly higher parasitic source resistance and lower extrinsic transconductance.

In order to demonstrate the improvements of the LCD design with an even higher performance HEMT structure, another set of comparison devices with atomic planar doping and 0.25 micron T-gates (i.e., mushroom gates) was carried out. A cross sectional view of the high performance, atomic planar doped HEMT structure with a 0.25 micron T-gate is shown in Figure 6.2.6.

![Diagram of high performance planar doped HEMT structure with quarter-micron T-gate.](image)

Figure 6.2.6: High performance planar doped HEMT structure with quarter-micron T-gate.

The fabrication processes for these devices are identical to the earlier devices except for the tri-layer photoresist T-gate process described in Chapter 5. The basic HEMT epitaxial structures used for this comparison were as follows: a 2500 Å In$_{0.52}$Al$_{0.48}$As undoped buffer; a 320 Å undoped In$_{0.53}$Ga$_{0.47}$As layer to form the 2DEG channel; a 30 Å In$_{0.52}$Al$_{0.48}$As undoped spacer; an atomic planar Si doping of $6 \times 10^{12}$ cm$^{-2}$ to provide the 2DEG sheet charge; either a 200 Å undoped In$_{0.52}$Al$_{0.48}$As Schottky enhancement layer and a 100 Å, $2 \times 10^{18}$ cm$^{-3}$ Si-doped In$_{0.53}$Ga$_{0.47}$As cap layer.
(conventional doped surface HEMT), or a 250 Å undoped In$_{0.52}$Al$_{0.48}$As layer and a 30 Å undoped In$_{0.53}$Ga$_{0.47}$As cap layer (LCD undoped surface HEMT). These layers were again sequentially grown on (100) oriented, Fe doped InP semi-insulating substrates. Hall measurements of the undoped surface structure yielded a 2DEG density of 3.4x10$^{12}$ cm$^{-2}$, with a room temperature electron mobility of approximately 11000 cm$^{2}$/V.s.

Figure 6.2.7 shows a comparison of typical I-V characteristics of (a) conventional highly doped surface and (b) LCD undoped surface HEMTs with 0.25 micron T-gate. Careful measurement of the extrinsic transconductance and output conductance shows that, for the conventional surface doped device, the output conductance is approximately 55 mS/mm with a maximum value of extrinsic $g_{m}$ of 933 mS/mm. The LCD undoped surface HEMT, again exhibits a lower output conductance of less than 30 mS/mm with a maximum value of extrinsic $g_{m}$ of 800 mS/mm. As a consequence of this improvement in $g_{o}$, the voltage gain ratio of $g_{m}/g_{o}$ has been improved from 16 in the conventional HEMT, to over 27 for the LCD HEMT. Figure 6.2.8 shows a comparison of the maximum stable gain (MSG) versus frequency for the highly doped surface and LCD undoped surface HEMTs. A state-of-the-art MSG of over 20.1 dB at 18 GHz has been achieved with the LCD undoped surface HEMT compared to 17.5 dB for the conventional design. Though the $f_{t}$ is again approximately the same for both devices at 90 GHz, an extrapolated $f_{\text{max}}$ of over 220 GHz is achieved for the LCD undoped surface HEMT compared to 160 GHz for the doped surface HEMT. This again demonstrates the validity of Equation 2.3.2.
These results clearly demonstrate that $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HEMT surface conductance, controlled by the surface cap layer doping and thickness, strongly affects the charge control nature of the 2DEG channel. By utilizing the concept of Low Conductance Drain design in order to reduce the 2DEG channel peak electric field, the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HEMT output conductance, as well as the high
frequency small signal gain performance have been significantly improved.

\[
\begin{align*}
\text{Gain (dB)} & \\
0 & 10 & 20 & 30 & 40 \\
1 & 10 & 100
\end{align*}
\]

**Figure 6.2.8:** Measures microwave gains of doped surface and LCD undoped surface HEMTs with 0.25 μm T-gate structures. A current gain cutoff frequency of over 90 GHz has been achieved by using the LCD undoped surface structure.

Because of the extension of electric field toward the drain in the ungated region (Figure 3.3.1), the effective conducting electron transit time is increased, since the saturated 2DEG electrons must travel through both the effective gate length plus the field spreading region before they are collected. This effect would predict a lower value of \( f_t \), in comparison to the expression in Equation 2.3.1, which is based upon a circuit model [8]. The net effect of the LCD structure on the current gain cut-off frequency, \( f_t \), may be a combination of these two competing processes, and thus becomes very hard to predict. Though the comparison studies did not clearly indicate a improvement of \( f_t \) in the LCD structure, a state-of-the-art current gain cut-off frequency of 260 GHz, with
non self-aligned LCD undoped surface HEMT structure, was demonstrated with a ultra short T-gate of 0.08 μm gate length In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT [45]. Figure 6.2.9 shows the calculated short circuit current gain $|I_{h21}|$ as a function of frequency for this ultra high speed LCD undoped surface HEMT.

![Graph showing the relationship between gain (dB) and frequency (GHz).]

Figure 6.2.9: Current gain (i.e., $|I_{h21}|$) of 0.08 μm HEMT as a function of frequency with input and output pad capacitances removed [45].

The maximum frequency of oscillation measured on comparable structures in the comparison studies, has clearly demonstrated that the LCD undoped surface HEMTs produced substantially higher value of $f_{\text{max}}$. In fact, the highest reported $f_{\text{max}}$ value of 455 GHz [46] was achieved through applying a similar LCD undoped surface HEMT structure developed in this thesis work.

6.3 Power performance of LCD undoped surface HEMTs
Because of the improved gate leakage and breakdown characteristics of LCD undoped surface HEMTs, it is possible to bias the devices at higher values of $V_{ds}$ and produce appreciably more power with the LCD structure. Power measurements were made on 0.3 micron gate length In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMTs with 150 $\mu$m gate periphery. When biased at $V_{ds} = 5$ V and $I_{dss} = 30$ mA, this device achieved a 1-dB gain compression power of 16.5 dBm with 11.3 dB gain, and a maximum power of 16.8 dBm with 10.2 dB gain at 18 GHz, as shown in Figure 6.3.1.

Figure 6.3.1: Power performance and associated gain of a LCD undoped surface In$_{0.52}$Al$_{0.48}$As/In$_{0.52}$Ga$_{0.47}$As HEMT measures at 18 GHz.
Though the power performance is not outstanding due to the limited input voltage swing (i.e., low pinch-off voltage), the most significant feature is the power gain linearity, which is excellent for HEMT type devices. This linearity is mainly due to the compressed, but relatively constant $g_m$ versus $V_{gs}$ curve observed at higher values of $V_{ds}$ bias, as shown in Figure 6.2.3.

The main disadvantage of the LCD undoped surface for power applications is that its I-V characteristics could easily produce Gunn oscillations [47] when biased at higher values of $V_{ds}$, generating a propagating dipole layer which moves through the electric field spreading region between the gate and drain electrodes. This phenomenon, however, is solvable by optimizing the parasitic surface conductance or by utilizing the double recess structure, which limits the electric field spreading distance (i.e., $L_{dc}$). Though the structure of undoped surface $\text{In}_{0.52}\text{Al}_{0.48}\text{As/In}_{0.53}\text{Ga}_{0.47}\text{As/InP}$ HEMT is not well optimized at the present time, the LCD structure is potentially capable of offering much lower gate leakage current and higher breakdown voltage, which is undoubtedly makes the LCD HEMT a very attractive structure for millimeter wave power applications.

6.4 Application of LCD HEMTs to mm-wave integrated circuits

In an extension of this study, pursued mainly by projects funded at Varian Associates, a number of millimeter-wave monolithic integrated circuits (MMICs) have been successfully designed and fabricated utilizing the LCD undoped surface $\text{In}_{0.52}\text{Al}_{0.48}\text{As/In}_{0.53}\text{Ga}_{0.47}\text{As/InP}$ HEMT [48, 49, 50, 51, 52, 53, 54]. Among these MMIC developments, three have achieved record setting performance;

(1): A seven-section distributed amplifier for operation over a bandwidth of 5 to 100 GHz, with an average gain of 5 dB across the entire band [50]. Figure 6.4.1 shows photomicrograph of the InP based 5-100 GHz MMIC. The measured gain

62
over the entire 5-100 GHz band is shown in Figure 6.4.2. This result represents the highest frequency multi-octave, and widest bandwidth distributed amplifier demonstrated to date. This circuit has set a milestone in the high frequency MMIC development.

Figure 6.4.1: Photograph of a single stage, 7-section 5-100 GHz $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As/InP}$ HEMT distributed amplifier [50].
Figure 6.4.2 Measures gain over the whole 5-100 GHz band with the InP based distributed MMIC amplifier [50].

(2): A Ka-band cascode distributed amplifier, which has demonstrated a small signal gain of 15 +/- 1 dB and a noise figure of 2.5-4 dB from 5 to 50 GHz [53]. Figure 6.4.3 shows a photomicrograph of the cascode distributed amplifier. The measured small signal gain across the entire frequency band is shown in Figure 6.4.4. This is the best reported gain and noise figure for a MMIC amplifier to date over these bandwidths.
Figure 6.4.3: Photograph of a monolithic 5 to 50 GHz cascode \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP} \) HEMT distributed amplifier [53].

Figure 6.4.4: Measured gain, return loss of the 5-50 GHz monolithic InP based cascode distributed amplifier [53].
A single stage, W-band distributed amplifier with a gain of 8.0 dB from 75 to 100 GHz [54], is shown in Figure 6.4.5. This is the best gain ever reported for monolithic integrated circuits in this frequency range.

![Graph showing gain vs frequency](image)

**Figure 6.4.5**: Measured 75-100 GHz gain of a single stage, w-band InP based HEMT monolithic cascode distributed amplifier (biased for maximum bandwidth) [54].

These results are clear indications that In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT with the LCD undoped surface structure is of extreme value for advancing high frequency, high performance MMIC developments.

### 6.5 Conclusion

Direct comparison of DC and microwave measurements between conventional doped surface and LCD undoped surface In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMTs, has
clearly demonstrated the improvements of short channel HEMT output conductance and its related \( f_{\text{max}} \) values, predicted by arguments given in Chapters 2 and 3. The troubling issue of high output conductance in \( \text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP} \) HEMTs has been successfully controlled, and perhaps finally solved through the concept of surface conductance induced 2DEG channel electric field modulation. Applications of this Low Conductance Drain (LCD) design have demonstrated its unique and valuable contributions to the advancement of millimeter-wave monolithic integrated circuit technology.
Chapter 7

Physical origin of the high output conductance

7.1 Introduction

The ultimate goal for this thesis has been to, not only demonstrate higher frequency HEMT devices and circuits, but to understand the nature of the physics behind these improvements. In Chapter 2, an intuitive explanation for using the Low Conductance Drain (LCD) approach was presented. While the LCD structure clearly reduced the output conductance, it is important to examine the self-consistency of this model with all of the experimental results. If these results fail this test, then we must search for the real mechanism and understand why our incorrect initial assumption led to the desired improvements.

From the experimental results presented in Chapters 4 and 6, we concluded that the background impurity concentration of the In$_{0.52}$Al$_{0.48}$As buffer used in the HEMT structures was not sufficient, by a factor of over 30, to conduct the high excess drain current observed in short channel HEMTs. Since the decrease of peak channel electric field with the LCD structure was clearly demonstrated by the PISCES simulation, the real question is how this peak electric field effects the drain current saturation. From Chapter 2, the 2DEG carrier density at velocity saturation is determined mainly by the gate potential and not by the drain-source bias. Thus from the basic charge control model, the transverse peak channel electric field should have no effect on the 2DEG carrier density which travel across the gate electrode. The explanation for the drain current increase with drain potential must then be related to the transport behavior of those 2DEG electrons entering the constant velocity regime. The conventional electron velocity saturation conditions may thus be altered due to the high transverse (i.e., parallel to the heterojunction interface) channel electric field. Because of both
individual energy bands and the heterojunction band alignment, there is a large difference in the electron transport behavior between the In$_{0.53}$Ga$_{0.47}$As channel and In$_{0.52}$Al$_{0.48}$As buffer. It is proposed that the actual mechanism responsible for the high output conductance is a 2DEG carrier deconfinement effect, which causes the HEMT drain current to saturate prematurely. Semiclassical treatments of electron transport and high energy intervalley scattering are discussed to demonstrate the validity of this proposed mechanism.

7.2 Breakdown of the substrate conduction assumption

The assumption made in Chapter 2 was that substrate conduction was the main mechanism responsible for high output conductance. Thus reduction of the average substrate electric field, $\langle \vec{E} \rangle$, would reduce the ohmic current component (i.e., output conductance, $g_0$) of the saturated drain current. However, it has been shown from the MBE growth experiments that the unintentional doping concentration of the In$_{0.52}$Al$_{0.48}$As buffer was approximately $6 \times 10^{14}$ cm$^{-3}$ N-type, with a typical In$_{0.52}$Al$_{0.48}$As buffer layer thickness of 2500 Å. The In$_{0.52}$Al$_{0.48}$As buffer layer sheet charge density is then equal to $1.5 \times 10^{10}$ cm$^{-2}$, with a saturation velocity of approximately $1 \times 10^7$ cm/s [55]. This gives a maximum substrate saturation current of 2.4 mA/mm, which is between 30 and 50 times smaller than the experimental data described in Chapter 6. Since the 2DEG charge is confined by the conduction band discontinuity between the In$_{0.53}$Ga$_{0.47}$As channel and the In$_{0.52}$Al$_{0.48}$As buffer, carrier injection into the buffer from the 2DEG electron pool near the low transverse electric field, source end of the gate, is very unlikely. This suggests that the high excess drain saturation current observed in conventional highly doped surface In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMTs must result from a mechanism other than substrate conduction.

Though the substrate conduction mechanism for output conductance is not substantiated by the experimental data, the reduction of peak channel electric field
realized with the LCD structure has dramatically improved the HEMT output characteristics, in spite of the inadequate explanation. From Chapter 2, the number of 2DEG electrons which reach velocity saturation is defined by Equation 2.2.1. Since the position at which velocity saturation is reached (i.e., \( \vec{E} = \vec{E_C} \)) is very close to the source, \( V_C(x) \) is negligible in Equation 2.2.1, hence the total number of 2DEG electrons which conduct the drain current is controlled predominantly by the gate potential. Thus the resulting drain current must be saturated if all the 2DEG electrons travel at a constant, single valued saturation velocity, \( V_{Sat} \). This means that unless there is another source of carrier injection into the gated channel, the validity of the basic charge control model with a single saturation velocity must be questioned in this particular HEMT structure.

7.3 High electric field induced 2DEG deconfinement

Electron transport in semiconductors parallel to a heterointerface has been treated extensively in the literature on both Si Metal-Oxide-Semiconductor structures and compound semiconductor-semiconductor heterojunctions [56, 57]. Under a high electric field situation, electron transport must include not only the band structure, but the electron-electron scattering and multiple scattering as well [58]. Earlier work on MOS systems has shown that if the electron gas is treated as two-dimensional, the density of states is independent of energy and the scattering terms in the Boltzmann transport equation are greatly simplified [59]. Writing the Boltzmann equation symbolically:

\[
\left( \frac{\partial f}{\partial t} \right)_{\text{Elec. field}} + \left( \frac{\partial f}{\partial t} \right)_{\text{Collision}} = 0 \tag{7.3.1}
\]

where \( f \) is the distribution function, and can be expressed as \( f = f_o + k_E \cdot g_E(\varepsilon) \), where \( f_o \) is the thermal equilibrium, spherical part of \( f \), \( k_E \) is the component of \( k \) (i.e., wave vector) in the direction of the electric field, \( g_E(\varepsilon) \) is the drift term, and \( E \) is the carrier energy. By replacing the energy term with its two-dimensional average value, Equation
7.3.1 can be expressed as:

\[
(\frac{\partial f}{\partial t})_{\text{Collision}} - \frac{g_e(E)}{\hbar} (g_e(E) + \frac{d}{dE} g_e(E)) = 0 \quad (7.3.2)
\]

and

\[
g_e(E) = \frac{q\hbar}{m} \frac{E}{\tau} \frac{df_0}{dE} \quad (7.3.3)
\]

where \(\tau\) is the momentum relaxation time. Neglecting the relaxation terms due to surface roughness and surface ions, which are less significant in HEMT devices, the spherical symmetrical part, \(f_0\), of the distribution function can be defined and solved under strong electric fields. The solution of \(f_0\) is of the form (see Appendix C) [59]:

\[
f_0 = A \cdot e^{-F_{a,o}} \cdot e^{-G_{a,o}} \quad (7.3.4)
\]

where \(A\) is a normalization constant, and \(F_{a,o}\) and \(G_{a,o}\) are two characteristic scattering functions related to both acoustical and optical phonon modes under very strong electric field. When the average electron energy is lower than the optical phonon energy, only acoustical phonon scattering is allowed and \(f_0\) is near the thermal equilibrium Maxwellian distribution. This is still considered a two-dimensional distribution and transitions in a direction perpendicular to the heterointerface are impeded [59]. However, when the electron energy becomes higher than the optical phonon energy, the carrier can emit optical phonons and perpendicular momentum is conserved by the emitted phonons, thus the electron scattering can no longer be regarded as two-dimensional.

It has been shown in the AlGaAs/GaAs system, that as the 2DEG electrons are heated by strong electric fields to energies comparable to the conduction band discontinuity, \(\Delta E_C\), the electrons can scatter into the AlGaAs region [61, 62]. This perpendicular transfer (with respect to the heterointerface) of electrons in real space, rather than in k-space, has pronounced effects on the HEMT steady state current. These electrons can either go into the AlGaAs layer or spread much deeper into the GaAs buffer layer, where they gain or lose random energy from subsequent scattering.

In the case of \(\ln_{0.52}\text{Al}_{0.48}\text{As}/\ln_{0.53}\text{Ga}_{0.47}\text{As}\) HEMTs, the thin \(\ln_{0.53}\text{Ga}_{0.47}\text{As}\)
2DEG channel is sandwiched between layers of wide band gap $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ with parallel heterointerfaces. Because of the large conduction band discontinuity, $\Delta E_C$, associated with these heterointerfaces, a much higher electron energy is needed to overcome the electron confinement barriers (i.e., $\Delta E_C$), and initiate the high electric field induced real-space transfer. Because of the high electric field and very short $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel, the electrons travel nearly ballistically and they can reach an energy greater than $\Delta E_C$. When these hot electrons scatter with phonons, the hot electrons redistribute into energy bands over the full range of $\mathbf{k}$-space in the band structure, thus the intervalley scattering must be included in the transfer process.

Because of insufficient studies of the detailed energy band structure of $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ system, we have used the $\text{AlGaAs/GaAs}$ system as a prototype for the following discussion. Figure 7.3.1 shows the energy dependent phonon scattering rate as a function of electron energy in GaAs [63]. For electron energies between 0.036 and 0.3 eV, a constant scattering rate of 0.8 to $1.0 \times 10^{13}$ sec$^{-1}$ indicates the electron is in the ballistic regime and is scattered predominantly by optical phonon emission. When the electron energy reaches 0.3 eV, intervalley scattering becomes possible through deformation potential scattering [63], thus the scattering rate increases rapidly with electron energy. This shows that for an electron overshoot velocity in the order of $5 \times 10^7$ cm/s, the ballistic transport distance is only 500 Å before an electron gains enough energy to be scattered into the upper conduction band valleys. Because of the high density of states in the upper energy bands, intervalley scattering to the L and X valley minima by deformation potential scattering is very strong. In the case of a quarter-micron gate length FET, a conducting electron may travel ballistically at the beginning of its acceleration, but suffer intervalley scattering near the high field drain region.
Figure 7.3.1: Energy dependent phonon scattering rate as a function of electron energy in GaAs at 300K [63].

Figure 7.3.2 shows the calculated hot electron kinetic energy distribution in a 0.25 μm GaAs MESFET, calculated by Monte Carlo particle simulation [64], where intervally scattering is clearly observed in the high electric field region (i.e., at the drain side of the gate edge).
Figure 7.3.2: Distribution of the Kinetic energy, calculated by two-dimensional Monte Carlo simulation, indicating the hot electron interval scattering at the high field regime [64].

7.4 Premature Current Saturation (PCS)

The correlation between the high output conductance observed in conventional highly doped surface In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/InP HEMTs and associated peak channel electric field has been discussed in the early chapters. The reduction of peak channel electric field achieved with the LCD undoped surface structure significantly reduces the real-space transfer of hot electrons in the high field region, and is thus consistent with our experimental results. This effect is referred to as the 2DEG carrier deconfinement process, which has a strong effect on the carrier transport properties, as described in the previous section.
The real question remaining, then, is how does the 2DEG carrier deconfinement process effect the drain current saturation of \( \text{In}_{0.52}\text{Al}_{0.48}\text{As/In}_{0.53}\text{Ga}_{0.47}\text{As/InP} \) HEMTs? To assist our discussion, the transverse electric field profile under the gate and the band diagrams at both velocity saturation (i.e., \( \mathbf{E} = \mathbf{E}_C \)) and peak electric field (i.e., \( \mathbf{E}_{\text{peak}} \)), of an \( \text{In}_{0.52}\text{Al}_{0.48}\text{As/In}_{0.53}\text{Ga}_{0.47}\text{As} \) double barrier confined quantum well structure, are shown in Figure 7.4.1. The transverse channel electric field profile shown in Figure 7.4.1 (a) was constructed from PISCES simulations (Chapter 5). The 2DEG charge density at the point of velocity saturation (i.e., \( \mathbf{E}_C \)) is denoted as \( N_{\text{tot}} \), as shown in Figure 7.4.1 (b), which is the charge density allowed to sweep through the channel under the gate, and is mainly controlled by the gate potential (Equation 2.2.1). In the case of conventional high surface conductance HEMTs, the peak channel electric field (i.e., \( \mathbf{E}_{\text{peak}} \)) rapidly increases as the drain to source bias potential moves beyond \( \mathbf{E}_C \) further into the saturation region. The 2DEG carriers are then heated by this high channel electric field, thus transferring (i.e., deconfining) the 2DEG carriers from the \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) quantum well into the \( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \) buffer region. This process is shown in Figure 7.4.1 (c), where the deconfining process is most likely a two-step process. The heated electron first gains enough energy to transfer, through deformation potential scattering, from the \( \Gamma \) valley to the \( L \) valley in the quantum well. This \( L \) valley is about 0.55 eV above the \( \Gamma \) valley for \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \). The intervalley transfer is associated with electron relaxation and the increased scattering rate for phonons [63].

It should be emphasized at this stage that the electron scattering is no longer restricted to two-dimensions, as described in the previous section. Since the L-\( \Gamma \) valley energy difference of \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) (i.e., 0.55 eV) is higher than the conduction band discontinuity \( \Delta E_C \) (i.e., 0.52 eV), the electron can then scatter into the \( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \) buffer by a subsequent scattering event to accommodate any necessary momentum change to either the L or \( \Gamma \) valleys in the \( \text{In}_{0.52}\text{Al}_{0.48}\text{As} \).
Figure 7.4.1: Illustration of 2DEG carrier deconfinement process under strong electric field; (a): transverse electric field profile under the gate electrode, (b): band diagram at the position of velocity saturation, (c): band diagram at the position of peak channel electric field.
Although In$_{0.52}$Al$_{0.48}$As is a direct band gap material [15, 65], the direct-indirect bandgap cross-over is relatively close (at x=0.55) to the lattice-matched composition (x=0.48). Thus the L and Γ valleys of In$_{0.52}$Al$_{0.48}$As lie at comparable energies, particularly weighted by their densities of states. Due to the very strong electric field, the real-space transfer of hot electrons, from the L valley of In$_{0.53}$Ga$_{0.47}$As, is likely to occur to the L satellite valley of In$_{0.52}$Al$_{0.48}$As, rather than to the Γ valley. This satellite-satellite valley scattering has been predicted, by Monte Carlo simulation, in a similar quantum well structure of AlGaAs/InGaAs/GaAs [66].

In the ideal situation where all electrons are confined in the In$_{0.53}$Ga$_{0.47}$As channel, the In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT drain current density can be expressed as:

\[ J_{ds} = \sigma N_{tot} \upsilon_{Sat, InGaAs} \]  

(7.4.1)

If \( x \) is defined as the fraction of electrons that are scattered (i.e., transferred) into the In$_{0.52}$Al$_{0.48}$As buffer, then Equation 7.4.1 becomes:

\[ J_{ds} = q \left( 1 - x \right) N_{tot} \upsilon_{Sat, InGaAs} + q \left( x \right) N_{tot} \upsilon_{InAlAs} \]  

(7.4.2)

where \( \upsilon_{InAlAs} \) is a function of both \( \langle E \rangle_{InAlAs} \) and whether alloy clustering has occurred in the epitaxial growth. The saturation field for In$_{0.52}$Al$_{0.48}$As is about 3 times that of In$_{0.53}$Ga$_{0.47}$As, at which point, the velocity \( \upsilon_{InAlAs} \) becomes the saturation value, \( \upsilon_{Sat, InAlAs} \), which is approximately 0.5 x 10$^7$ (with clustering) or 1.4 x 10$^7$ cm/s (without clustering) [55]. Since the electron mobility and saturation velocity in In$_{0.52}$Al$_{0.48}$As are about one order of magnitude and 2 to 3 times lower, respectively, than the equivalent parameters in In$_{0.53}$Ga$_{0.47}$As, the saturation drain current is reduced from the high value predicted by Equation 7.4.1, to a lower value from Equation 7.4.2. It should be pointed out that the percentage of 2DEG electrons transferred to In$_{0.52}$Al$_{0.48}$As buffer, is a function of the In$_{0.53}$Ga$_{0.47}$As channel electric field \( \langle E \rangle \).

While \( \upsilon_{InAlAs} \) is a function of the buffer electric field \( \langle E \rangle_{InAlAs} \), which depends very much on the background impurity level or the density of deconfined 2DEG electrons which reside in the buffer region. This simple differential velocity argument between
the $In_{0.53}Ga_{0.47}As$ channel and $In_{0.52}Al_{0.48}As$ buffer (Equations 7.4.1 and 7.4.2), does not consider band bending at the channel-buffer interface due to the large number of injected (i.e., deconfined) electrons, which impedes the deconfinement process and tends to restore the drain current characteristics.

In Figure 7.4.2, we show three different I-V curves for comparative discussion. The ideal I-V curve is based upon the constant saturation velocity charge control model, which might be a reasonable model for the LCD HEMT where all of the electrons stay in the $In_{0.53}Ga_{0.47}As$ quantum well channel. For the highly doped surface (i.e., high drain conductance) HEMT, the drain current starts to "saturate" at a value lower than the ideal curve value, due to the smaller effective channel conductance (Equation 7.4.2) when carrier deconfinement begins. As the drain voltage increases further, both (x) and the buffer electric field increase, resulting in higher $In_{0.52}Al_{0.48}As$ electron velocity, $\nu_{InAlAs}$, and higher buffer layer conductance. Also the band bending at the buffer interface, due to the presence of deconfined electrons in the buffer, causes the deconfinement process to be self-limiting or even saturating. Thus the combined drain current (i.e., channel and buffer) increase asymptotically toward the ideal value at higher $V_{ds}$, until the electric field reaches the impact ionization breakdown threshold and the current increases rapidly with $V_{ds}$, as shown in Figure 7.4.2. This unusual drain current saturation behavior, caused by the high electric field induced 2DEG deconfinement process, is referred as Premature Current Saturation (PCS). This proposed current saturation model, however, is still preliminary and needs further detailed investigation. The low temperature buffer (LTB) approach, which drastically reduce buffer electron mobility, $\mu_{InAlAs}$, and velocity, $\nu_{InAlAs}$ [9, 10], has effectively eliminated the buffer conduction current, thus producing the drain current characteristic shown in Figure 7.4.2. Though the LTB has dramatically reduced $g_0$, the improvement in output conductance was achieved by compromising the overall drain I-V characteristics (i.e., $I_{dss}$ and $g_m$) [10], hence it does not lead to meaningful improvements in HEMT high frequency performance.
Figure 7.4.2: Comparative illustration of I-V characteristics between premature current saturation and low temperature buffer HEMTs, with reference to the ideal situation (i.e., charge control model with single valued saturation velocity).

7.5 Conclusion

The underlying device physics of the $\text{In}_{0.52}\text{Al}_{0.48}\text{As/In}_{0.53}\text{Ga}_{0.47}\text{As/InP}$ HEMT drain I-V characteristic has been investigated. Through examining the experimental evidence presented in previous chapters and basic electron transport theory, a model of premature current saturation (PCS) is proposed to explain the improvements in the output conductance achieved by the LCD HEMT design. The high output conductance observed in conventional $\text{In}_{0.52}\text{Al}_{0.48}\text{As/In}_{0.53}\text{Ga}_{0.47}\text{As/InP}$ HEMT design is caused by a rapidly increasing channel electric field near the drain, which results in hot electron induced 2DEG carrier deconfinement (i.e., real-space transfer), causing the drain current to saturate prematurely (i.e., incomplete saturation). This self-
consistent electron transport model for In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/InP HEMT has been successfully applied to explain the saturation observations in these devices.
Chapter 8

Conclusions

8.1 Conclusions

The main contributions made in this thesis have been in three areas: (A) Successful development of MBE growth of high quality \( \text{In}_{0.52}\text{Al}_{0.48}\text{As/In}_{0.53}\text{Ga}_{0.47}\text{As/InP} \) HEMT structures, (B) The successful development of Low Conductance Drain (LCD) HEMT structure to greatly reduce the high output conductance associated with \( \text{In}_{0.52}\text{Al}_{0.48}\text{As/In}_{0.53}\text{Ga}_{0.47}\text{As/InP} \) HEMTs, and (C) The development of the Premature Current Saturation (PCS) model and 2DEG deconfinement mechanism as explanation of the fundamental device physics behind HEMT operation under high electric fields.

It is clear that this work has significantly advanced the state-of-the-art HEMT technology, not only in the area of device or circuit performance, but also the understanding of fundamental \( \text{In}_{0.52}\text{Al}_{0.48}\text{As/In}_{0.53}\text{Ga}_{0.47}\text{As/InP} \) HEMT operation under high electric field. This study has indicated new directions of further enhancing the HEMT performance, namely the 2DEG channel electric field optimization by considering extrinsic device parameters and the development of HEMT heterostructures for better 2DEG confinement. Though the degree of influence may be different, this predictive 2DEG transport model developed in this study is undoubtedly applicable to all generic HEMT devices, such as AlGaAs/GaAs and AlGaAs/InGaAs/GaAs Pseudomorphic HEMTs.

The state-of-the-art HEMT device and millimeter wave monolithic integrated circuit (MMIC) performance achieved during the course of this study have greatly enhanced the confidence and assured the practical values of this work. It is my sincere desire to further my involvement in this exciting research and development area, and I hope as
well as expect, that the future HEMT technology will benefit from this present thesis.

8.2 Suggestions for future work

Based on the concepts of optimizing the 2DEG channel electric field in prevention of carrier deconfinements, and enhancing the possibility of ballistic transport in ultra short channel HEMTs. Three categories of suggested future works are given here:

(1) Device structure engineering: Modify the conventional HEMT structure by inserting an extra wide band gap buffer barrier, which repels the hot electrons from escaping out of the confinement quantum well. This enhanced buffer barrier arrangement will confine the 2DEG electrons to stay in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel, thus maintaining the superior electron transport properties for its best high frequency performance.

(2) Double recess structure: This is the most preferred structure for the Low Conductance Drain (LCD) design. Though the double recess process of micron size feature has been demonstrated, the application of sub-quarter-micron feature is not well established. Since the recess characteristic distance $L_{dc}$ should be in the range from couple hundred to thousands of angstroms, the process control with overlay alignment becomes practically impossible. A novel way of doing this fine line double recess remains to be developed.

(3) Quantitative modeling of 2DEG transport: Better understanding of the electron transport properties in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ are required for accurate simulation and modeling purposes. The utilization of two-dimensional device simulator with heterojunction handling capabilities will become extremely useful in the future to provide quantitative as well as conceptual evidence on new HEMT design, which is a never ending task in advancing the high frequency device technology.
appendix a

primitive simulation of inp hfmt

$*** define rectangular grid ***$

mesh
  nx = 100
  ny = 21
  rect diag.fli outf = trd

x.m
  y = 0
  r = 1.

x.m
  y = 100
  r = 1.

y.m
  x = 1
  r = 0.

y.m
  x = .0002
  r = 1.

y.m
  x = .01
  r = 1.

y.m
  x = .025
  r = 1.

y.m
  x = .035
  r = 1.

y.m
  x = 21
  r = 1.2

$*** regions ***$

region
  num = 1
  ix.l = 1
  ix.h = 23
  iy.l = 1
  iy.h = 3
  GaAs

region
  num = 2
  ix.l = 57
  ix.h = 100
  iy.l = 1
  iy.h = 3
  GaAs

region
  num = 3
  ix.l = 23
  ix.h = 57
  iy.l = 1
  iy.h = 3
  insulator

region
  num = 4
  ix.l = 1
  ix.h = 100
  iy.l = 3
  iy.h = 6
  GaAs

region
  num = 5
  ix.l = 1
  ix.h = 100
  iy.l = 6
  iy.h = 8
  GaAs

region
  num = 6
  ix.l = 1
  ix.h = 100
  iy.l = 8
  iy.h = 21
  GaAs

$*** electrodes ***$

elec
  num = 1
  ix.l = 1
  ix.h = 5
  iy.l = 1
  iy.h = 1

elec
  num = 2
  ix.l = 25
  ix.h = 55
  iy.l = 3
  iy.h = 3

elec
  num = 3
  ix.l = 95
  ix.h = 100
  iy.l = 1
  iy.h = 1

select
  num = 4
  ix.l = 1
  ix.h = 100
  iy.l = 21
  iy.h = 21

$*** dopig ***$

doping
  region = 1
  unif
  conc = 4e18
  n.type
  outf = hemtdop

doping
  region = 2
  unif
  conc = 4e18
  n.type

doping
  region = 4
  unif
  conc = 5e14
  n.type

doping
  region = 5
  unif
  conc = 2e18
  n.type

doping
  region = 6
  unif
  conc = 5e14
  n.type

$*** model and material ***$

contact
  num = 2
  workf = 4.6
  surf.rec

symb
  newton carriers = 1

method
  itlimit = 25
  xnorm = true
  autonr

mater
  num = 1
  perm = 3.0
  mun = 4000
  vsat = 1.2e7

mater
  num = 2
  perm = 13.0
  mun = 4000
  vsat = 1.2e7

mater
  num = 3
  perm = 1.0

mater
  num = 4
  perm = 13.0
  mun = 1000
  vsat = 6.0e6

mater
  num = 5
  perm = 13.0
  mun = 10000
  vsat = 2.0e7

mater
  num = 6
  perm = 13.0
  mun = 1000
  vsat = 6.0e6

models
  temp = 300
  fldmob
cn = mob

$*** bias ***$

solve
  init
  v1 = 0.0
  v2 = 0.0
  v3 = 0.0
  outf = hemtii

solve
  v1 = 0.0
  v2 = 0.2
  v3 = 0.0
  vstep = 0.2
  nstep = 1
  elect = 2
  outf = hemtii

log
  outf = ivlog

solve
  v1 = 0.0
  v2 = 0.4
  v3 = 0.1
  vstep = 0.1
  nstep = 9
  elect = 3
  outf = hemtio

solve
  v1 = 0.0
  v2 = 0.4
  v3 = 1.2
  vstep = 0.2
  nstep = 9
  elect = 3
  outf = hemtio

$contour plot$
load
  infile = hemtii

$plot.1d j.elec x.axis = v3
y.axis = i3$
plot.2d
  boundary
  no.top
contour
  poten = -3.0
  max = 3.0
  del = 0.2
pause
end

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**Appendix B**

**MESA LAYER**

1. Wafer clean  
   TCE, ACE, IPA, N₂ dry
2. Dry bake  
   130°C bake
3. Resist spin  
   Shipley 1370 @ 5000 rpm
4. Softbake  
   80°C bake
5. Expose (DUV)  
   Mesa mask
6. Develop  
   Shipley 351 Dev. 5:1, D.I. rinse, N₂ dry
7. Inspect  
   Optical inspection
8. Mesa etch  
   Selected etchant
9. Elec. test  
   Test for mesa isolation
10. Dektak  
    Measure mesa height
11. Resist strip  
    ACE, IPA, D.I. water rinse, N₂ dry

**OHMIC CONTACT METALLIZATION**

1. Spin clean  
   Spin at @ 3500 rpm, spray with ACE while spinning, rinse with IPA
2. Dry bake  
   130°C bake
3. Resist spin  
   Shipley 1370 resist @ 5000 rpm
4. Prebake  
   70°C bake
5. Chloro. soak  
   Chlorobenzene soak @ room temperature
6. Softbake  
   70°C bake
7. Expose  
   Source-Drain ohmic mask
8. Develop  
   Shipley 351 Dev. 5:1, D.I. rinse, N₂ dry
9. Inspect  
   Optical inspection
10. Plasma ash  
    100W power
11. Clean  
    BOE dip, D.I. water rinse, N₂ dry
12. Metallization  
    AuGe/Ni/Au
13. Liftoff  
    ACE soak, ultrasonic, IPA rinse, N₂ dry
14. Inspect  
    Second optical inspection
15. Alloy  
    350°C furnace anneal

**GATE FORMATION**

1. Spin clean  
   Spin at @ 3500 rpm, spray with ACE while spinning, rinse with IPA
2. Dry bake  
   180°C bake
3. Resist spin  
   Spin Isofine PMMA resist at low speed
4. Softbake  
   170°C bake (Hotplate)
5. Expose  
   Gate exposure with E-beam
6. Develop  
   X-cycle spray develop
7. Inspect  
   Optical inspection
8. Clean  
   H₂O:NH₄OH dip, cold D.I. water rinse
9. Gate recess  
   Cold etchant, D.I. water rinse, N₂ dry
10. Clean  
    H₂O:NH₄OH dip, cold D.I. water rinse
11. Metallization  
    Ti/Pt/Au E-beam evaporation
12. Liftoff  
    TCE boil, TCE rinse, ACE rinse, IPA rinse, N₂ dry
13. Inspect  
    Second optical inspection
Appendix C

Two-dimensional electron transport in high electric field

In a two-dimensional system, the Boltzmann transport equation is expressed:

\[ \left( \frac{\partial f}{\partial t} \right)_{\text{Elec. field}} + \left( \frac{\partial f}{\partial t} \right)_{\text{Collision}} = 0 \]  \hspace{1cm} (C-1)

where \( f \) is the distribution function, and can be expressed as \( f = f_0 + k_E g_E(E) \), where \( f_0 \) is the thermal equilibrium, spherical part of \( f \), \( k_E \) is the component of \( k \) (i.e., wave vector) in the direction of the electric field, \( g_E(E) \) is the drift term and \( E \) is the carrier energy. By replacing the energy term with its two-dimensional average value, Equation 7.3.1 can be expressed as:

\[ \left( \frac{\partial f}{\partial t} \right)_{\text{Collision}} - \frac{\hbar}{\tau} \left( g_E(E) + E \frac{d g_E(E)}{dE} \right) = 0 \]  \hspace{1cm} (C-2)

and

\[ g_E(E) = \frac{q \hbar E}{m} \tau \frac{d f_0}{dE} \]  \hspace{1cm} (C-3)

where \( \tau \) is the momentum relaxation time. Now we need to calculate the collision operator for scattering by acoustical and optical phonons, which can written as:

\[ \left( \frac{\partial f_0}{\partial t} \right)_{\text{Collision}} = - \int \left( f_0(k) P(k \cdot -k') - f_0(k') P(k' \cdot k) \right) \cdot d^2 k' \]  \hspace{1cm} (C-4)

where \( P(k \cdot -k') \cdot d^2 k' \) represents the probability per unit time that a carrier with \( k \) is scattered into the element of area \( d^2 k \) at \( k' \). By inserting the matrix elements for acoustical and optical (intervalley) phonons into Equation C-4, we obtain in cylinder coordinates the collision operator for acoustical phonon scattering:

\[ \left( \frac{\partial f_0}{\partial t} \right)_{\text{ac}} = \left( \frac{2m_m Z_A^2}{\hbar^2 p} \right) \frac{d}{dx} \left[ x \left( \frac{\partial f_0}{\partial x} + f_0 \right) \right] + S_A \frac{d}{dx} \left[ x \left( \frac{\partial f_0}{\partial x} + f_0 \right) \right] \]  \hspace{1cm} (C-5)

where \( Z_A \) is the acoustical surface deformation potential in eV, \( p \) is the areal mass density, \( x = E/k_B T \), \( S_A = \frac{2m_m Z_A^2}{\hbar^2 p} \), \( k_B \) is the Boltzmann constant. For optical phonons:
\[
\left( \frac{\partial f_0}{\partial t} \right)_{opt} = \sum_{R} S_R((N_R+1) f_0(x+x_R) - N_R f_0(x) \right) \\
+ \theta(x+x_R)[N_R f_0(x-x_R) - (N_R+1) f_0(x)]]
\]

(C-6)

where \( \theta \) is the step function, \( x_R = h\omega R/k_BT \), \( N_R \) is the phonon occupation number. Combining Equations C-5 and C-6, we can then solve \( f_0 \) under hot-electron-high field condition. If the electric field is not high enough and only acoustical phonon scattering is allowed, the solution for \( f_0 \) is:

\[
f_0 = A \exp[-x/(1+E^2/E_0^2)]
\]

(C-7)

where \( E_0^2 = mk_BT S_A/q^2\tau_{ac} \). A is a normalization constant. This shows that \( f_0 \) is a Maxwellian distribution. It is thus concluded that the electron transport is confined in two-dimensions, since in three dimensions, the distribution function is not Maxwellian even for acoustical scattering alone.

At very high electric field, the electron mean energy can be larger than the optical phonon energy, then the solution for \( f_0 \) becomes:

\[
f_0 = A \exp[-S_Rx_R/(S_A - S_{ARG}(x>x_R))] \exp[S_x x/(S_R - S_{ARG}(x>x_R))]
\]

(C-8)

where \( S_{ARG} = -q^2 E^* \tau_{ac}/mk_BT \), A is again a normalization constant. In the validity range of Equation C-8 where the distribution function is no longer Maxwellian, all subbands are populated due to very strong electric fields, and the electron scattering cannot be regarded as two-dimensional anymore.
References


Thompson, L. E. Larson, S. E. Rosenbaum and M. J. Delaney, "AllnAs-GaInAs
HEMTs utilizing Low Temperature AllnAs Buffer Grown by MBE", IEEE Elect.
Temperature Buffer AllnAs/GalnAs on InP HEMT Technology for Ultra High Speed


1974.


Discontinuity for InAlAs/InGaAs Heterojunction", J. Appl. Phys., Vol. 55, No. 8,

[18] M. A. Littlejohn, J. R. Hanser and T. H. Glisson, "Velocity-Field Characteristics of

[19] A. Cappy, B. Carnez, R. Fauquembergues, G. Salmer and E. Constant,
"Comparative Potential Performance of Si, GaAs, GaInAs, InAs Submicrometer-


