HIGH SPEED, LOW DRIVING VOLTAGE VERTICAL CAVITY GERMANIUM-SILICON MODULATORS FOR OPTICAL INTERCONNECT

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I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

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Abstract

Information processing requires interconnects to carry information from one place to another. Optical interconnects between electronics systems have attracted significant attention and development for a number of years because optical links have demonstrated potential advantages for high-speed, low-power, and interference immunity. With increasing system speed and greater bandwidth requirements, the distance over which optical communication is useful has continually decreased to chip-to-chip and on-chip levels. Monolithic integration of photonics and electronics will significantly reduce the cost of optical components and further combine the functionalities of chips on the same or different boards or systems. Modulators are one of the fundamental building blocks for optical interconnects. Previous work demonstrated modulators based upon the quantum confined Stark effect (QCSE) in SiGe p-i-n devices with strained Ge/SiGe multi-quantum-well (MQW) structures in the i region. While the previous work demonstrated the effect, it did not examine the high-speed aspects of the device, which is the focus of this dissertation.

High-speed modulation and low driving voltage are the keys for the device's practical use. At lower optical intensity operation, the ultimate limitation in speed will be the RC time constant of the device itself. At high optical intensity, the large number of photo generated carriers in the MQW region will limit the performance of the device through photo carrier related voltage drop and exciton saturation. In previous work, the devices consist of MQWs configured as p-i-n diodes. The electric field induced absorption change by QCSE modulates the optical transmission of the device. The focus of this thesis is the optimization of MQW material deposition, minimization of the parasitic capacitance of the probe pads for high speed, low voltage and high contrast ratio operation. The design, fabrication and high-speed characterization of devices of different sizes, with different bias voltages are presented. The device fabrication is based on processes for standard silicon electronics and is suitable for mass-production. This research will enable efficient transceivers to be monolithically integrated with silicon chips for high-speed optical interconnects. We demonstrated a

modulator, with an eye diagram of 3.125GHz, a small driving voltage of 2.5V and an f_{3dB} bandwidth greater than 30GHz. Carrier dynamics under ultra-fast laser excitation and high-speed photocurrent response are also investigated.

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Chapter 1 Introduction

1.1 Interconnects

Interconnects are the communication system that provides channels to transmit data. In conventional data networks and intra-/interchip data links, interconnects have continued to scale in complexity and bandwidth for the past fifty years. The limitation of metal interconnects in terms of loss, dispersion, crosstalk and fundamental speed limits are becoming increasingly obvious as interconnect density increases. This naturally leads to the development of optical interconnects, especially based on a Si photonics technology platform. This is because of the low cost, high performance and CMOS compatible processes of electronic-photonic integration. A gradual transition of electrical to optical technology in the interconnect field is taking place. This trend started with longer links and is expanding to short range applications. These applications areas for optical interconnects include high-performance computing, data centers, mobile-to-server interconnects and desktop computers.

Transistor densities that can be achieved inexpensively on an integrated circuit will continue to double every two years for some time into the future [1]. This trend has continued for more than half a century and is still dominating the semiconductor industry today. As it appears on the ITRS roadmap, electrical interconnects are increasingly becoming the bottleneck for today's integrated circuit operation. Among a number of possible solutions to overcome the challenge, optical interconnects are a very viable candidate to be the next generation of interconnect technology for integrated circuits. Their advantages and limitations have been carefully examined in the past few years [2-7].

We can divide the interconnects into two different levels, depending on architecture: inter-chip (off-chip) interconnects and intra-chip (on-chip) interconnects.

1.1.1 Off-Chip Interconnects

The term "inter-chip interconnects" normally refers to short range optical communication systems with a range of less than 100 meters. That includes last-mile transmission, storage area networking and other applications. The interconnect hierarchy in the off-chip interconnect domain (< 100m) is typically categorized into the following three levels: cabinet level (1 − 100m), backplane level between boards (10cm – 1m), chip-to-chip on a board (< 10cm) [8].

There are several reasons why electrical interconnects are commonly used for these interconnects: (1) The infrastructure already exists; (2) Low cost deployment (3) Speed and signal integrity requirements could previously be satisfied for most applications. However, when the signal is transmitted at several gigahertz in electrical interconnects, several issues emerge: (1) parasitic effects lead to serious electromagnetic interference (EMI) and susceptibility problems, which damage the signal integrity; (2) Dielectric material leakage does not scale with the geometry of the line; (3) Metal line scaling causes more power consumption (4) The theoretical maximum capacity of electrical lines will soon be reached; (5) Signal latency increases as the operating frequency increase.

Optical interconnect platforms are providing solutions for 10G Ethernet and storage networks [9], board level and chip-to-chip interconnects [10]. Fig 1.1 (a) shows the Intel QuickPath architecture as an example of the off-chip optical interconnect structure. DRAM is the memory unit, IOH is the input/output hub. This architecture is scalable in terms of operating speed and bandwidth [11]. If an efficient optical communication solution based on CMOS-compatible processes exists, it will be economically viable to be integrated in the core chips (such as chipset or CPU) instead of merely to be used for I/O networking chips, and it will eventually be the solution for all inter-chip interconnects. [12] Fig 1.1(b) shows the layout of an

inter-chip optical interconnect system developed by HP, all the black dies include chips, memory units, caches and other computational devices. They are connected by an optical communication loop and powered by an off-chip laser.

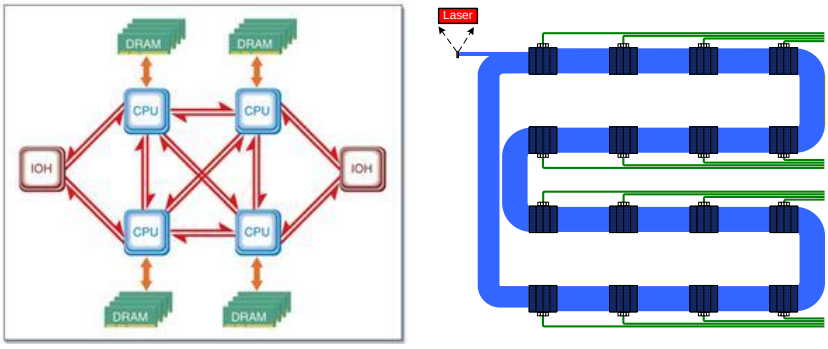


Figure 1.1(a) Intel QuickPath interconnect architecture (b) HP layout of the off-chip optical interconnect

1.1.2 On-Chip Interconnects

Intra-chip interconnects are used for signaling, propagation, and networking on the same chip. Fig. 1.2 shows a cross-sectional SEM view of a CMOS chip. Transistors are fabricated at the bottom of the multilayer structure. There are local, semi-global and global interconnects; metals from different layers are connected by vias. As the transistor density kept increasing, the complexity of the interconnect layout and number of layers increased as well.

CMOS devices at the bottom of the chip are connected by local and semi-global wires in the middle levels and by global wires in the top levels. Because metal wires have high resistance and relatively low inductance, the delay of intra-chip interconnects is RC-limited, where C is the MOS capacitance in the loading stage, and R could be the resistance of metal interconnects, the channel resistance of the MOS device in the driving stage, or the combination of both.

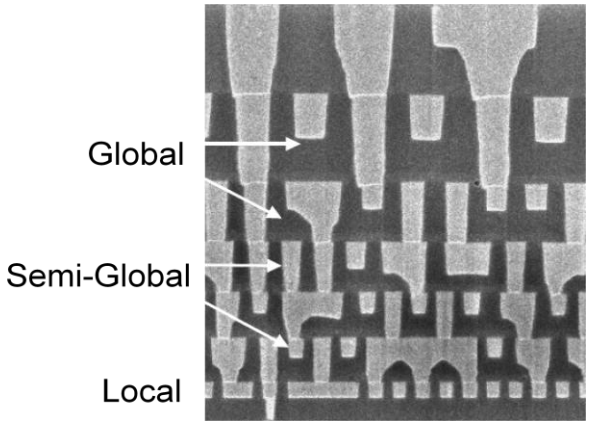


Figure 1.2 Cross-sectional of a CMOS chip. [13]

Fig. 1.3 shows the trends of delay versus technology node predicted by the International Technology Roadmap for Semiconductors (ITRS). The delays of devices and local interconnects are reduced as devices scale, but the delays of global wires keep increasing [14]. The key reason why global interconnects cannot share the same advantages Moore's law brings to all other components is because the cross-sectional area of wires are reduced with each technology node, but the length is almost the same, and hence the resistance and delay increase dramatically. In addition, the skin-depth effect at high frequency further increases the resistivity of the wires.

Even though repeaters [15, 16] are used to segment the global wire into several shorter sections, the delay cannot be effectively reduced when the technology node reaches the sub 50-nm regime. More importantly, the power consumption from repeaters increases dramatically. This imposes a serious limitation for future CMOS technology to keep using metal global interconnects for signaling and clocking. Low power, low cost, integrated optical components need to be developed for future interconnects.

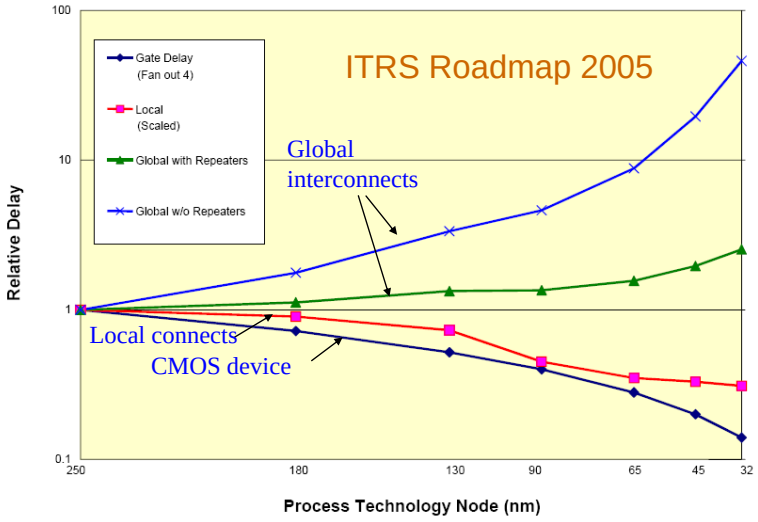


Figure 1.3 Relative delay versus technology node for gate, local interconnects, and global interconnects with and without repeaters

1.2 Optical Interconnect Systems

In order to realize high-speed inter-chip or intra-chip interconnects, nanophotonics would be the best replacement for electrical interconnects if low cost and integration can be achieved. This has multiple advantages: (1) Low power: It is generally considered that power consumption in the data links will be critical factor for computation speed of computers. When devices scale down and circuit operation speed increases, the traditional electrical interconnects will consume more power than the system can handle. Light traveling in a proper medium, such as fibers or silicon waveguides, has nearly zero power loss over the distance ranges where electrical interconnects still exist (< 1 mile), (2) High bandwidth: An electrical wire is a low pass filter and will limit the bandwidth of data transmission. At high frequency, the current takes the path of least inductance which is primarily on the surface of a transmission line, which is known as the "skin effect" This will decrease the conductance and increase attenuation. This frequency-dependent attenuation due to the skin effect causes the signal pulse to spread out, and leads to inter symbol interference (ISI). An optical light-wave is an electromagnetic wave with bandwidth as high as 200THz. It can carry a signal without changing its frequency or propagation and it is

immune to interference. (3) Cross talk free: An electrical wire acts as a good antenna at high frequencies, and it broadcasts its signal to adjacent wires through inductive and capacitive coupling between transmission lines. At high frequency, electromagnetic interference (EMI) will limit the density of electrical interconnects. Optical signals, on the other hand, are inherently immune to EMI. They don't detect and generate RF signals and their wavelength multiplexing capability is strong [17].

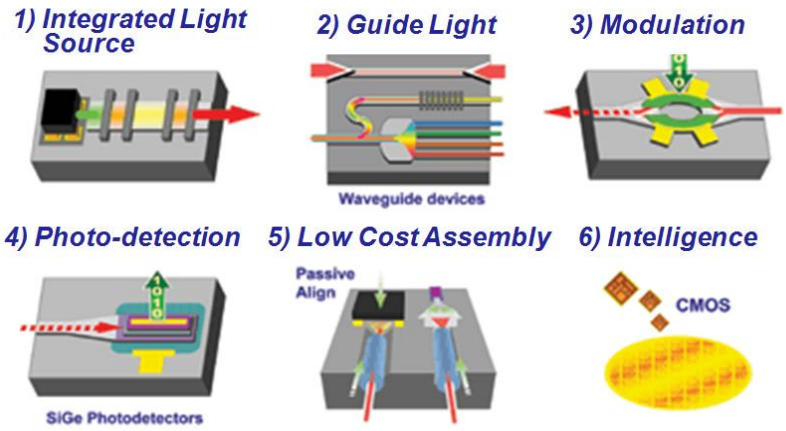


Figure 1.4 Optical interconnect system and building blocks [11]

Optical interconnect systems consist of four parts: light source, waveguide, modulation and photo-detection as shown in Fig. 1.4. The light source can be either an off-chip or on-chip laser. The modulator can be an electro-refractive Mach-Zehnder modulator, or an electro-absorptive surface normal or waveguide modulator. The carrier channels can be silica fibers, free-space air, or waveguides. Existing Si waveguide technology is based on SiGe/Si or silicon-on-insulator (SOI) [18, 19]. The detectors can be p-i-n diodes (low noise, unity responsivity), metal-semiconductor-metal (MSM) diodes (short response time), or avalanche photodiodes (APDs). Group-IV materials, such as silicon or germanium, have already been used as photodetectors [20]. There is also mature technology for optical carrier channels and receivers based on silicon-compatible technology. The key obstacle to realize optical interconnects is the transmitter. Prior to recent work [12], there was no efficient Si-based modulation mechanism and this function was only implemented by

expensive III-V compound semiconductor devices. Thus while the optical interconnect systems were promising, there was virtually no means to implement them for short-distance inter-chip or intra-chip communications.

Modulators are favored instead of direct-driven lasers for several reasons. (1)There is no efficient light emission in group IV materials yet. Silicon and germanium are indirect band-gap and tin is a semi-metal. It is hard to see a path to find a reliable group IV laser device today. (2) In order to modulate lasers at high bit rates, they must be pre-biased and driven at current densities well above threshold, which consumes high power and leads to performance degradation and failure [21]. (3) The heat generation from lasers is undesired for CMOS chips. The temperature variation in CMOS chips also causes wavelength shifts and this instability can prohibit precise channel allocations for multiple wavelength multiplexing in the same medium, such as wavelength-division-multiplexing (WDM) schemes. (4) It is very hard to incorporate a large number of lasers on a single chip. The complexity of the fabrication process will increase the cost dramatically. So we prefer to use on-chip modulators as the solution for transmitters and modulate the light coming from an off-chip continuous-wave (CW) laser.

1.3 Research on Optical Modulators

Typical modulators can be categorized as amplitude modulated or phase modulated. In practical applications, amplitude modulation is normally used, because it is hard for photo detectors to distinguish phase change. The studies of different modulation mechanisms and recent advances on silicon based modulators are introduced below.

1.3.1 Modulation Mechanism Study

1.3.1.1 Thermo-Optic Effect

The thermo-optic effect is the thermal modulation of the refractive index of a material. The modulation of the refractive index of a material depends on its thermo-optic

coefficient α and can be expressed as $n(T)=n_0+\alpha T$. In a modulator, thermal optical modulation is typically applied using a Mach-Zehnder (MZ) structure. When two light beams pass through the two arms of the MZ structure, one of the arms can be heated, which changes the index, leading to different optical path lengths. One of the beams will change accordingly. Therefore the superposition of the two beams at the other end will be modulated. Si MZ modulators based on SOI have been studied extensively [22-24]. The disadvantage of this structure is the high power consumption and slow transition time. (~10ns)

1.3.1.2 Electro-Optic Effect

The change of a material's refractive by an electric field is called the electro-optic effect. When the refractive index depends linearly on electric field, it is called the Kerr effect; if the relationship is quadratic, it is called the Pockels effect. The first mature technology using this effect was in lithium-niobate modulators [25]. The electro-optic effect is relatively weak, so another stronger effect was studied for high-speed operation [26-28]. The MOS capacitor on SOI was used. The refractive index is tuned using carrier injection in MOS transistors in a MZ structure. Ring structures have been thoroughly studied as well [29].

1.3.1.3 Electroabsorption Effect

The absorption coefficient in a material can be changed when the electric field applied across it is changed. This is called the electroabsorption effect, which includes the Franz-Keldysh effect [30-31] and the quantum-confined Stark effect (QCSE) [32-33]. The QCSE is widely used in high-speed optical modulation applications today [34-35]. Much work has been done in III-V based materials before the first QCSE in SiGe was observed in 2005 [36-41].

1.3.2 Previous work on high-speed Si based modulator

A Mach-Zehnder interferometer using the electro-optic effect was developed by Intel in 2005. Recently, Intel has demonstrated high-speed performance with a 10Gbps

eye diagram and small signal modulation with a 30GHz 3dB bandwidth [42]. The contrast ratio is higher compared to prior devices, and the transverse size is small, leading to even higher-speed possibilities. These devices are also completely CMOS compatible. The major issue for these devices is that they are too long (~11mm), leading to high power consumption, and it is very hard to bring a high-speed RF signal onto the device. Device design and fabrication are thus very complicated.

The ring structure [29] based on SOI has a smaller size at roughly ~12 μm in diameter. This is three orders of magnitude smaller than the MZ modulator. A ring resonator modulator operating at 1.5GHz has been demonstrated with high contrast ratio. The disadvantages of the structure are the large power consumption, high voltage requirement, narrow bandwidth and thermal sensitivity. Because the modulator needs a high quality-factor (Q ~ tens of thousands) resonator, the result is a very narrow optical bandwidth and severe thermal instability.

A key question is therefore whether germanium could produce strong, high-speed modulation using the QCSE. Germanium, like silicon, is an indirect gap semiconductor, but unlike silicon, it has a useful direct band gap only slightly higher in energy than the indirect band gap. However, modest QCSE was been observed in indirect gap AlGaAs [37-38].

Previous efforts to find mechanisms such as the QCSE in Si/Ge structures were largely unsuccessful. SiGe/Si quantum wells with type-I alignment (electron and hole minima in the same material layer) show either no QCSE [39] or relatively inefficient effects [40-41]. Strained SiGe/Si quantum wells on relaxed SiGe buffers and Ge/Si quantum dots on Si substrates, with type-II band alignment (electron and hole energy minima in different layers), can exhibit large shifts of optical transitions with electric field, but have relatively low absorption associated with the shifted transitions.

Another approach to SiGe waveguide modulators is based upon the Franz-Keldysh effect [44]. Waveguide structures using the Franz-Keldysh effect provide an easy means to control the extinction ratio and because the device has small dimension, it has low power consumption. Using SiGe material, the device is compatible with

CMOS processes. This device has so far achieved a limited small signal 3dD bandwidth of 1.2GHz without large signal measurements being done. A relative serious limitation is that a rather high bias voltage (>10V) was needed to achieve the required band edge shift.

1.4 Organization

The dissertation reports the study of high-speed germanium-silicon electroabsorption modulators aiming for optical interconnects with CMOs compatible, mass-producible fabrication processes. Chapter 2 discusses the theoretical background for electroabsorption effects, as well as SiGe properties and previous SiGe electroabsorption approaches. Chapter 3 presents the Ge/SiGe quantum well structure design which utilizes the unique band structure of Ge for the electroabsorption effect. The effects of structural parameters are simulated by the resonant tunneling method. Chapter 4 discusses SiGe growth, by chemical vapor deposition, and material characterization. High-quality Ge quantum wells grown on silicon substrates were demonstrated. Chapter 5 presents the device fabrication processes and reports experimental measurement results. The first high-speed QCSE was observed in group-IV materials. Finally, Chapter 6 summarizes this dissertation and suggests several future directions for further scientific and engineering advances

Chapter 2 Background

2.1 Absorption in Semiconductors

2.1.1 Interband Absorption

The operation of optical devices is strongly related to upward and downward transitions of carriers between energy bands. These transitions result in optical absorption and emission of light. The absorption of a photon results in the transition from a lower energy state to a higher energy state, with or without the assistance of phonons. For the transition, the energy and the momentum conservation rules always have to be satisfied.

The energy-momentum diagrams of direct and indirect transitions are shown in Fig. 2.1 (a) and (b). In Fig. 2.1 (a), electrons and holes are at the zone center of the k-E band structure. At k=0, when a photon with larger energy than the band gap passes through the material, it will excite an electron from the valence band to the conduction band. The absorption coefficient can be written as:

$$\alpha = A^* \sqrt{h\upsilon - E_g} \tag{2.1}$$

α is the absorption coefficient, a function of the light frequency; ν is the light frequency; h is Planck's constant (hν is the energy of a photon with frequency ν); E_g is the band gap energy, A* is a frequency-independent constant, which can be written as

$$A^* = \frac{q^2 x_{vc}^2 (2m_r)^{3/2}}{\lambda_0 \epsilon_0 a^3 n} \tag{2.2}$$

where m_r is the reduced effective mass; q is the elementary electron charge; n is the (real) index of refraction; ε_0 is the vacuum permittivity; x_{vc} is a "matrix element",

with units of length and a typical value the same order of magnitude as the lattice constant. The formula is only valid for photons with energy larger than the band gap. It only includes band-to-band absorption.

An indirect band gap transition is shown in Fig. 2.1(b). Holes are located at global minimum energy at the zone center of k-E band structure. However, the global minimum for electrons in the conduction band is not at the zone center. That means electrons and holes do not have the same k-momenta. When a photon with energy larger than the band gap passes through the material, a phonon needs to be absorbed to complete the absorption. This greatly reduces the transition probability and therefore leads to a low absorption coefficient. The coefficient can be written as:

$$\alpha = \frac{(h\upsilon - E_g + E_p)^2}{\exp\left(\frac{E_p}{kT}\right) - 1} + \frac{(h\upsilon - E_g - E_p)^2}{1 - \exp\left(-\frac{E_p}{kT}\right)} \tag{2.3}$$

E_p is the energy of the phonon that assists in the transition; k is Boltzmann's constant; T is the thermodynamic temperature.

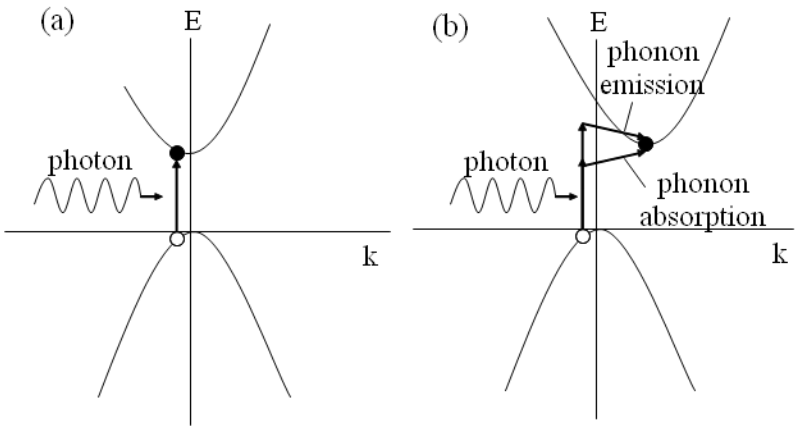


Figure 2.1: (a) Direct band absorption at zone center. (b) Indirect band absorption with phonon assistance.

2.1.2 Exciton Absorption

In semiconductor materials, especially in intrinsic regions where the screening effect of free carriers can be neglected, electrons and holes produced by absorption of a photon of near-bandgap energy pair to form an exciton. An exciton is basically a bound state of an electron and a hole. The binding energy of the exciton is analogous with that of the Bohr atom for an impurity center with quantized states.

Excitons in bulk semiconductors are called free excitons or Mott-Wannier excitons and are usually only observed at low temperatures (See, e.g., [45-46]). The binding energy can be decided by the Rydberg equation

$$E_{3\text{–}D,\,ex}^{n} = \frac{-m_r^* q^4}{2(4\pi\varepsilon_r\varepsilon_0\hbar)^2}\frac{1}{n^2} = \frac{E_B}{n^2} \tag{2.5}$$

where q is the elementary electron charge, m^*_r is the reduced effective mass of the exciton, $\hbar$ is the reduced Planck constant, n is the quantum number (a positive integer), $\varepsilon_r\varepsilon_0$ is the permittivity, and E_B is the Rydberg binding energy. The exciton binding energies for bulk Si, Ge, and GaAs are 14.7 meV, 4.15 meV, and 4.2 meV respectively [47]. For bulk semiconductors, excitons were not observed in semiconductors until epitaxial techniques enabled the growth of very pure crystals which are exactly neutral. If an electric field is applied it can ionize the impurities, and the additional charge modifies the band-edge potential. This is seen in the experiments where the slope of the absorption edge can be changed by tuning the applied electric field. Moreover, the ionized carriers screen the Coulomb interaction between the electrons and holes. This can inhibit or even prevent the formation of the excitons. The diameters of excitons are typically in the order of 10 nm; thus an electric field of ~ 10^4 V/cm can ionize them and make the absorption peaks broaden or disappear.

In quantum well systems, the electrons and holes are confined in the well regions and also have 2-D gas behavior through the well plane. Instead of Bohr atom type behavior, the binding energy in an ideal 2-D scenario can be written as [46]

$$E_{2-D,\ ex}^{n} = \frac{E_B}{(n-\frac{1}{2})^2}, \tag{2.6}$$

By comparing equations 2.5 and 2.6 it can be seen that for the same n-state, the 2-D exciton energy will be larger than the 3-D counterpart. Due to the concentration of the density of states, the quantum confinement also increases the absorption coefficients and therefore the 2-D exciton can be detected at room temperature [49]. The relationship of 3-D exciton, 2-D exciton and bulk absorption can be compared in Fig. 2.2.

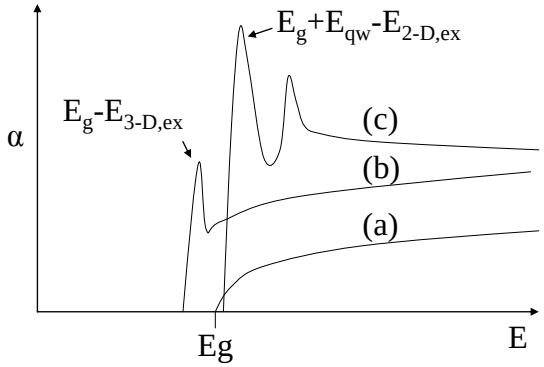


Figure 2.2: Absorption spectra of the same material: (a) no exciton (b) 3-D excitons (c) 2-D excitons confined in the quantum well. (Not to scale) [12]

When a semiconductor material has impurities like donors and acceptors, they will cause some absorption. Fig 2.3 below shows three types of impurity absorption: donor-acceptor, donor-band and acceptor-band absorption.

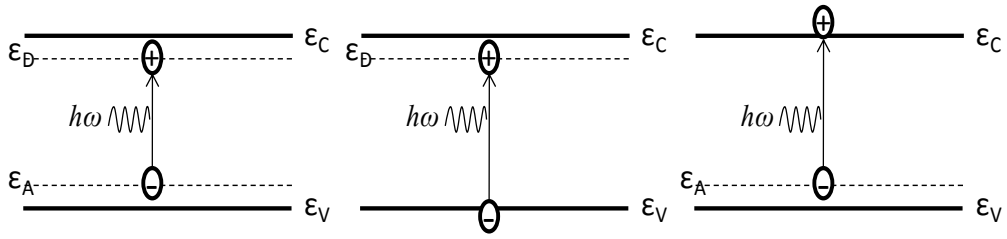


Figure 2.3: Illustration of (a) donor-acceptor, (b) donor-band and (c) acceptor-band absorption transitions

The transition energy of donor-acceptor absorption can be written as follows:

$$\hbar\omega = E_g - E_D - E_A + \frac{q^2}{\varepsilon_0 \varepsilon_r r} \tag{2.7}$$

The last term on the right-hand side of equation 2.7 stands for the Coulomb interaction between the donor and acceptor atoms. That leads to lowering of the binding energies. Also, as the distance between the donor and acceptor varies, the absorption energies and intensities change as well. Moreover, near-bandgap transitions between impurities and the opposite bandedge can take place when the impurity levels are ionized. Since the transition happens between discrete impurity levels and a band of energies, the transitions are observed as shoulders on the low-energy side of the absorption edge.

2.1.3 Low Energy Absorption

2.1.3.1 Shallow Impurity-Band Transition

At lower temperatures, when impurity levels are not ionized, carriers on the energy levels can be excited to the band edge by a low energy photon. Fig 2.4 below shows the two types of low energy impurity-band transitions.

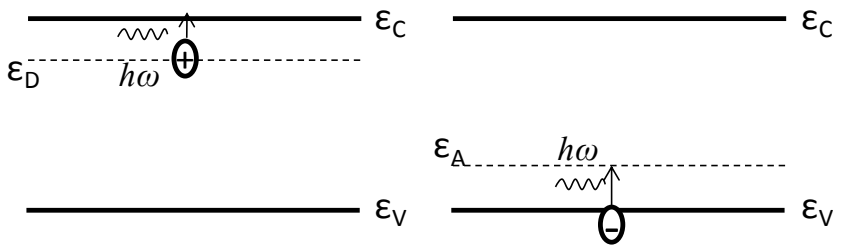


Figure 2.4: Illustration of low energy (a) donor-band and (b) acceptor-band absorption transitions

For this absorption the photon energy must be equal to or greater than the ionization energy of the impurity. This energy usually corresponds to the far infrared region of the optical spectrum.

2.1.3.2 Intraband Transition

At the zone center the valence band structure of most semiconductors consists of the light-hole (LH), the heavy-hole (HH) bands and the split-off (SO) bands. The three subbands are separated by spin-orbit interaction. In a p-type semiconductor the valence band is filled with holes, and the occupancy of the different bands depends on the degree of doping and the position of the Fermi level. With the right energy of the incident photons, absorption between different subbands can be observed. However, these types of transitions are not observed in n-type materials.

2.1.3.3 Free-Carrier Absorption

Free carrier absorption occurs when a material absorbs a photon and a carrier is excited from a filled region below the Fermi level to an unoccupied region above the Fermi level (in the same band). This is different from interband absorption in semiconductors because the electron being excited is a conduction electron (i.e. it can move freely). In interband absorption, the electron is being raised from a valence band to a conducting one. This transition also needs to conserve momentum. Momentum conservation is normally provided by optical or acoustic phonons.

2.1.4 Franz-Keldysh Effect

The change in absorption in the semiconductor with a strong electric field applied is called the Franz-Keldysh effect [30-31]. Under applied bias, the wavefunctions of electrons and holes turn from oscillatory to decaying behavior, which is declined by Airy function. In the absence of a photon, the valence electron has to tunnel through a triangular barrier of height E_g and thickness d, given by d= E_g/qE. With the assistance of an absorbed photon with energy less than the band-gap energy, the tunneling barrier thickness is reduced to d*= $(E_g$-hω)/qE, the overlap of the wavefunctions increases further and the valence electron can tunnel more easily to the conduction band. The whole process absorbs a photon with energy less than the band gap while providing conservation of momentum. The relationship of the absorption coefficient and the electric-field can be written as follows: [50]

$$\alpha = K(E')^{\frac{1}{2}} \frac{1}{8\beta} \exp\left(-\frac{4}{3}\beta^{\frac{3}{2}}\right) \tag{2.8}$$

Where

$$E' = \left(\frac{q^2 E^2 \hbar^2}{2m_r^*}\right)^{\frac{1}{3}}$$
$$\beta = \frac{E_g - \hbar\omega}{E'} \tag{2.9}$$

And K is a material-dependent parameter that has the value of $5 \times 10^4 \text{cm}^{-1}(\text{eV})^{-1/2}$ in GaAs. From a quantitative examination of the various terms in equation 2.8, the exponential term is the transmission coefficient of an electron through a triangular barrier and can be obtained from the Wentzel-Kramers-Brillouin (WKB) approximation. The other factors are related to the upward transition of an electron due to photon absorption. Based on that, in GaAs or SiGe materials, the magnitude of absorption is relatively small unless the electric field is higher than 10^5 V/cm [12]; thus it is not an efficient modulation mechanism.

2.1.5 Quantum Well Structure

A quantum well is a potential well that confines particles to two dimensional movement. When the quantum well thickness becomes comparable with the de Broglie wavelength of the particles confined, discrete energy levels will form and are called "energy subbands".

Quantum wells are formed in semiconductors by having a material, like gallium arsenide sandwiched between two layers of a material with a wider bandgap, like aluminum arsenide. These structures can be grown by molecular beam epitaxy or chemical vapor deposition with control of the layer thickness down to monolayers. The ideal case is quantum well surrounded by with infinite barriers. The quantized momentum vectors can be written as

$$k = \frac{n\pi}{L} \quad , \tag{2.10}$$

L is the width of the quantum well and n is the quantum number (a positive integer). This implies that the allowable energy states are discrete. The quantum confinement makes the transition energy of electrons from the valence to the conduction band larger than the band gap. The energy difference shown in Fig 2.5 is defined as the "quantum well energy"

$$E_n = \frac{(\hbar k)^2}{2m} = \frac{n^2 h^2}{8mL^2} \quad , \tag{2.11}$$

m is the effective carrier (electron/hole) mass and h is the Planck constant. That means the transition energy can be tuned by changing the quantum well width. Additionally, the effective mass of holes in the valence band is changed to more closely match that of electrons in the conduction band. These two factors made quantum well semiconductor a better structure for optical emission and absorption device applications.

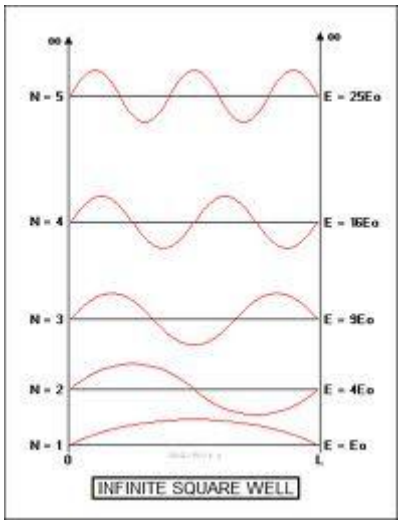


Figure 2.5: Ideal quantum well system with infinite barriers. Carriers' wave functions are confined inside well with discrete energy states

2.1.6 Quantum-Confined Stark Effect

Fig 2.6 illustrates the basic principle of the quantum-confined Stark effect (QCSE).

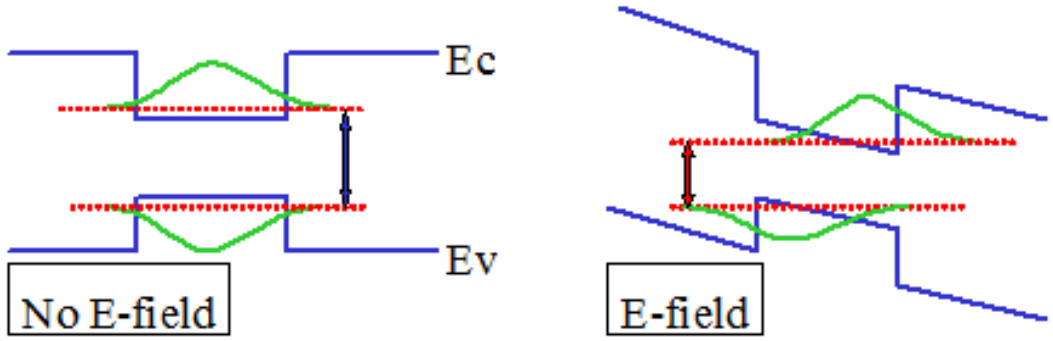


Figure 2.6: Quantum well (blue lines), carriers' wave functions (green lines) and states (red dash lines), and transition energy (arrows) with and without electric field influence.

When a semiconductor is fabricated with very thin layers (e.g. 10nm), the optical absorption spectrum changes radically as a result of the quantum confinement of carriers in the one dimensional quantum wells [32-33]. In a multi quantum well system the confinement changes the absorption from the smooth function of bulk material to a series of steps.

When there is no electric field, electron and hole wavefunctions are confined in the quantum well, and the overlap of the wavefunctions is increased. This results in an increase in the oscillator strength of the interband transitions between the discrete electron and hole bound energy states, which are produced by the size quantization. Therefore, strong resonances corresponding to the heavy-hole and light-hole transitions are seen near the band-edge of the well material even at room temperature.

When an electric field is applied across the quantum wells, it spatially separated the electrons and holes, reducing the overlap of their wavefunctions. This leads to red shift of the absorption and decrease of the absorption intensity. However, the exciton peaks are still strong for two reasons: (1) Two-dimensional quantum wells compress the excitons like pancakes. However, since typical well dimensions are ~10 nm and exciton diameter is normally larger than 30 nm, there is some penetration of the exciton wavefunction into the barrier material. (2) The wall of the quantum well impedes the electron and hole from tunneling out of the well. These two factors let the exciton remain relatively strong.

One of the other interesting phenomena triggered by multi quantum well system is that under high electric field, some forbidden transitions (such as even-symmetric electrons to odd-symmetric holes, or odd-symmetric electrons to even-symmetric holes) start to appear.

The appropriate Hamiltonian can be to analyze the QCSE energy transitions [32]:

$$
\begin{aligned}
H &= H_{ez} + H_{hz} + H_{eh} \\
H_{ez} &= \frac{-\hbar^2}{2m^*_{e\perp}} \frac{\partial^2}{\partial z_e^2} + V_e(z_e) + eFz_e \\
H_{hz} &= \frac{-\hbar^2}{2m^*_{h\perp}} \frac{\partial^2}{\partial z_h^2} + V_h(z_h) + eFz_h \\
H_{eh} &= \frac{-\hbar^2}{2\mu} \frac{\partial^2}{\partial r^2} - \frac{e^2}{\varepsilon[(z_e - z_h)^2 + r^2]^{1/2}}
\end{aligned}
\tag{2.12}
$$

H_{ez} is the electron energy Hamiltonian, H_{hz} is the hole energy Hamiltonian and H_{eh} stands for the exciton binding energy. m_e, m_h and μ correspond to the electron, hole and exciton masses. This Hamiltonian for the envelope functions of electrons and holes within the effective mass approximation does not include center-of-mass kinetic energy of electron and hole in the plane became negligible kinetic energy can be given to this motion by optical excitation. By applying separation of variables and transfer matrix techniques, the confined energy levels for electrons and holes under different biases can be calculated. Analysis shows that even under high electric field, the exciton binding is very strong in quantum well structures, further strengthening the QCSE [32].

When applying an electric field parallel to the quantum well plane, the band edge absorption broadens with increasing field consistent with field ionization. If the field is higher than ~10^4 V/cm, the exciton peaks broaden and eventually disappear, similar to 3-D excitons. For an electric field applied perpendicular to the wavefunction, the barriers confine electrons and holes in the well region even under a high electric field. Even at 50 times the classical ionization field with a shift of 2.5 times the zero-binding energy, the exciton peaks still remain resolved [33]. This effect is due to two factors: (1) carriers cannot tunnel through the quantum wells fast enough, so the ionization is

impeded (2) the quantum well size is much smaller than the exciton dimension. It is clear that this unique mechanism is mostly contributed by quantum well confinement.

The QCSE strength is sensitive to the polarization of the optical waves [34, 50, 51]. For transverse electric (TE) mode, the heavy hole (HH) exciton is 2 times stronger as compared to light hole (LH) transistions; for the transverse magnetic (TM) mode, only the LH exciton transition is allowed. This is very important for QCSE based optical waveguide modulator design.

By changing the absorption coefficient (α) of the quantum well structure, the dielectric constant ε will be changed as well. This leads to the change of the refractive index (n) as well. The complex form of the dielectric constant ε can be written as $\varepsilon = \varepsilon_r^{'} + j\varepsilon_r^{''}$; the refractive index (n) and absorption coefficient (α) are proportional to the real and imaginary parts of $\sqrt{\varepsilon}$, which corresponds to the real part (χ') and imaginary part (χ'') of the complex form of the susceptibility. χ' and χ'' can be correlated through the Kramers-Kronig relations [39, 40] as

$$\chi'(\omega) = \frac{2}{\pi} P\int \frac{y\ \chi''(y)}{y^2 - \omega^2} dy$$
$$\chi''(\omega) = -\frac{2\omega}{\pi} P\int \frac{\chi'(y)}{y^2 - \omega^2} dy \qquad (2.13)$$

where P is the principal value of the Cauchy integral, so a change of the band-edge absorption coefficient by the QCSE also causes a change of the refractive index, and vice versa. To correlate refractive index to absorption, the following equation can be deduced from equation 2.13:

$$n_r(E) = 1 + \frac{ch}{2\pi^2} P\int \frac{\alpha(E')}{E'^2 - E^2} dE, \qquad (2.14)$$

It can be seen that the change of the absorption coefficient is larger than the relative change of the refractive index. However, the use of the refractive index change in QCSE is widely used in today's high-speed optical communication devices; where size is not very critical compared to on-chip optical interconnect applications.

2.2 SiGe Material Platform

QCSE modulators are used widely in III-V compound alloys today. However, today's semiconductor IC industry is primarily based on a Si platform. In order to integrate optical interconnect systems, the material, device and fabrication process have to be Si compatible. On the other hand, Group-IV materials like Si and Ge are widely used in today's semiconductor industry. SiGe alloys have several advantages [52-54]: (1) Heterostructures improve the electrical properties (2) They are compatible with CMOS processes (3) Current material deposition technology can deposit high-quality SiGe thin films cost effectively.

2.2.1 Band Structures

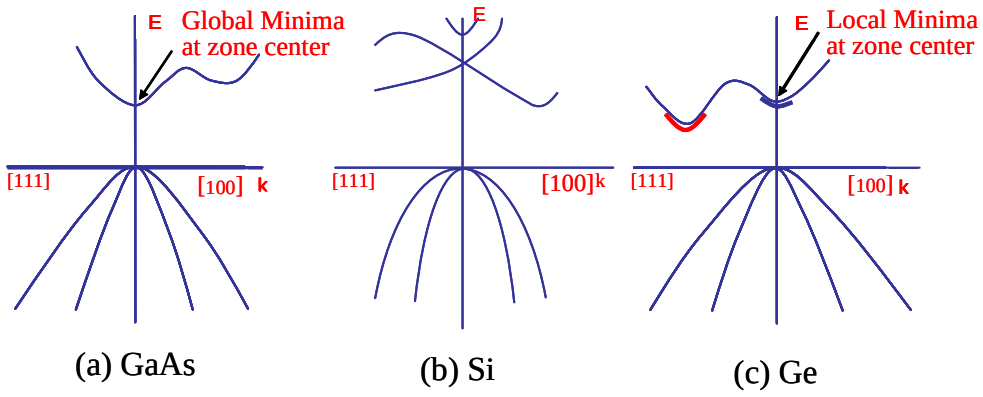


Figure 2.7 : Simplified k-E band structures of bulk semiconductors: (a) GaAs (b) Ge (c) Si.

Fig 2.7(a) shows the GaAs band E-k diagram. GaAs is a direct band gap material with both global minima of the conduction band and global maxima of the valence bands at the zone center of the band structure. The material can have radiative recombination and can absorb light through zone-center transitions. This is the most efficient optical transition process; therefore in most applications, including laser, LED, photodetector and QCSE modulation, direct bandgap material is used. For Si materials shown in Fig 2.7(b), the maxima of the valence band is at the zone center, however, the global minimum of its conduction band is far from the zone center [55, 56]; thus the optical processes for absorption and emission are very inefficient. This

also indicates that Si can be very useful in optical waveguide applications. The Ge band structure shown in Fig 2.6 (c) appears to be of special interest. The global maximum for the valence band is at the zone center. Even though the global conduction band minimum is at L valley, there is a local minimum at the zone center for the conduction band, and it is very close to global minimum. At room temperature, the absorption edges related to the direct and indirect transitions are ~ 0.8 eV [57] and ~0.64 eV respectively [58]. Fig. 2.8 shows the bulk absorption coefficient spectra versus the photon energy and wavelength for different semiconductor materials that are commonly used [59]. Si exhibits very typical indirect band gap absorption behavior; the absorption coefficient depends linear on the square root of the energy. For GaAs, there is almost no absorption below 1.43 eV; after that there is a very sharp transition. That is due to the direct bandgap. Similar behavior can be observed on InAs. For Ge, at 0.64eV, the absorption curve is similar to Si, however, after 0.8eV, there is a very sharp transition, and the absorption coefficient reaches 5000 cm^{-1}. This high absorption efficiency of Ge comes from its Kane-shaped band structure at the zone center [60] similar to the direct band gap III-V compounds.

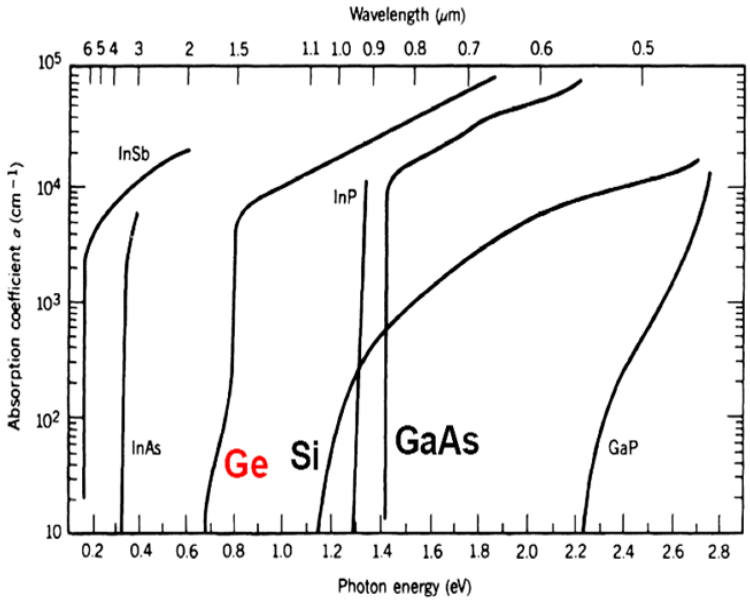


Figure 2.8: Bulk optical absorption coefficient spectra of major semiconductor materials. [57]

2.2.2 SiGe Alloy Properties

In applications of QCSE on a Si platform, understanding the SiGe alloy properties is the key for material structure design. Band structures, band alignment, effective mass and mobility will be especially important.

2.2.2.1 Band Structure of SiGe Alloy

One of the most critical features of Si and Ge is that the two materials are completely miscible. For $Si_{1-x}Ge_x$ alloys, over the entire x range from 0 to 100%, the compound will always have the cubic diamond lattice with a lattice parameter that increases almost linearly with increasing x. The lattice mismatch between pure Si and pure Ge is 4.2%. Both materials, including their alloys of all compositions, are indirect band gap semiconductor.

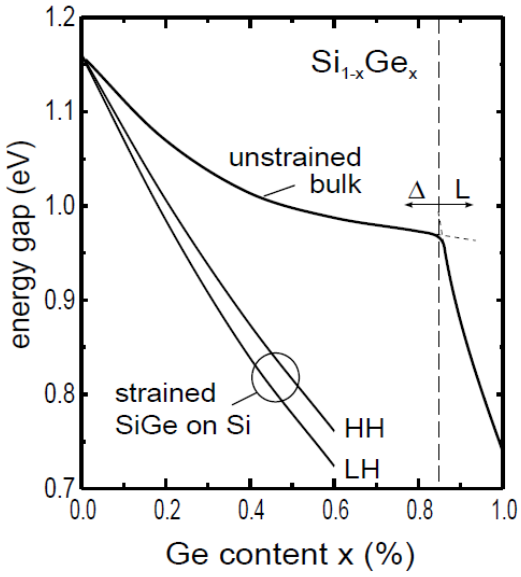


Figure 2.9: Band gap variation of SiGe alloys on Si with different Ge content x. [53]

Fig 2.9 shows the bandgap variation of SiGe alloys on Si with different Ge content. It can be seen that the bandgap variation is strongly affected by strain in the $Si_{1-x}Ge_x$ crystal. The lower two curves corresponds to the variation of strained $Si_{1-x}Ge_x$ alloys. The strain introduces heavy-hole/light-hole splitting of the valence band maximum

[53]. That means the in-plane compressive strain reduces the indirect bandgap when the Ge composition increases. However, for a relaxed $Si_{1-x}Ge_x$ layer, the bandgap behaves differently. The conduction band minima are six-fold degenerate in Si (located along the {100} directions near the X point) and eight-fold degenerate in Ge. (located at the Brillouin-zone boundary in the {111} directions). The indirect bandgap at 300 K (4.2 K) decreases monotonically from 1.11 (1.17) to 0.66 (0.74) eV as the Ge content x increases from 0 to 100%. When x=0.85, the indirect bandgap changes from the Δ minima to the L minima. That means the band structure of the material is more Ge like [61-63]. This leads to changes of the optical and electrical properties, which affect our design of SiGe/Ge quantum wells for photonic applications.

2.2.2.2 Band Alignment in SiGe Heterostructures

The SiGe quantum well structures developed in this work include thin layers of SiGe alloys with different Ge compositions. The large lattice constant mismatch between Si and Ge (4.2%) makes the different-composition SiGe layer strained. The strain can affect the band structure and the effective mass of electrons and holes and split the valence bands and Δ valleys. [53, 62, 64]

When two semiconductors form a heterojunction, discontinuities can occur in the valence bands and in the conduction bands. If one of the semiconductors is coherently strained on the other, two additional effects on the band structure have to be considered: hydrostatic strain shifts the energy position of bands and uniaxial or biaxial strain splits degenerate bands. The total change in the band is expressed as

$$\Delta E = \Delta E_a + \Delta E_h + \Delta E_s \tag{2.15}$$

ΔE_a stands for the alloy effect for the unstrained material, ΔE_h represents the shift due to hydrostatic strain and ΔE_s is the possible splitting due to uniaxial strain. The hydrostatic tensile (or compressive) strain lowers (or raises) all conduction bands and raises (or lowers) all valence bands. On the other hand, the uniaxial stress does not affect the average band energies, it only breaks the degeneracy of the valence bands. The valence band splittings in heavy hole (HH), light hole (LH), and spin-orbit-split

hole (SO) bands are determined by using the values for the spin–orbit splittings and in the strained $Si_{1-x}Ge_x$ layers. The Δ bands split into the four equivalent in-plane valleys Δ_4 and the two valleys along the growth direction Δ_2.

The band gap energy associated with the Δ valley might decrease or increase with the biaxial strain due to the complex conduction band structure, but the band gap energy associated with the L or Γ valley (more relevant to our interest in Ge-rich SiGe structures) would increase (or decrease) with the compressive (or tensile) biaxial strain.

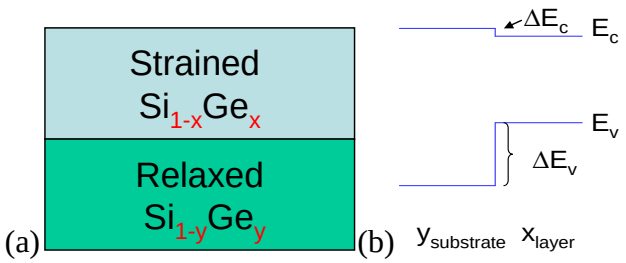


Figure 2.10: (a) heteroepitaxy of strained $Si_{1-x}Ge_x$ layer on relaxed $Si_{1-y}Ge_y$ buffer. (b) Typical band alignment (when x>y).

In this work, we are focusing on a strained $Si_{1-x}Ge_x$ layer deposited on a relaxed $Si_{1-y}Ge_y$ buffer, as shown in Fig 2.10 (a) above. Fig 2.10(b) shows the band alignment. Previous work [12] shows that most of the band offset is in the valence band and the valence band maximum is always in the SiGe layer with higher Ge concentration. That indicates weak electron quantum confinement, which is not favorable for quantum well device design. Therefore further band engineering needs to be done.

2.3 Band Engineering

Earlier work done in Stanford University related to QCSE on a SiGe platform has focused on finding the right band alignment of SiGe heterostructures. Most investigations can be divided into two categories based on quantum well alignment: (1) type-I system (2) type-II system. All of them were based on Si-rich alloys, which leads to weak indirect band absorption.

2.3.1 Type-I Aligned Quantum Well

The type-I aligned quantum well has both the conduction band minimum and the valence band maximum in the same layer. Si-rich SiGe quantum well structures were grown on Si [35-37]. Their absorption is very weak due to two effects: (1) the absorption is based on indirect band transitions; (2) the electron confinement is very weak due to the small conduction band offset discussed in the previous section.

2.3.2 Type-II Aligned Quantum Well

The type-II aligned quantum system has the conduction band minimum and the valence band maximum in different layers. Different structures, such as relaxed SiGe buffers [38] or higly strained Ge quantum dots on Si substrates [39] have been characterized. In this scenario, holes and electrons are not strongly confined.

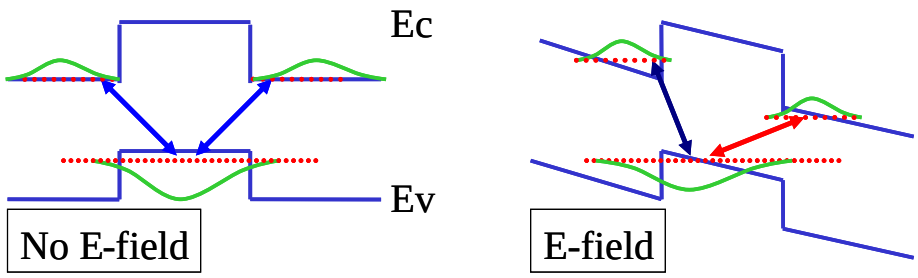


Figure 2.11: QCSE in a type-II aligned quantum well. Both blue and red shifts occur in the transitions under an electric field.

Fig 2.11 shows the transitions in a type-II aligned quantum well with and without an electric field. The electrons are confined in the Si-rich material and holes are confined in the Ge-rich material. As can be seen in Fig 2.11, electrons and holes are not confined in the same layer. When an electric field is applied, the transition energy on one side of the quantum well decreases and on the other side of the quantum well, the electron energy increases. That leads to large absorption shifts. However, since the coupling of carriers is weak, the absorption is very small and not practical for modulator applications.

2.3.3 Band Engineering in Ge Quantum Wells

Extensive calculation of the energy band shift between strained $Si_{1-x}Ge_x$ and relaxed $Si_{1-y}Ge_y$ layers were performed previously [53]. Although slightly different approaches were used, overall agreement based on previous work has been reached. Only a limited number of experimental results conducted under well defined strain conditions are available; they basically confirm the theoretical offsets within negligible error margins. The valence band maximum always occurs in the layer with higher Ge composition. Therefore, finding a position for the right conduction band offset is more critical in our work.

Fig 2.12 shows the contours of conduction band offsets (ΔE_C) between the strained $Si_{1-x}Ge_x$ and relaxed $Si_{1-y}Ge_y$ layers. For $x<y$, the conduction band minimum lies in the tensilely strained $Si_{1-x}Ge_x$ layer, and the band alignment is type-II. When $x>y$ and $y<0.6$, the conduction band offset is smaller than $\pm$20meV, which indicates a basically flat conduction band alignment within the accuracy of the calculations. For Ge-rich strained layers ($x>0.8$) with Ge-rich substrates ($y>0.6$), a type-I alignment is predicted.

It can be seen from Fig 2.12 that previous work has been focused on Si-rich substrates with varying Ge composition. They all used indirect bandgap transition; Si-rich type-I alignment has weak absorptioin; Ge-rich alloys are type-II due to strain effects. All these factors lead to failure of finding strong absorption for these SiGe alloy systems.

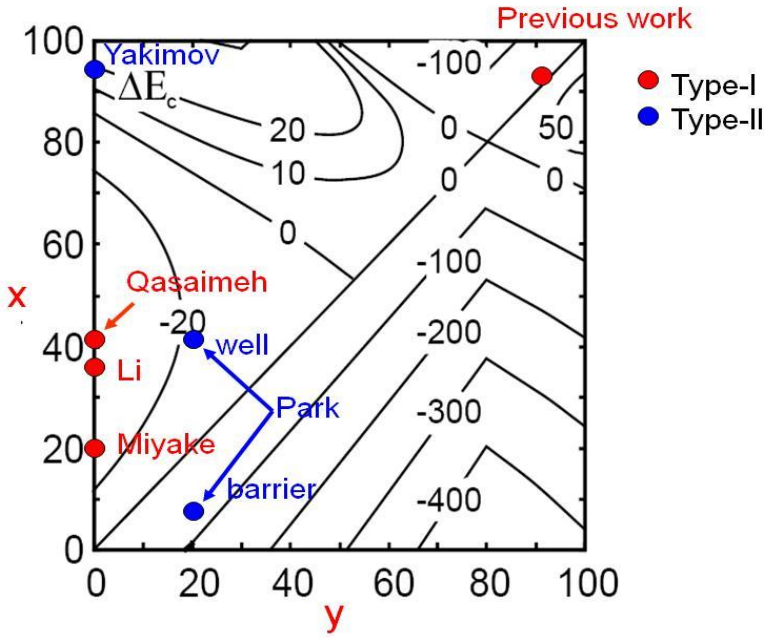


Figure 2.12: Conduction band offsets in SiGe heterostructures. x and y denote the Ge content in the strained epi-layer and relaxed buffer. Early SiGe work has been summarized (offset contours from ref. [51], data points from [35-40]).

In order to have high Ge content for high absorption efficiency and also to prevent type-II alignment, the upper right corner of Fig. 2.12 becomes the area of choice investigated in recent work and continues in this work.

2.4 Structure Design

Based on previous discussion, it is clear that QCSE is the strongest optical modulation mechanism and is more pronounced for direct band absorption in type-I aligned quantum wells. Because Si and Ge are indirect band gap material, photon absorption needs phonon assistance. Therefore, indirect transitions are insufficient due to the low coupling probability. The absorption coefficient near the band edge is low because there is no clear minimum in the conduction band at the zone center for Si and Si-rich SiGe alloys. However, in Ge there is a local minimum at the zone center, allowing efficient direct band gap transitions with high absorption efficiency. Equally important is that this direct conduction band minimum is not much higher than that of the global indirect band minimum, so the absorption coefficient ratio between the direct band

transition and the indirect band transition is still high enough that a sharp absorption edge can be observed in Ge. This Kane-shape band structure of Ge at the zone center is similar to that of direct band gap III-V compound materials, such as GaAs or InAs, and in recent work [41] this feature has been utilized to band-gap engineer the Ge quantum wells for the quantum-confined Stark effect. The approach has been continued and refined in the present work.

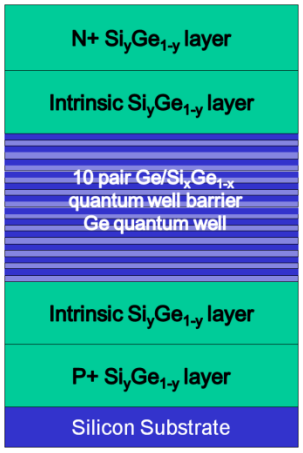


Figure 2.13: A SiGe p-i-n structure on silicon with $Ge/Si_{1-x}Ge_x$ quantum wells on relaxed $Si_{1-y}Ge_y$ buffer

Due to the high lattice mismatch between Si and Ge, Ge layers directly grown on silicon tend to form 3D islands or become highly strained. These effects will result in type-II alignment. In order to avoid this, a relaxed Ge-rich SiGe layer was used as the buffer layer between quantum well structures and the Si substrate.

Fig 2.13 shows the basic device structure for our modulator devices. Standard p-i-n structures were used. The whole p-i-n diode is grown on a relaxed Ge-rich buffer layer to reduce strain effects. The i-region is used so that the electric field is uniform across the Ge/SiGe quantum wells in the intrinsic region where a voltage is applied to tune the band-edge absorption. Inside the multiple-quantum-well (MQWs) structure, strain-balanced $Ge/Si_{1-x}Ge_x$ pairs were grown to balance the strain and eliminate strain induced bandgap changes.

2.4.1 Band structure design

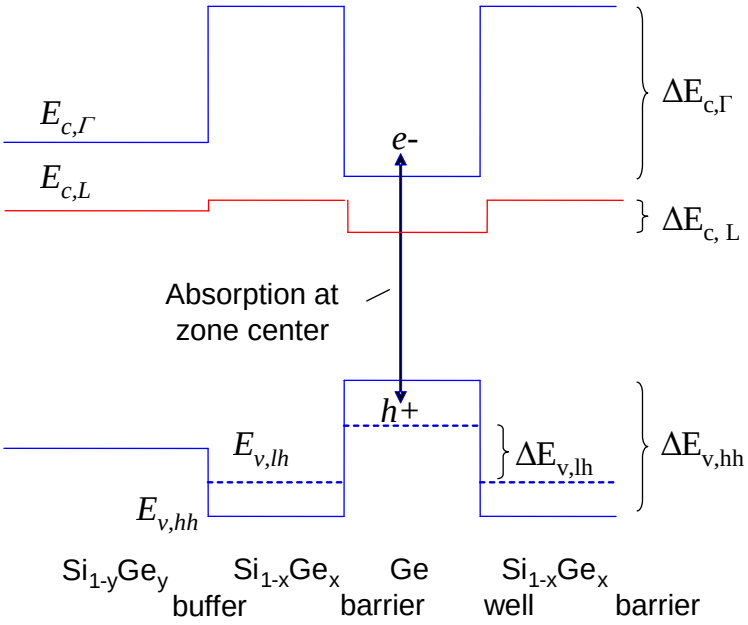


Figure 2.14: Sketch of the band structure in real space (not to scale) of a Ge/SiGe MQW structure. $E_{v,lh}$ and $E_{v,hh}$ are the valence band edges of the light holes and the heavy holes respectively. $E_{c,\Gamma}$ and $E_{c,L}$ are the conduction band minima at the zone center (the Γ point) and at the L valleys. ΔE represents the band offset.

Fig 2.14 above shows the band alignment of the material. The Ge/SiGe quantum well structure is grown on a relaxed SiGe buffer layer. Since the Ge well (and SiGe barrier) is compressively (and tensily) strained, its valence bands are split and leaving the heavy hole (and light hole) at the top of the valence bands. There is little strain in the relaxed SiGe buffer, therefore its valence band remains degenerate. In the conduction band, the global minima of the buffer and barriers are L valleys and lower than Γ point. This design has several advantages. The sharp edge and high absorption efficiency of Ge and the compressive strain from the SiGe barriers provide a strong Stark shift. By using a Ge-rich buffer, both the indirect bands and direct bands are type-I. By using this design, the modulator device can use the direct bandgap transition, which is much stronger than the indirect transition. Also this helps photo-generated carriers to be scattered into the L valley where they can be swept out by the electrical field more easily, leading to faster carrier recovery dynamics.

2.4.2 Band Parameters

Through previous band structure calculations [62], we calculate the band offset by using the following equations.

Valence Bands: The valence band offsets for a strained $Si_{1-x}Ge_x$ layer on a relaxed $Si_{1-y}Ge_y$ layer can be expressed as [62-64]:

$$\Delta E_{hh}(x,y) = [0.74 - 0.07y][x - y] \tag{2.16}$$

$$\Delta E_{lh}(x,y) = -0.3y + 0.289y^2 - 0.142y^3 + \left(0.683 - 2.58y + 3.21y^2 - 1.24y^3\right)x + \left(0.435 + 0.704y - 2.439y^2 + 1.295y^3\right)x^2 + \frac{\left(-0.354 - 3.77y + 8.79y^2 - 2.46y^3\right)}{\left(1 - 2.7y + 28.1y^2\right)}x^3 \tag{2.17}$$

if z > 0.5 and $|x - z| \le 0.5$, which covers the SiGe composition range of our interest.

The valence band energy positions of the strained Ge well and SiGe barrier relative to the relaxed $Si_{1-z}Ge_z$ buffer can be calculated using Eq. (2.16) for the heavy hole and Eq. (2.17) for the light hole;, thus the offsets of the heavy hole and light hole valence bands, $\Delta E_{v,hh}$ and $\Delta E_{v,lh}$, between the well and barrier can be extracted.

Direct Conduction Bands: The direct band gap energies (with the relevant conduction minimum at the Γ'_2 point) of bulk Ge and Si are 0.8 eV and 4.175 eV respectively at room temperature [65]. The direct band gap energy of SiGe is linearly interpolated between the value of bulk Ge and Si here, thus the band offset between the Ge well and $Si_{1-x}Ge_x$ barrier can be expressed as

$$\Delta E_{c,\Gamma} = (4.175 - 0.8)x - \Delta E_{v,hh}. \tag{2.10}$$

This interpolation does not consider the strain effect on the conduction band.

Indirect Conduction Bands: The indirect band gap alignment is not critical to the optical absorption in this work. The band alignment has been shown in Fig 2.14. The indirect conduction band contour is shown in Fig 2.12 for SiGe strained layers grown on SiGe relaxed buffer layers with different Ge composition in each layers.

Effective Masses: The effective masses of $Si_{1-x}Ge_x$ are linearly interpolated between the values for Si and Ge. Their values along the growth direction at the Γ point are $0.041m_o+0.115(1-x)m_o$ [50], $0.28m_o+0.21(1-x)m_o$ [58], and $0.044+0.116(1-x)m_o$ [58] for the electron, heavy hole, and light hole respectively and m_o is the electron rest mass. It should be noted that there is an uncertainty in the electron effective mass at the zone center where fewer experimental studies have been done for silicon.

It can be seen that all the calculations are based on linear interpolation, excluding he strain effect for the conduction band. However, previous simulation [12] has shown that the uncertainties from strain have only negligible effect on the quantum well energy shift, because of the large conduction band offset in the direct bandgap.

2.4.3 Previous Simulation

Theoretical calculation and simulation of band alignment were previously done in order to understand how the design parameters in the quantum well structure impact the performance of the material [12].

The simulation procedure includes three steps [66]: (i) first design the potential line-up of the quantum well and divide it into small slices along the growth direction, (ii) build up carrier transfer matrices for each slice and heterojunction based on the electric field, well/barrier thicknesses, and band alignment as well as carrier effective masses, (iii) multiply the transfer matrixes and then extract the tunneling resonance energy under different electric fields.

Simulation shows the following trend in quantum well design: (i) the quantum well energies of the electron and heavy hole are lowered by increasing electric field, (ii) quantum well thickness affects the transition energy and stark shift significantly, (iii) barrier and buffer composition have weak impact on QCSE (iv) conduction band offset does not affect the quantum well energy very much.

With the conclusions above, we finalize our design to be: $Si_{0.1}Ge_{0.9}$ buffer layer and $Si_{0.15}Ge_{0.85}$ barrier with pure Ge quantum wells. The quantum well thickness is 10 nm, and the barrier thickness is 16.5nm.

Chapter 3 SiGe Material Growth

3.1 SiGe Alloy Surface Morphology

Studies [67-70] show that if the lattice mismatch between heterostructures is small and the thickness of the epilayer does not exceed the critical thickness (ref Mathews & Blacklee), the atoms on the two sides of the interface are in perfect registration in-plane and the mismatch is accommodated entirely by the elastic strain in the epilayer; the growth of the epilayer is then coherent, pseudomorphic or commensurate. This is also true for SiGe heterostructures, although the range of composition and thickness is certainly more constrained than in most III-V systems.

Strained SiGe layers of increasing thickness on Si tend to relax strain both by dislocation formation and by roughening the surface. Theis leads to local elastic relaxation of strain. Such roughening may be enhanced by local inhomogeneities caused by enhanced diffusion to dislocations, point defects or contamination. However, even a perfect SiGe layer on Si may have three different surface morphologies [71-74].

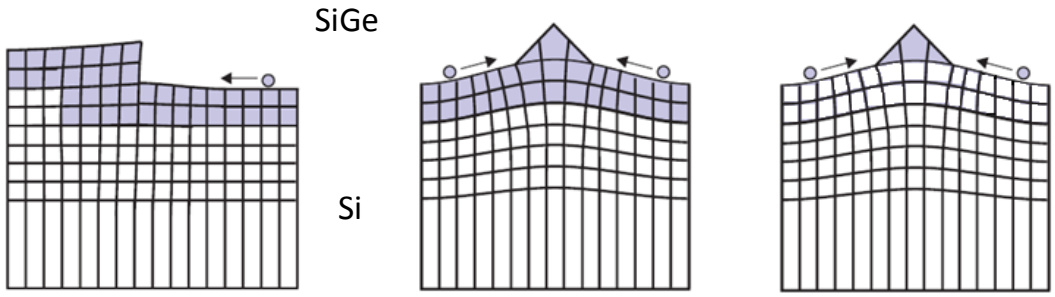


Figure 3.1: Thin film growth modes: (a) 2D growth (b) mixed growth (c) pure 3D growth [75]

Fig 3.1 (a) shows the homogeneous 2D deposition of a SiGe layer in the step-flow mode on a Si substrate which has a small (inevitable) miscut. Growth on a miscut substrate may result in a layer of modulated thickness. Some SiGe material may accumulate at the intrinsic step edges, as mismatch strain can be partially relieved by accumulation at these locations. The local relaxation of lattice parameter of epitaxial SiGe in the vertical as well as the lateral direction is enabled by the modified boundary condition of a stepped free surface with additional free bonds compared with a flat layer. The elastic SiGe relaxation causes a distortion of the underlying Si substrate, which reduces the strain energy gained by the system. The relaxation energy increases with the amount of deposited SiGe material, with the Ge content and with the step height. This induces an instability in the strained layers on vicinal surfaces due to accumulation of material at step edges and enhanced bunching of surface steps in the strained layers.

Fig 3.1 (b) shows mixed growth of 2D and 3D features. Under this scenario, elastic strain is reduced by undulation of the strained layer surfaces. With waviness in certain directions, the lattice remains strained in that direction. The material forms 2D islands and allows relaxation in all directions, and the relaxation energy gained may be larger compared with the former case. The surface area in that situation is normally increased and energetically less-favourable crystal planes will be formed to lower the overall energy of the system.

Fig 3.1 (c) shows the 3D growth of islands and the process, which was described and analyzed in Ref. [70]. If grown at higher temperatures (600-700 ℃), the transition

from uniform 2D layer growth of SiGe alloy to 3D nucleation of stable islands takes place rapidly like a phase transition. This requires two conditions: (1) The diffusion length of adatoms has to be large enough to enable effective mass transport. (2) A material-dependent energy barrier has to be overcome for island formation.

By understanding the difference in surface morphology, slow kinetics can be used to prevent approaching the energetically favored structure. 3D growth can be avoided by using a low substrate temperature and high growth rate to yield a high-quality and relatively flat surface.

The methord to quantify strain is very important to measure the stress between thin-film materials. Fig 3.2 (a) schematically shows the structure of strained SiGe grown on a Si substrate. The lateral lattice spacing is compressed to $a_{\parallel}$ which is the same or close to that of Si. The vertical spacing will be extended to $a_{\perp}$. Fig 3.2 (b) shows the relaxed SiGe layer grown on Si. The lattice constant is the same as that of bulk SiGe having the same composition.

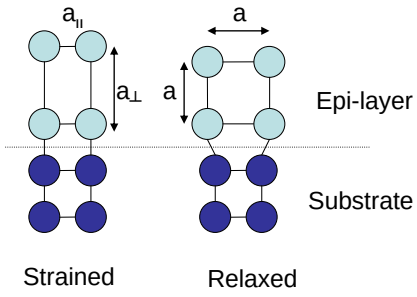


Figure 3.2: Atom arrangements of (a) strained (b) relaxed epi-layers on substrates.

For Fig. 3.2 (a), the stresses on the epi-layer are $a_{\parallel}$ (parallel to the interface) and $a_{\perp}$ (perpendicular to the interface) and can be expressed as

$$\varepsilon_{II} = \frac{a_{II} - a}{a} \tag{3.1}$$

$$\varepsilon_{\perp} = \frac{a_{\perp} - a}{a} = \frac{2\ C_{12}}{C_{11}} \varepsilon_{II}\ , \tag{3.2}$$

where C_{11} and C_{12} are the elastic stiffness constants. C_{11} and C_{12} of Si (and Ge) are 16.58 and 6.39 (and 12.85 and 4.82) respectively (all in units of 10^6 N/cm^2) [71]. For

certain materials, stresses in both directions can give us a very clear picture of information such as critical thickness, potential crystal quality, etc.

3.2 Growth Techniques

3.2.1 Deposition Systems

3.2.1.1 Molecular Beam Epitaxy

Molecular beam epitaxy (MBE) was the original technique used for the growth of epitaxial SiGe layers and is the growth technique that commonly used in III–V heterostructure growth research. In MBE a molecular or atomic beam of the growth species is created by heating the raw material above its melting point using an effusion cell. Shutters are then used to select which materials may impinge on the heated substrate on which nonequilibrium thermodynamic processes compete to produce an epitaxial layer.

Since Si and Ge melting points are quite different, it is not very efficient to use MBE to grow SiGe alloys. Also, it is not very easy to get high quality material and well controlled doping profiles in the MBE system available to this work.

3.2.1.2 Chemical Vapor Deposition

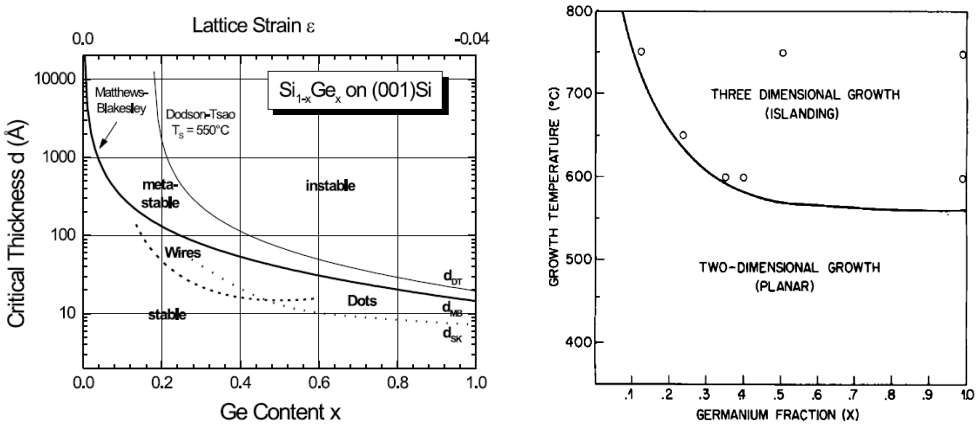
Standard silicon CVD is typically carried out at atmospheric pressure or reduced pressure (~5-100 Torr) and involves the pyrolysis or reaction at an elevated temperature of a precursor gas of Si, such as silane, disilane or a silicon halide. Radio frequency coils or high-intensity lamps are used to heat the system to temperatures ranging from 900^{o}C to greater than 1100^{o}C to volatilize nominally contaminating species, such as water, oxygen or carbon and then to grow the desired layer.

CVD has the advantage over MBE of lower background contamination and fewer defects. It is also significantly more uniform mainly due to the higher development budgets and, consequently, to the development of high throughput production tools. The biggest advantage of CVD growth is that the growth rate and Ge

composition are dependent on the pressure, gas flow rate and substrate temperature, allowing multiple choice of variables to control the layer characteristics. However, if any of these parameters change, the growth rate and composition need to be recalibrated.

3.2.2 3-D growth Suppression

Because Si and Ge have a large lattice mismatch, the high strain energy tends to relax by forming dislocations or 3D islands [75-77]. This work is focused on high Ge composition SiGe alloy growth; the conditions under which it is very easy to get dislocations or 3D growth.



(a) (b)

Figure 3.3: (a) Critical thickness of SiGe film on Si [74]. (b) Dependence of growth mode on growth temperature and Ge content [75].

Fig 3.3 (a) shows the critical thickness of $Si_{1-x}Ge_x$ grown on Si with different Ge content and growth temperature. It clearly shows that under non-equilibrium growth conditions, the critical thickness decreases as Ge content increases under three type of growth. Fig 3.3 (b) shows that for Si-rich SiGe, 2D growth can be obtained at fairly high temperatures. If Ge composition is greater than 50%, it is very likely to produce 3-D islands when growing at temperatures above 550^{o} C. In order to have a sharp and periodic quantum well structure, a flat surface is necessary, and 3-D growth must be

avoided. In order to control the strain in the Ge/SiGe MQWs, a relaxed, Ge-rich SiGe layer is deposited first as an intermediate lattice matching buffer layer.

3.2.3 Profile Control

In order to get effective absorption and clear QCSE, sharp interfaces with abrupt Ge composition profiles need to be formed when growing multiple quantum wells. Two factors become the main obstacles: Diffusion and segregation effects. Segregation is the migration of Ge atoms to the surface to lower the surface energy. This happens commonly in MBE growth [78]. When the growth starts, minimization of the surface free energy drives the segregation of the Ge mostly to the surface, the initial monolayers of the alloy layer are depleted in Ge, leading to a Ge-rich surface layer. By the end of the deposition, as Si continues to be deposited, Ge continues to segregate while simultaneously being partially incorporated into the growing SiGe layer. Diffusion on the other hand, happens by exchange of Si and Ge between lattice sites. When the temperature is high enough (i.e $>500^{o}$ C), Si and Ge will have significant interdiffusion.

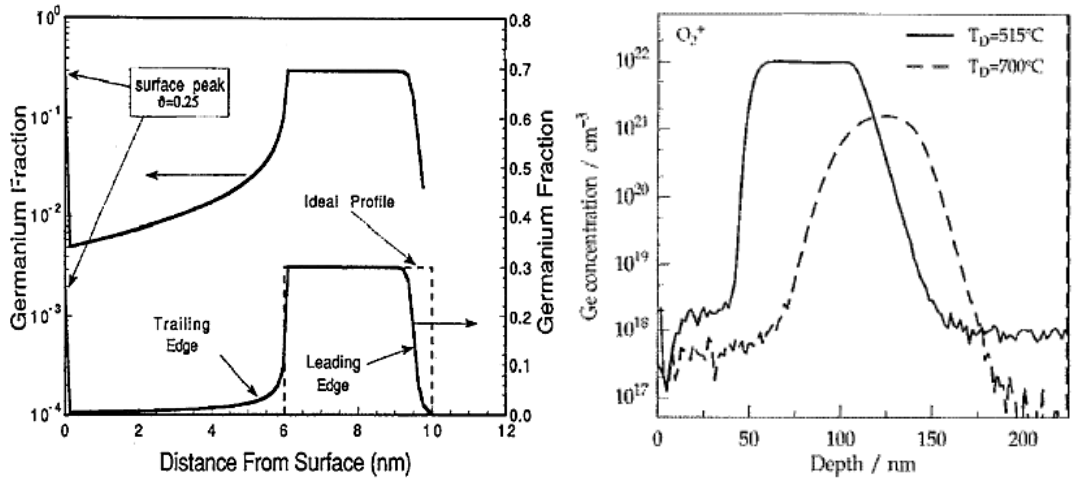


Figure 3.4: (a) Ge profile on SiGe sandwich structure grown by MBE. (b) Ge profile of SiGe heterostructure grown by CVD [78-79]

Fig. 3.4 (a) shows a SiGe layer between pure Si cap and buffer layers grown by MBE. Clear Ge segregation and SiGe interdiffusion are predicted and observed. In Fig

3.4 (b) a $Si_{0.75}Ge_{0.25}$ layer was grown on a Si substrate in a UHV/CVD system. It can be seen that there is no Ge segregation. That's because in CVD systems, hydrogen is present from the growth reactant and reduces Ge segregation. Also it can be seen that at low temperatures, Ge tends to diffuse less [79]. In a reduced-pressure CVD reactor, hydrogen is typically added as a carrier gas, further reducing segregation.

From the discussion above, we can carefully design our structure to minimize these two effects. In order to grow sharp quantum well structures, it is more favorable to use a CVD deposition system and grow at low temperatures.

3.3 Chemical Vapor Deposition (CVD) Approach

3.3.1 System Introduction

Figure 3.5: Applied Materials Centura Epi RPCVD reactor used in this work

Fig 3.5 shows the CVD tool used for this study. It is a reduced pressure CVD (RPCVD) reactor. It is a commercially available, cold-wall, single-wafer, mass-production tool and is routinely used in CMOS chip fabrication processes. The model used in this work is an Applied Materials Centura Epi Reactor with a "High Temperature Film" (HTF) chamber. The growth pressure capability of this reactor ranges from ~1 Torr to 600 Torr, the operating temperature capability ranges from 450-1200° C.

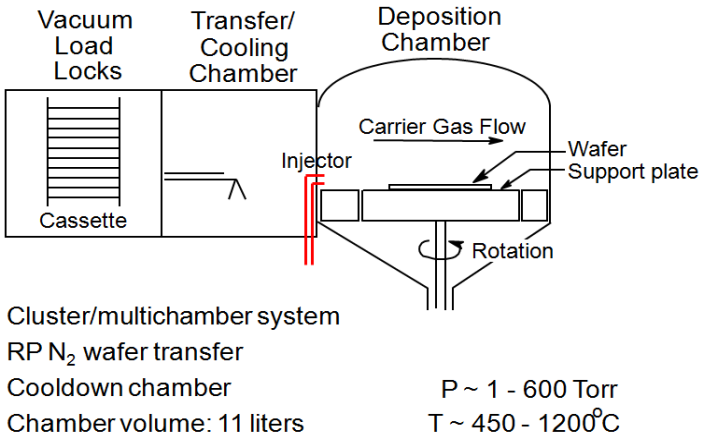


Figure 3.6 Fig 3.6: Applied Materials Centura Epi RPCVD schematic

Fig 3.6 shows the schematic of the Epi reactor. It is a multi-chamber system. Wafers are loaded into the vacuum load lock, which is then pumped to 80 torr. A wafer is then transferred into the transfer chamber before being moved into the deposition chamber. The wafer is put on a rotating support plate in the deposition chamber. Gas comes in from an injector on one side of the deposition chamber and is evacuated on the other side. The carrier gas and reactant gases flow across the rotating wafer during the deposition.

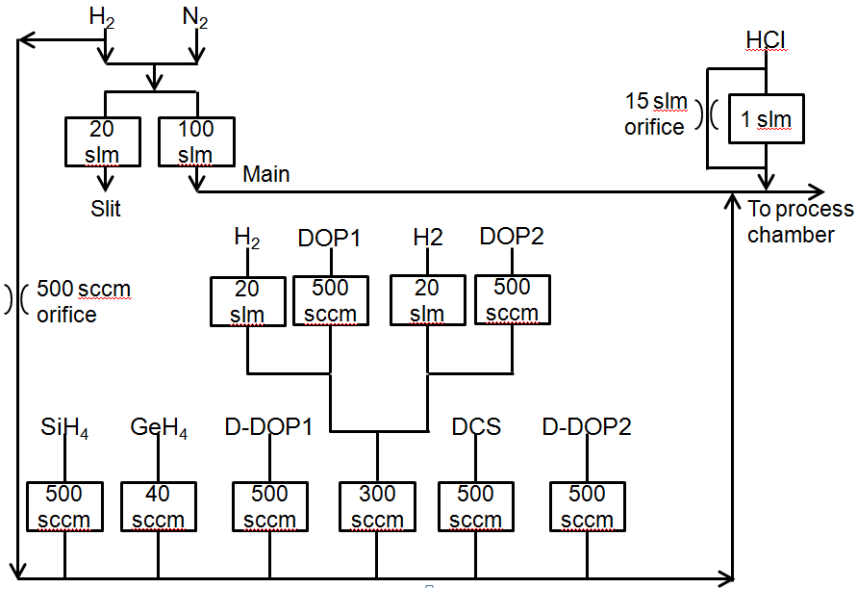


Figure 3.7: Schematic diagram of the Centura gas flow control system

The schematic of the gas control panel is shown in Fig. 3.7. The reacting gases include silane (SiH_4) and dichlorosilane (DCS) for Si, germane (GeH_4) for Ge and for SiGe alloy growth. Different concentrations of diborane (B_2H_6), arsine (AsH_3), and phosphine (PH_3) are used as dopants. The carrier gases are hydrogen and nitrogen, and the etching gas is HCl. The diluted dopant can be injected directly into the main gas stream or further diluted to obtain a wide range of different doping concentrations.

3.3.2 Growth Calibrations

Before loading, the Si wafers are cleaned using the standard pre-deposition procedure (4:1 H_2SO_4:H_2O_2 at 90 ℃ for 10 min, 5:1:1 HCl:H_2O_2:H_2O at 70 ℃ for 10 min, 2% HF for 30 s, with DI water dump/rinse between each step, and finally spin dried). No extra protective surface layer is necessary because the cleaning bench and the CVD reactor are in the same clean-room fabrication facility.

After loading the wafers into the load lock chamber, it is purged with nitrogen and pumped to a vacuum of 80 Torr. Before loading a wafer into the growth chamber, the growth chamber will go through a standard high temperature HCl etch to remove any prior residual SiGe deposition and dopant on the support plate or the chamber walls. After loading and before growth, the Si substrate is baked at 1000 ℃ for 5 min to remove any surface oxide. Epi-layers are grown by custom recipes edited by growers. The wafer is then unloaded after the growth and sent for processing and characterization.

The composition of Ge in SiGe was measured by secondary ion mass spectrometry (SIMS). The thickness of the layer can be characterized by SEM, TEM and mass-difference. SEM and TEM can show real cross-sectional images of the deposited SiGe film, which provide the most accurate thickness measurement if the sample is well aligned and the cross-section is perpendicular to the growth direction. The mass-difference method uses a scale to measure the mass increment after the deposition of a single SiGe layer. When the SiGe density (i.e., composition) as well as the wafer size are known, the thickness can be calculated by dividing the mass

difference by the wafer surface area and film density. The accuracy of this method is relatively poor, so the deposited film thickness should be at least 0.5μm thick. However, the mass has been shown to be the same when comparing the values of the same wafers before cleaning and after cleaning/baking (without growth). The advantage of this method is that it is convenient, fast and non-destructive.

Fig 3.8 shows the SIMS measurement of the calibration growth of SiGe with different Ge compositions. Ge content targeting from 84% to 97% in the SiGe alloy were successfully grown under similar conditions. With these conditions, the layer thickness and the SiGe composition information, we have multiple degrees of freedom to design the quantum well structures with different SiGe layers.

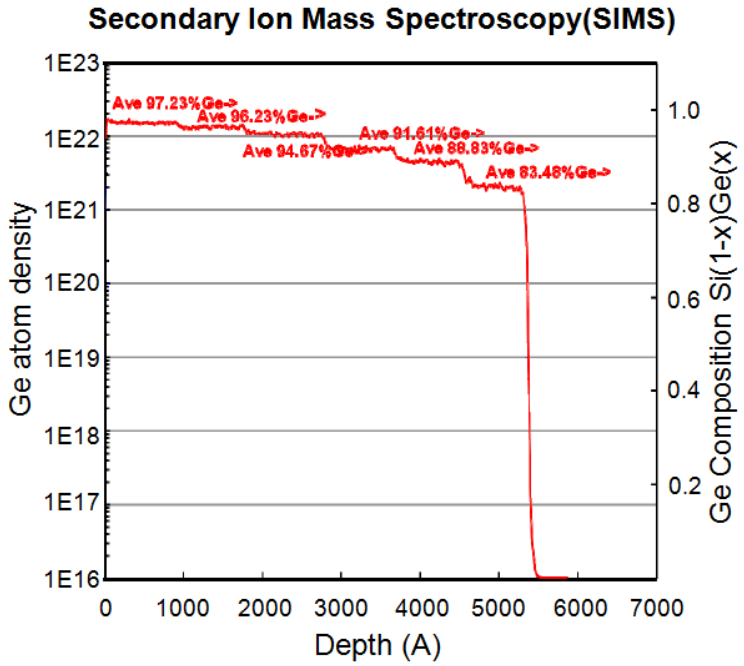
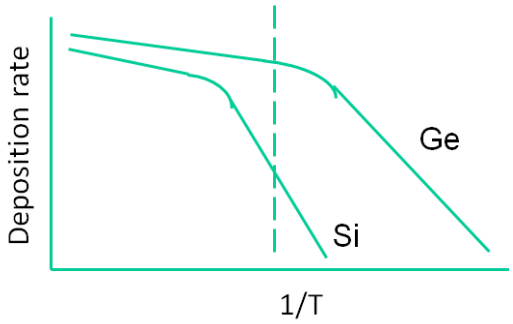


Figure 3.8: SIMS measurement of SiGe layers grown on Si using RPCVD

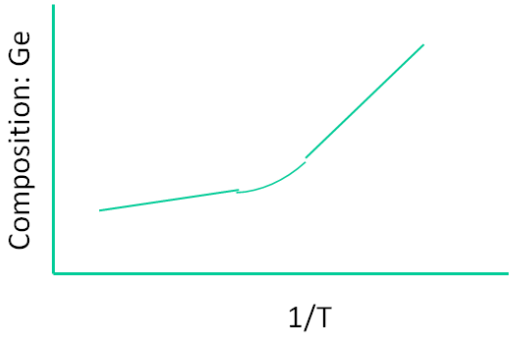
3.3.3 Growth Rate Design

There are five growth parameters, including the germane flux, silane flux, carrier gas (H_2) flux, chamber pressure, and growth temperature, which determine the SiGe

composition and growth rate. Some of these parameters affect both the composition and the growth rate.



(a)



(b)

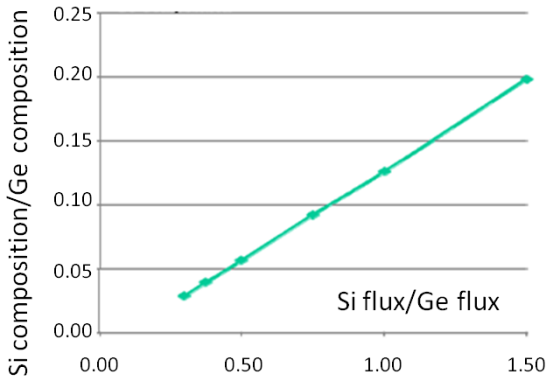
Figure 3.9: (a) Temperature dependence of Si and Ge growth. (b) Temperature dependence of Ge composition in SiGe layers

Fig 3.9 (a) schematically shows the temperature dependence of Si and Ge growth. Changing the temperature not only alters the growth rate, but also changes the Ge composition. That's because the Si and Ge precursors have different activation energies. According to Fig 3.3, in order to get a smooth surface for Ge rich SiGe layers, the growth temperature has to be lower than 450^{o} C.

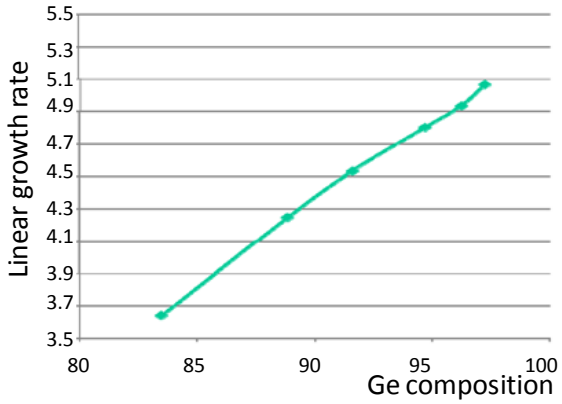
Previous work tried several growth temperatures from 350^{o} C to 450^{o} C[12]. It was found that when the germane and silane fluxes as well as the growth temperature are fixed, the growth rate of SiGe (with 5% Si content or more) and pure Ge are both inversely proportional to the carrier gas flow; however, the former is almost independent of the chamber pressure while the later is proportional to it. Moreover, for

Ge-rich SiGe, the X_{Si}/X_{Ge} composition ratio is proportional to the silane - germane flux ratio and is independent of the temperatures. Also, the overall growth rate is proportional to the Ge composition at a given growth temperature.

A series of SiGe samples was grown at different temperatures (300, 325, 350, 375, 400, 425 and 450 ℃). The germane flux, hydrogen flux, and chamber pressure were 40 sccm, 30 slpm, and 40 Torr, respectively, and the silane flux was varied from 10 to 70 sccm. By considering the needed growth rate at the desired Ge composition, 375 ℃ is chosen to be the growth temperature.



(a)



(b)

Figure 3.10: (a) SiGe concentration ratio vs Si/Ge flux ratio. (b) Growth rate vs.Ge composition.

Fig 3.10 shows the growth result under the above conditions. Fig 3.10 (a) clearly indicates that under these conditions, the Si/Ge concentration ratio is proportional to

the Si/Ge flux ratio. Fig 3.10 (b) shows that the growth rate of SiGe is linearly dependent on Ge composition.

3.3.4 SiGe Growth Model

The growth model for SiGe alloys with SiH_4 and GeH_4 precursors is complicated [80, 81]. The growth of $Si_{1-x}Ge_x$ by CVD can be divided into two regimes: a heterogeneous decomposition dominated regime and a homogeneous decomposition dominated regime.

Heterogeneous decomposition: In $Si_{1-x}Ge_x$ CVD, there are four types of surface sites on the substrate: H-terminated Si sites (H-Si), H-terminated Ge sites (H-Ge), H-free Si sites (-Si), and H-free Ge sites (-Ge). With two precursors involved (SiH_4 and GeH_4), there are a total of eight most likely heterogeneous reactions on the substrate.

Notation	Description	Reactions
$J_{GeH4/Ge}$	GeH_4 flux on Ge sites	$GeH_4(g) + 2\text{-}Ge(s) = H_3Ge\text{–}Ge(s) + H\text{–}Ge(s)$
$J_{GeH4/H–Ge}$	GeH_4 flux on H–Ge sites	$GeH_4(g) + H\text{–}Ge(s) = H_3Ge\text{–}Ge(s) + H_2(g)$
$J_{GeH4/Si}$	GeH_4 flux on Si sites	$GeH_4(g) + 2\text{-}Si(s) = H_3Ge\text{–}Si(s) + H\text{–}Si(s)$
$J_{GeH4/H–Si}$	GeH_4 flux on H–Si sites	$GeH_4(g) + H\text{-}Si(s) = H_3Ge\text{–}Si(s) + H_2(g)$
$J_{SiH4/Ge}$	SiH_4 flux on Ge Sites	$SiH_4(g) + 2\text{-}Ge(s) = H_3Si\text{–}Ge(s) + H\text{–}Ge(s)$
$J_{SiH4/H–Ge}$	SiH_4 flux on H–Ge sites	$SiH_4(g) + H\text{–}Ge(s) = H_3Si\text{–}Ge(s) + H_2(g)$
$J_{SiH4/Si}$	SiH_4 flux on Si sites	$SiH_4(g) + 2\text{-}Si(s) = H_3Si\text{–}Si(s) + H\text{–}Si(s)$
$J_{SiH4/H–Si}$	SiH_4 flux on H–Si sites	$SiH_4(g) + H\text{–}Si(s) = H_3Si\text{–}Si(s)+ H_2(g)$

Table 3.1: Most likely heterogeneous reactions in Si1−xGex CVD from GeH4 and SiH4

Table 3.1 shows the eight most likely reactions in the heterogeneous decomposition regime. The activation energies for reactions on H-terminated Si and Ge sites are larger than those on H-free Si and Ge sites. As a result, reaction fluxes on H-terminated Si and Ge sites can be neglected compared to those on H-free Si and Ge sites. Therefore, we can reduce the number of expression for the Si and Ge fluxes [81].

Fig 3.11 (a) shows the schematic of all the possible heterogeneous reactions. Equations of fluxes can be written in relation to partial pressures of different gases and θ_{Si} and θ_{Ge} represent the ratio of H-terminated Si sites to all Si sites and the ratio of H-terminated Ge site to all Ge sites, respectively. Fig 3.11 (b) shows the H desorption from surface sites and H diffusion between Ge and Si sites. In SiH_4 CVD, the H coverage of Si sites; θ_{Si}, decreases with increasing temperatures and increases with larger flow rates of SiH_4.

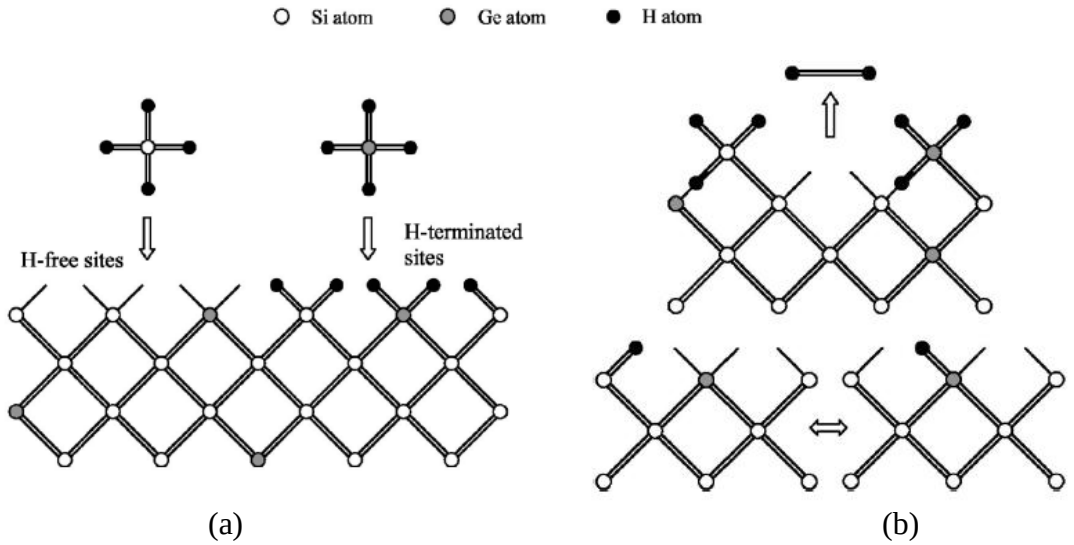


Figure 3.11: (a) Most likely heterogeneous reactions in $Si_{1-x}Ge_x$ CVD from GeH_4 and SiH_4. (b) H desorption from surface sites and H diffusion between Ge and Si sites.

Surface H coverage in $Si_{1-x}Ge_x$ growth is complicated due to the presence of Ge. At lower temperatures, H desorption occurs more easily when Ge is present. This significantly increases the SiGe alloy deposition rate. The adsorption of SiH_4 and GeH_4 brings H to the surface and H desorption removes H from the surface. In addition, H atoms diffuse between Ge and Si sites on the surface. H desorption is enhanced when a H atom diffuses to a Ge site compared to desorption from a Si site.

Homogeneous decomposition: SiH_4 homogeneously decomposes into SiH_2 and H_2 at temperatures higher than 950 ℃. However, the temperature for $Si_{1-x}Ge_x$ growth by CVD is often between 350 and 550 ℃, and thus homogeneous decomposition of SiH_4 is very slow and can be neglected. GeH_4 also decomposes into GeH_2 and H_2. At 300 ℃, heterogeneous decomposition of GeH_4 predominates when the GeH_4 flow rate is low,

and homogeneous decomposition of GeH_4 predominates at 450 ℃ when the GeH_4 flow rate is high. However, a side effect of GeH_4 homogeneous decomposition is that it complicates the gas phase chemistry for both GeH_4 and SiH_4, especially at high temperatures or high GeH_4 flow rates.

Based on the discussions above, in order to make the growth rate more predictable and controllable, precise control of temperature and gas fluxes need to achieve to have a well controlled heterogeneous regime growth rate. Also, at 350-450 ℃, the growth rate with moderate Si and Ge fluxes must be controlled to get a predictable homogeneous growth rate.

3.3.5 Doping Control

Four different diluted dopant sources are available, including 1% B_2H_6 (for high p-doping), 100 ppm B_2H_6 (for low p-doping), 1% PH_3 (for high n-doping), and 100 ppm AsH_3 (for low n-doping). Their growth mechanisms are similar to those of Si and Ge hydride. High-level PH_3 or B_2H_6 doping for SiGe growth can change the growth rate, but its influence on SiGe composition is less than 1% [12].

In this work, the buffer layer and the cap layer are doped. The intrinsic region needs to have very low doping. The sharpness of the doping profile and the consistency of SiGe composition are very important to device operation. Therefore low-level 100 ppm, 100 ppm B_2H_6 and 100 ppm AsH_3 are used.

Fig 3.12 shows the measured doping profile in a SiGe p-i-n diode grown on a Si substrate. The total thickness is 2.8 μm, with 0.4μm of P region, 0.4μm of n region and 2μm of intrinsic region. The average composition of the entire structure is $Si_{0.1}Ge_{0.9}$. The red line is the Ge composition, and the green line is the Si composition. The yellow line is the B doping profile. The P region doping reaches 4e18 cm^{-3}, which falls into our doping expectations. In the i-region and n-region, since the B concentration is much lower than 1e16cm^{-3}, the lower limit of the SIMS characterization, the measurement result is noisy. That's mostly due to the auto doping in the chamber. When the gas sources are switched, there are still residues of previous gases in the

chamber that will affect doping concentration. This is also true for the As concentration measurement in the p region and i regions. In the n region, the As concentration is lower than 1e18 cm^{-3}. This is lower than we expected. And the doping consistency over the depth is not very stable.

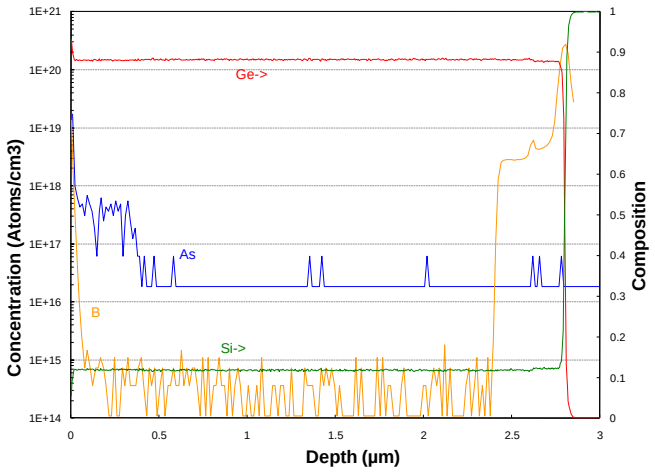


Figure 3.12: Doping profile: SIMS measurement of a SiGe p-i-n test diode. Red line is the Ge composition, green line is the Si composition. Blue line is the As doping level and yellow line is the B doping level.

3.4 SiGe Buffer Layer Growth

3.4.1 Multiple SiGe Buffer Growth Approach

According to the previous discussion, it is desirable to grow SiGe/Ge quantum wells on a Ge-rich buffer to control the strain and its influence on material quality and band alignment. Fig 3.13 shows the prior methods used for SiGe buffer growth on Si: graded buffer method (REF), direct buffer method with single-growth-temperature (REF) and direct buffer method with two-growth-temperatures (REF). For the graded buffer method, Ge composition of SiGe layers increases continuously from zero at the Si substrate to the desired Ge composition. For the direct buffer method, films with a single SiGe composition or pure Ge are deposited on top of silicon substrates at low

temperature. After growth, the wafers are annealed at higher temperatures. The procedure can be iterated several times. The two-temperature growth technique first deposits a thin layer of low temperature SiGe, anneals at high temperature and then grows thicker layers of SiGe at high temperature.

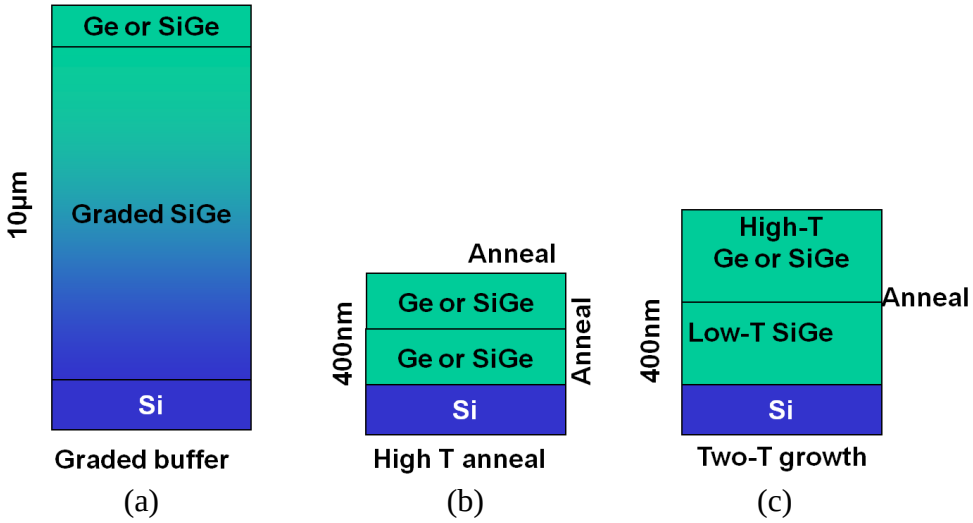


Figure 3.13: Buffer growth methods: (a) graded buffer; (b) direct buffer with two cycles of low T growth and high T anneal; (c) direct buffer with two growth-temperatures.

Method	Graded Buffer		Direct Buffer		
			Two T growth	Single T growth	
Equipment	UHVCVD [86]	MBE[87]	UHVCVD[88] MBE[89] RPCVD[90]	MBE[87]	RPCVD[91]
Procedure	Graded $Si_{1-x}Ge_x$ From x=0 to 100%		Two T growth	Above melting temperature	Low T growth High T anneal
As-grown roughness	High	Low	Low	High	High
Roughness reduction	CMP	Sb surfactant	Not used	Not used	anneal
TDD(cm^{-2})	2.1e6	5.4e5	1e7	1-3e5	1e7
Thickness	10µm	4µm	1µm	2.5µm	0.4-1µm

Table 3.2: Comparison of Ge-on-Si growth methods. [86-91]

In the Ge-rich SiGe buffer growth, most studies were targeted toward the pure Ge-end for laser, photodetector, and electronics applications based on Ge-on-Si or

III-V-on-Ge-on-Si [82-85]. Previous work mainly focuses on growth methods of Ge-on-Si buffers. The comparison with the literature is summarized in Table 3.2. The buffer layer is Ge-rich SiGe.

In the graded buffer approach, the buffer layer is normally 10-15μm thick. The roughness is very high and requires either CMP or Sb surfactant introduction during growth to smooth it. Neither of these approaches is suitable for subsequent quantum well p-i-n deposition. Moreover, this thick buffer layer is not practical for optical modulator applications. The key advantage of this approach is that it produces a low threading dislocation density [83, 84] (TDD) at the top of the grown layer.

In order to reduce the buffer layer thickness, direct growth of SiGe on Si was studied. One interesting approach was to deposit Ge on Si above the Ge melting temperature [88]. This will offer 100% relaxed SiGe layer with low TDD and high surface roughness and 3-D islanding, which is not desirable for optical applications. In order to avoid this, two variations were introduced: (1) Two temperature growth. About 30-50nm of Ge layer was deposited at 300-350^{o}C to relax and flatten the layer (shown in Fig 3.13(c)). Then a thicker Ge layer is deposited at 600^{o}C. Finally the sample is annealed at 900^{o}C in between the low and high temperature growth to reduce the TDD. (2) Low temperature growth and high temperature anneal. (Multiple hydrogen annealing for heteroepitaxy, MHAH shown in Fig 3.13(b)). Ge is directly grown on a Si substrate at a relatively low temperature (~350^{o}C), and then annealed at a high temperature to reduce the surface roughness and TDD. During annealing, since Ge atoms have higher energy, they reflow and smooth the surface. This is unsuitable, because the roughness is too high. In normal cases the roughness will be higher and 3-D structures will be formed. In order to reach the desired level of surface roughness, 2-3 cycles of growth and annealing are needed. The drawbacks are the high initial surface roughness and the need for long-time annealing in a specific high temperature range to reduce the roughness. Both methods can achieve a moderate TDD level (~10^{7}/cm^{2}); the roughness in (1) is lower than in (2), but it requires two different

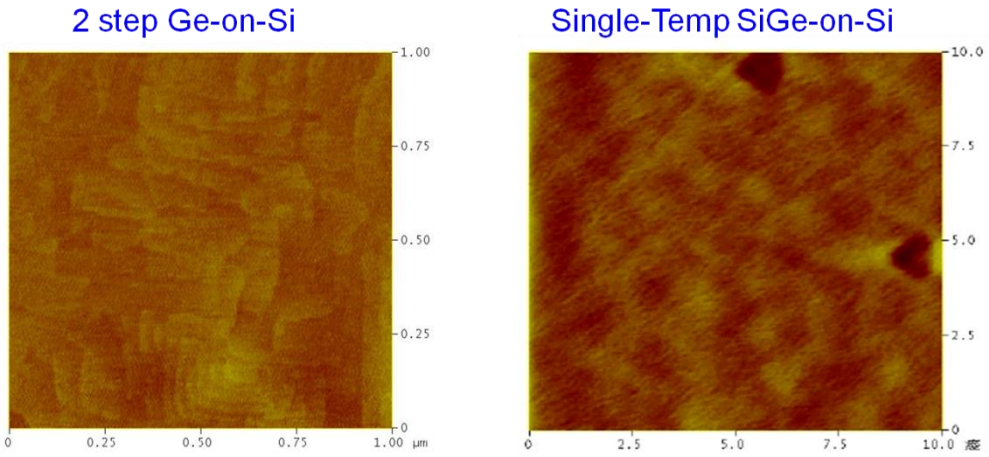
growth temperatures, and this gives more variations in Ge composition in multiple quantum well structure growth.

Comparing these two alternatives, it is obvious that there are tradeoffs between surface roughness and thickness and TDD. Since surface roughness and buffer thickness are more critical in this work than TDD, and a thinner layer is beneficial for further single mode waveguide and device design, the MHAH method is used in this work, because it has thinner buffer and comparable surface roughness to the other method.

3.4.2 Direct Buffer Growth

Since the QCSE is based on absorption, a moderate level of threading dislocations is acceptable. On the other hand, a thin buffer is preferred for optical device design in practice. Since temperature affects growth rate dramatically in the regime this work focus on, growth should be done at the same growth temperature to get a stable Ge composition and growth rate.

One of the key differences between Ge-rich SiGe and Ge growth is that Si atoms in the deposition can suppress 3-D growth. A flat initial surface can be achieved in the SiGe-on-Si growth at a single growth temperature before annealing, but the pure-Ge-on-Si growth requires annealing to reduce the surface roughness, or may even require two growth-anneal cycles.



(a) (b)

Figure 3.14: [12] AFM image of as-grown surface. (a) MBE-grown Ge-on-Si with 2-growth-temperatures. (b) RPCVD-grown SiGe-on-Si at a single growth temperature. Both samples were annealed

Fig 3.14 shows the AFM comparison of the Ge-on-Si and SiGe-on-Si samples. Fig 3.14 (a) shows Ge grown on Si using the two temperature growth method by MBE (300/600 ℃), it had only 0.2 nm root-mean-square (RMS) roughness. It represents the best as-grown surface in the Ge-on-Si case from previous work. Fig 3.14 (b) shows an AFM image of the surface of SiGe on Si grown by RPCVD at a single temperature of 400 ℃ with annealing at 850 ℃ for the first layer and 750 ℃ for the second layer. The silicon concentration is 10%, but the RMS roughness is also 0.2nm after the annealing. If Ge is grown under the same conditions, the RMS roughness will be 25nm. The surface roughness shown in Fig 3.14(b) increases to 1~2 nm with longer annealing time and higher temperature.

Previous work [12] has characterized $Si_{0.05}Ge_{0.95}$ alloy layers using the single temperature growth method. A SiGe layer was deposited on silicon at 400 ℃ and then annealed at 850 ℃; a second SiGe layer was deposited and annealed after that. TEM measurements have shown that most threading dislocations have been terminated at the Si - SiGe interface. Only a few of them have propagated into the second layer. Even though threading dislocations lead to increased dark current, it is still tolerable in modulator applications.

3.5 Ge/SiGe Quantum Well Structure Growth

3.5.1 Stain Balanced Structure

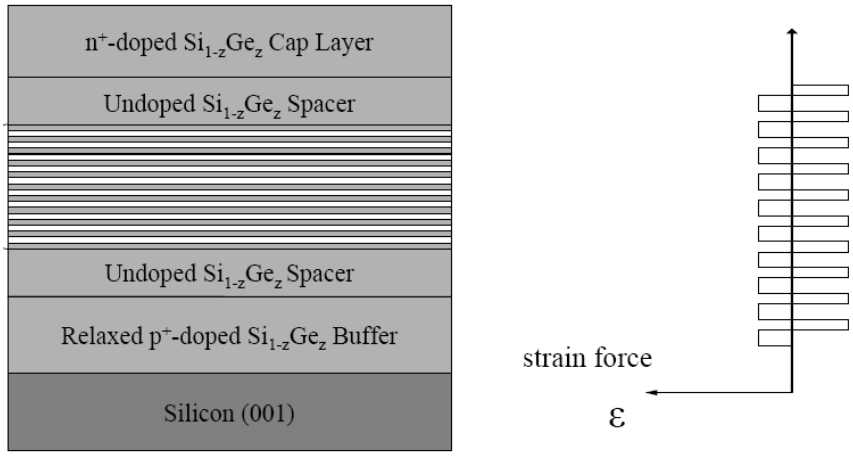


Figure 3.15: Strained Ge/$Si_{1-x}Ge_x$ quantum well structure on relaxed $Si_{1-z}Ge_z$ buffer and its strain balance.

Fig 3.15 shows the detailed structural information for the multi quantum well system designed in chapter 2. A relaxed p-doped $Si_{1-z}Ge_z$ buffer layer is deposited on a Si substrate. The intrinsic Ge spacer and wells and the SiGe barriers are then deposited on top as an i-region. The thickness and composition of the barriers and wells are designed in a way that the quantum well superlattice is strain-balanced. Since the Ge well is compressively strained relative to the $Si_{1-z}Ge_z$ buffer, the $Si_{1-x}Ge_x$ barrier must be tensily strained (x>z) to compensate the compressive stress in the QW. The average Si concentration in the Ge/SiGe MQW region is designed to be the same or similar to that in the buffer. The strain forces of the compressed Ge and extended SiGe layers of each QW pair cancel, and no net strain energy accumulates into the next pair. Theoretically this would enable extension of the strained layer thickness beyond the critical thickness limitation to infinity.

Since all quantum-well layers are strained relative to the buffer, their $a_{\parallel}$ are the same, but the $a_{\perp}$ of the Ge well (and the SiGe barrier) is larger (and smaller) than their equilibrium value due to the strain.

3.5.2 Growth Techniques

The buffer layers are grown at 375 ℃ for two cycles. For each cycle, 200nm of SiGe was deposited and then annealed at 850 ℃ for 30 min. After two cycles another SiGe intrinsic spacer with 100nm was deposited. SiGe/Ge quantum wells are deposited at 375 ℃ as well. After that, another SiGe intrinsic spacer with 100nm thickness was deposited. Finally, 200 nm of n-doped SiGe layer with same Ge composition as the buffer layer is deposited as a cap layer. Before growth of each layer, the reactant gas flows were switched to "vent" for 40 s with only H_2 carrier gas flowing into the chamber to keep the gas flow steady. This will ensure all the MQW interfaces are sharp and the Ge and doping profiles are sharp as well.

Fig. 3.16 is a cross-sectional TEM image of 10 pairs of strained SiGe/Ge QWs grown on relaxed SiGe on Si. The Ge well is 10 nm and the $Si_{0.15}Ge_{0.85}$ barrier is 18 nm. The sharp and regular MQW structure provides steep barriers for better carrier confinement and improved optical quality.

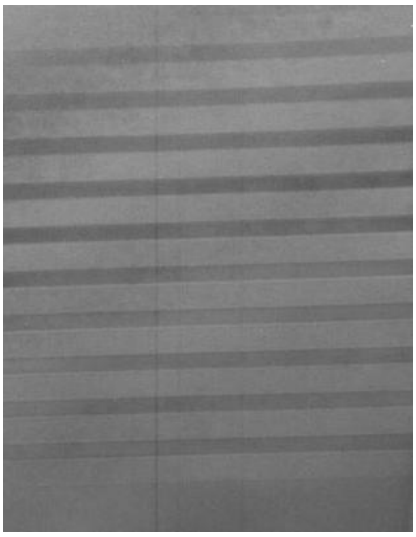


Figure 3.16: Cross-sectional TEM image of 10-pair MQW grown on SiGe on Si.

Due to the high lattice mismatch between Si and Ge, the structure is highly strained. If the buffer layer is not fully relaxed and the amount of strain is not correct in the Ge/SiGe MQWs, band misalignment could have a negative impact on the

absorption length and strength. XRD was used to examine the strain balance in the grown structure.

Fig 3.17 shows a 2-D XRD reciprocal-space map of the MQW Ge/SiGe structure. The Si substrate signal and SiGe buffer layer signal are clear and sharp. The buffer peak is obviously surrounded by several other peaks from the Ge/SiGe MQWs, which indicates a high MQW quality in this sample since it is difficult to observe that in SiGe/Si MQWs even when they are in the Si-rich end. Also, the line between SiGe and Si peaks is parallel to the omega-theta relaxation line, clearly indicating that the buffer layer is fully relaxed.

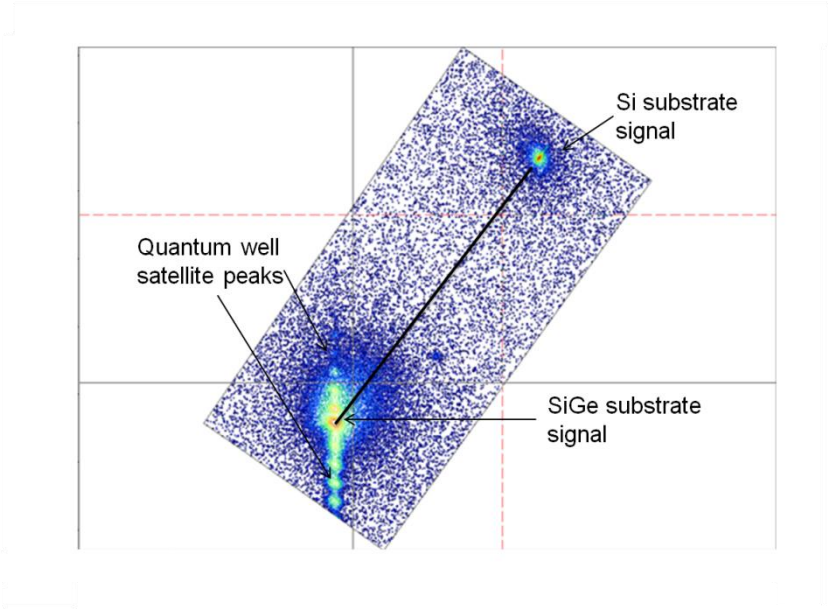


Figure 3.17: 2-D XRD reciprocal-space map of quantum well sample

3.6 Selective Growth

In selective epitaxy, the substrate is covered by a dielectric masking layer everywhere except for the growth window. During selective epitaxy, growth occurs

only inside the growth window. In order to extend the selective growth technique to waveguide modulator applications, selective growth is studied in this work.

Selective growth of bulk Ge on Si has been investigated for optical detector applications [89]. In our work, we extend the selective growth to a more complex structure: 10 pairs of 10nm compressively-strained Ge quantum wells with 18nm $Si_{0.15}Ge_{0.85}$ barriers which are embedded in the intrinsic region of a vertical p-i-n $Si_{0.1}Ge_{0.9}$ diode structure, for optical modulator applications. The entire p-i-n structure is grown at 395°C on a pre-patterned (001) silicon substrate by reduced pressure chemical vapor deposition (RPCVD).

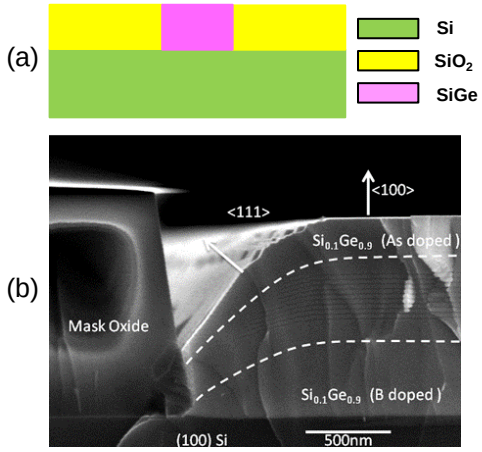


Figure 3.18: (a) Schematic of selective growth. (b) SEM of actual growth

Fig 3.18 (a) shows a schematic of the selective growth. The pre-patterned substrates have a 1.2 μm thermal oxide, acting as a growth mask, with growth seeding windows of different widths. Boron and arsenic are incorporated in the p and n regions, respectively, through in-situ doping. Fig 3.18 (b) shows strong faceting within 1um in regions next to the growth window boundary. Planar and uniform quantum well structures are grown away from the faceting region.

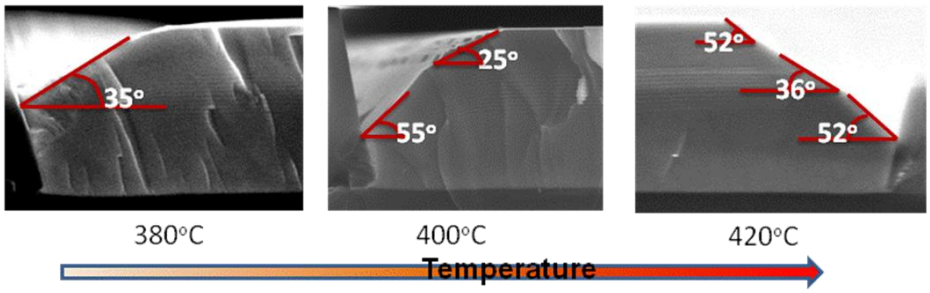


Figure 3.19: Temperature dependence of the selective growth

Fig 3.19 shows the selective growth for the same window size but with different growth temperatures. It can be seen that at different growth temperatures, not only is the growth rate changed, but the facet angle at the surface is different. At 380^{o} C, <211> (35^{o}) facet growth dominates; at 400^{o} C, <111> and <311> facets can be observed; at 420^{o} C, <111> and <211> facets can be seen. There are several growth factors interacting with each other, leading to multi facet growth patterns. This is not favorable for future device fabrication, however, this problem can be solved by growing a thicker layer and using CMP for real device applications.

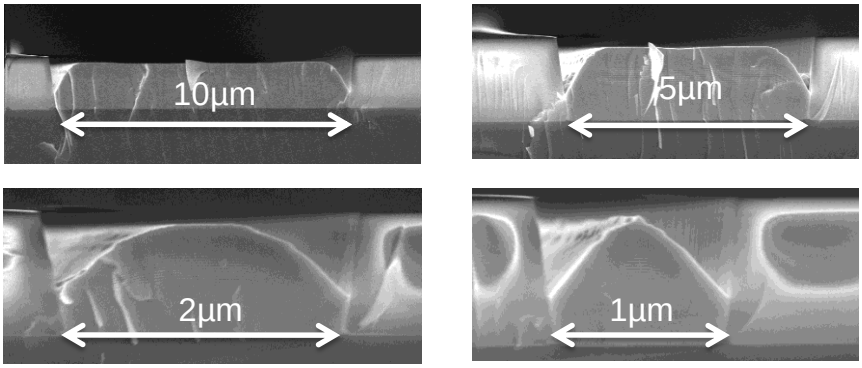


Figure 3.20: SEM image of selective growth of SiGe on Si with different window opening sizes

Fig 3.20 shows the selective growth of SiGe on Si with different window opening sizes. From the SEM picture, the grown thickness is independent of growth window size. That lack of dependence on growth window size leads to the conclusion that there is no loading effect in SiGe selective growth in this work. Also, measurement shows that there are no obvious discrepancies in facet angles with different window opening sizes under the same growth conditions. That reduces the complexity of future fabrication for different device lengths in waveguide modulator applications. One

interesting observation is the orientation of the quantum wells. It can be seen on the SEM picture that the quantum well was tilted at the edge of the oxide SiGe interface.

Chapter 4 Device Fabrication

4.1 DC PIN Diode Fabrication

Previous work demonstrated strong QCSE absorption spectra in Ge/SiGe quantum wells [41]. Because of the thin quantum wells and barriers, growth of these structures is moderately challenging, thus proving that our material exhibits significant QCSE is a first step before fabricating a high-speed optical modulator.

Our DC SiGe modulator devices are SiGe p-i-n diodes on Si with Ge/SiGe quantum wells in the i-region. The Ge/SiGe quantum-well structures were grown by RPCVD. We used thin, direct deposition of SiGe buffers on Si, as described in Chapter 3, and 10 pairs of quantum wells on top of the buffer with a single growth temperature of 375 ℃ used for all layers.

Fig. 4.1 shows the device fabrication processes. 4-inch, (001)-oriented, boron-doped Si wafers with resistivity 10-20 Ω-cm were used as starting substrates. Two boron-doped Ge-rich SiGe layers (p-type dopants with doping levels ~$5x10^{18}$ cm^{-3}) were deposited on silicon sequentially and annealed. The first 250nm layer is annealed at 850 ℃ for 30-60 min, and then a second 250 nm SiGe layer is deposited at 375 ℃ and annealed at 700 ℃ for 5 min. Undoped spacers, and Ge/SiGe quantum wells and barriers were then deposited and capped by arsenic-doped layers (n-type dopants with doping levels ~ $6x10^{18}$ cm^{-3}).

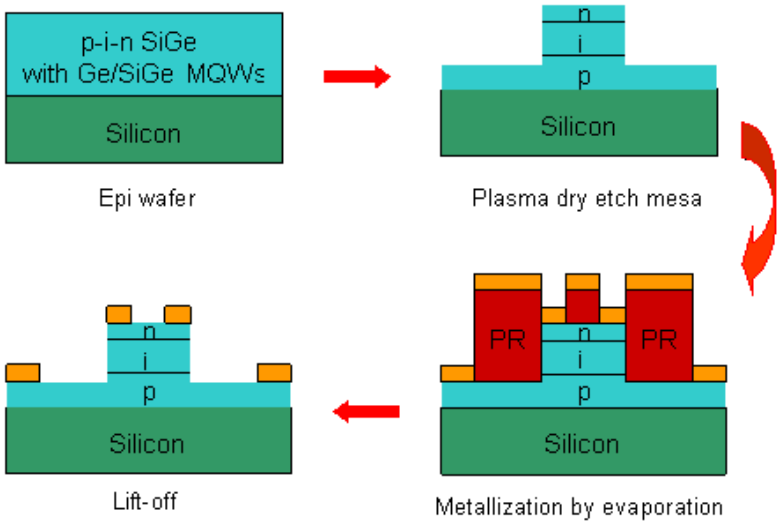


Figure 4.1: DC p-i-n diode device process flow.

Epi wafers were coated with 1μm thick photoresist (Shipley 3612) in the standard 4-inch SVG coater track, using the standard recipe without edge bead removal. The resist was then patterned, using optical lithography in the Karl Suss MA-6 aligner and developed in the SVG developer. The square mesas with different sizes ranging from 100×100 to 500×500μm were plasma dry etched to reach the bottom p-doped region with CF_4 etchant in the Drytek2 etcher.

Rectangular ring contact regions were patterned with 1.6μm thick photoresist (Shipley 3612), again using the SVG coater, Karl Suss aligner, and SVG developer. The size of the optical window inside ring contacts range from 80×80μm to 450×450μm Metal layers, including 20 nm Ti and 400 nm Al, were deposited by electron beam evaporation. The metal was lifted-off in acetone/methanol/isopropanol solvents and then annealed at ~375℃ for ~30 seconds in the rapid thermal annealer (RTA) to form Ohmic n- and p- contacts.

4.2 Modulator DC Operation

The cross section schematic of the DC PIN diode is shown in Fig. 4.2. It has a 400 nm relaxed boron-doped $Si_{0.1}Ge_{0.9}$ p-type buffer grown on silicon, an intrinsic region containing 10 pairs of strained quantum wells (including 10 nm Ge well and 16 nm

$Si_{0.15}Ge_{0.85}$ barrier) two 100 nm $Si_{0.1}Ge_{0.9}$ spacers, and a 200 nm arsenic-doped $Si_{0.1}Ge_{0.9}$ n-type cap layer.

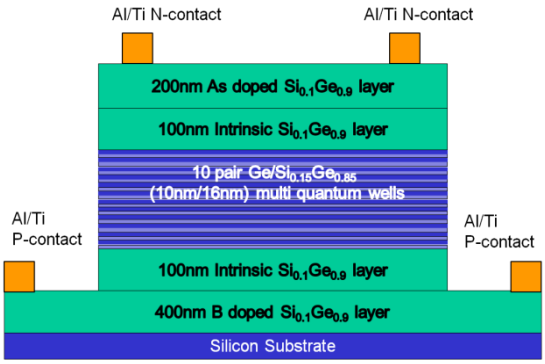


Figure 4.2: Schematic of the side view of PIN diode for DC measurements

The photo-absorption current is measured at room temperature and shown in Fig 4.3 below. The spectra show clear exciton absorption peaks at room temperature. In bulk Ge, an exciton absorption peak can be seen at low temperature [90], but such peaks are not usually clearly resolvable at room temperature. The appearance of room temperature peaks is characteristic of the quantum wells, and is explained by the increased carrier confinement which maintains the excitons. At zero applied voltage, there is also a clear shift of the direct optical absorption edge from its value in bulk, unstrained Ge (~0.8 eV at room temperature) to the lowest energy exciton peak position of ~0.88 eV. This shift can be explained as a combination of strain and quantum confinement. The peaks and the shift show empirically that, despite the lower-energy indirect conduction bands in the wells, there is strong quantum confinement at the zone center in the Ge conduction and valence bands. When an electric field is applied, there is a clear QCSE shift of the absorption edge to lower photon energies. Note also that the exciton peak width, ~8 meV half- width at half-maximum, has little or no apparent change with applied bias.

Since the Ge wells are under compressive strain, the heavy hole band becomes the topmost valence band, and the band-edge absorption peak is related to the heavy-hole exciton. The high responsivity without any bias voltage indicates that the i-region of this p-i-n device is highly intrinsic with a low background doping level, and hence the built-in field depletes the whole i-region and sweeps all photo-generated carriers to the

heavily doped regions where they are collected. This is also advantageous when these electroabsorption modulators are used as photodetectors.

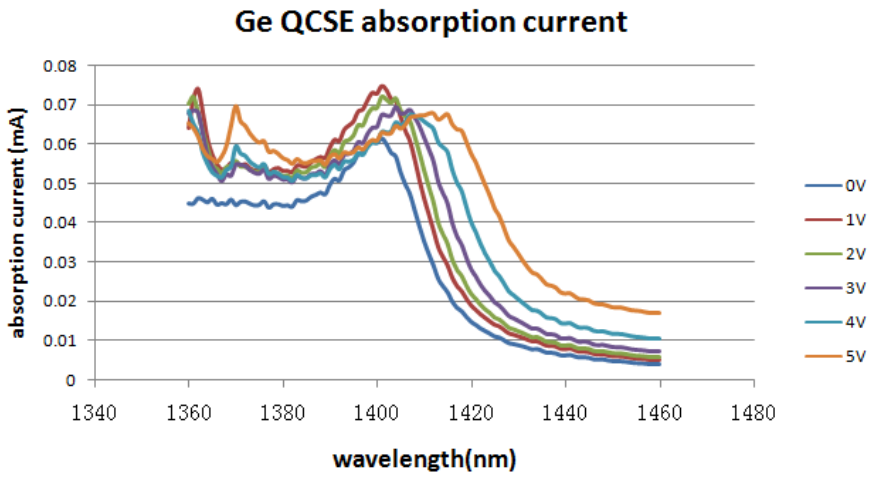


Figure 4.3: Optical absorption current measurement (DC) device size: 100×100μm

The current under 0 V bias is low, because there is more leakage current under reverse bias. Also the current at 5V reverse bias is higher than that at 4V for the same reason. That means that the material quality is not optimized yet. Due to the dark current issue, we can see the best operating range is below 5V.

In future applications, high contrast under a low voltage swing is required for the modulators. In this generation of devices, contrast ratio of almost 2 is achieved at 1410nm as the reverse bias changes by 3 volts. Also the n doping level and doping activation are relatively low and the n contact is not as low resistance as desired. In order to improve the contrast ratio for future applications, we use the following techniques: (1) longer time purge of reacting gases after the p doping growth and before the intrinsic region growth; (2) eliminate the intrinsic spacer and grow more pairs of quantum wells; (3) increase the doping level of n region to form better contact; and (4) use 15 seconds anneal with RTA at 500 ℃ after the growth to activate more n dopants.

Fig 4.4 shows the optical absorption spectra after the growth and processing improvements. It can be seen that on the left side of the figure, after the short anneal,

the material quality and the contacts have improved. We can see a clear trend of the exciton peaks becoming smaller and wider as the bias voltages increases due to reduced spatial overlap of the electron and hole states at higher electric fields. This is reflected in the decrease in absorption current as voltage increases. Most important, a contrast ratio of 2.4 is achieved with only a 1 V swing. This will be very useful for future applications.

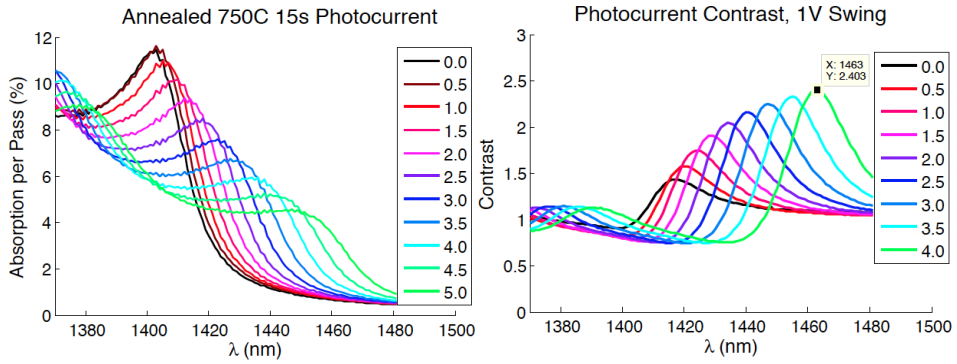
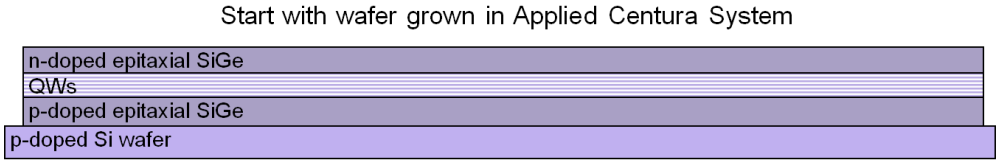


Figure 4.4: Optical absorption current measurement after the material and processing improvements

4.3 AC High-speed Modulator Fabrication

After the basic DC p-i-n diode is fabricated and tested, we observed QCSE (which we discussed in 4.2); the next step is to design and fabricate a high-speed modulator. We use the usual surface normal co-planar optical modulator structure. We started with the same epitaxial process we used in section 4.1 and fabricated devices with different mesa sizes (ranging from 100×100 to 500×500μm) with standard CMOS compatible processes. We also used the standard ground-signal-ground (GSG) probe configuration to couple the RF signal to the devices.



(a)

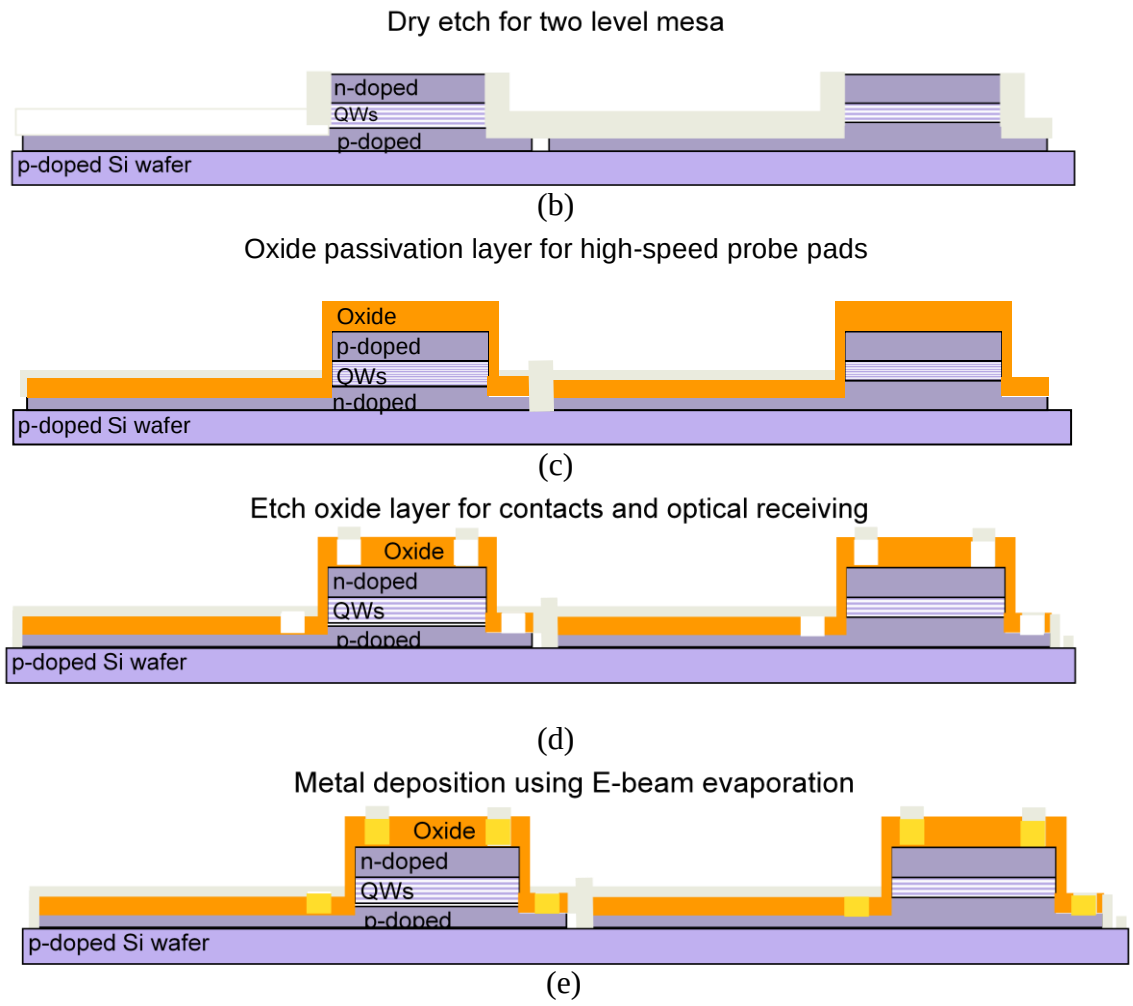


Figure 4.5: High-speed modulator device process flow (a) epi wafer; (b) two mesa etch; (c) oxide passivation deposition; (d) double contact for p and n regions; (e) metal deposition for contacts

After the wafer is fully grown by RPCVD, the processing steps for the high speed modulator are illustrated in Fig 4.5: (1) n contact mesa; (2) p contact mesa (3) oxide passivation layer deposition (4) oxide window opening etching (5) metal deposition for p and n contacts. The detailed processing steps are explained below.

The first two steps (Fig 4.5 (b)) define the two-level mesa. 1μm thick photoresist (Shipley 3612) is spun for 30 seconds at 5000 rpm. A post bake of 120 seconds at 90^{o} C follows. A Karl Suss MA-6 aligner and standard optical lithography are used. Exposure time is 1.1 second. The wafer is then developed using LDD26W developer for 60 seconds. The first mask defines the upper mesa which extends down to the p-contact region. The second mask isolates the different devices by etching completely

down to the silicon substrate. Sulfur hexafluoride is used as the etchant. To better control the etch depth, a dummy wafer with the same epitaxial structure is etched to calibrate the etch rate immediately before etching the real devices.

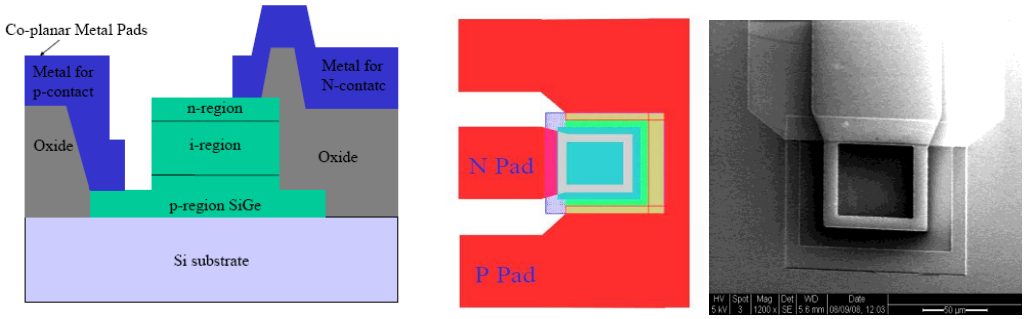
The second step is to deposit an oxide insulation layer using LPCVD to deposit a 600nm thick silicon dioxide layer at 400^{o}C for 30 minutes. The pressure is roughly 350mtorr. Silane and oxygen are used in this process without phosphine doping.

The third step is back side oxide etching. We use 20:1 buffered oxide etchant (BOE) to get better uniformity. The front side is covered by photoresist during this etch.

The fourth step is to pattern the optical window used for light input and to define the contact openings for transmission line evaporation. The mask process uses standard optical lithography, and the oxide is wet etched by 20:1 BOE. The etching rate of undensified low-temperature oxide in 20:1 BOE is 74nm/min, and the oxide thickness is ~600nm in total. Since the wet etch is isotropic, and the side etch will potentially lead to a short circuit, the over etch must be less than 1 minute. We control the etching by monitoring the residual oxide thickness every 2 minutes during the wet etch. We use a Nanospec film thickness measurement system, which is a non-contact, spectro-reflectometry tool that can measure transparent thin film thickness by processing the reflected light from the sample.

The fifth step is contact metallization. We use a metal liftoff approach by first using a mask to deposit photoresist to form a protection layer, then e-beam evaporating the contact metal over the patterned photoresist. 30nm of titanium (Ti) and 1μm of aluminum (Al) are deposited. Ti helps the metal adhere to the wafer while Al helps to produce reasonable contact coverage over the three-dimensional transmission line structures. A 20 second HF dip before metal evaporation is very important to achieve high-quality, low-resistance Ohmic contacts. Since the oxide opening is 600nm deep, the contact metal has to be thick enough to get reliable metal coverage over the step at the edge of the oxide. After the evaporation, a standard metal lift-off process in an ultrasonic bath is used to remove the resist and excess metal,

leaving the desired contact pattern. After lift-off, the contacts are alloyed using rapid thermal annealing (RTA) at 375 ℃ for 30 seconds.



(a) (b) (c)

Figure 4.6: (a) Schematic side view of the modulator; (b) schematic top view of the modulator; (c) SEM top view of the modulator

Fig 4.6 (a) shows the side view of the high-speed optical modulator. Fig 4.6 (b) shows the top view. These two pictures clearly indicate the structure of the device. The device is a p-i-n structure with MQWs in the i region. The standard GSG pad configuration is used and separated by densified oxide deposited by LPCVD. The deposition time is 30 minutes and temperature is 400 ℃ Fig 4.6 (c) shows an SEM picture from the top. We can clearly see the 3D structure of the metal contact, which can easily break at the edge between the SiGe and the oxide. The key for an effective contact is to ensure over etch of the oxide on SiGe before an adequately thick metal contact layer is subsequently deposited.

4.4 Summary

As discussed above, a p-i-n diode is fabricated on a SiGe quantum well structure and QCSE with high contrast ratio and clear exciton signal were observed. High-speed devices were fabricated based on the same processes which are CMOS compatible. High-speed optical measurement results will be discussed in the next chapter.

Chapter 5 High Speed Characterization

5.1 High Speed E-O Response

5.1.1 Measurement Setup

To demonstrate high-speed modulation of the device, the setup up in Fig. 5.1 was used to measure the electro-optical response. All measurements were performed on wafer using a Cascade MicroTech Air Coplanar Ground-Signal-Ground (GSG) Wafer Probe and a Cascade Summit Probe station. The RF driving voltage was generated by a pulse generator, and it was sent to the device by the transmission line contact pattern fabricated on the device. Also, a reverse bias of about 3V was applied by the voltage source to keep the device within its working regime. A tunable laser with an operating range from 1260-1680nm was used. Light was coupled into the device through a single mode fiber with a lensed tip. The transmitted light was collected by an objective lens and coupled into a multimode fiber. The light was detected and processed by a digital communication analyzer (DCA).

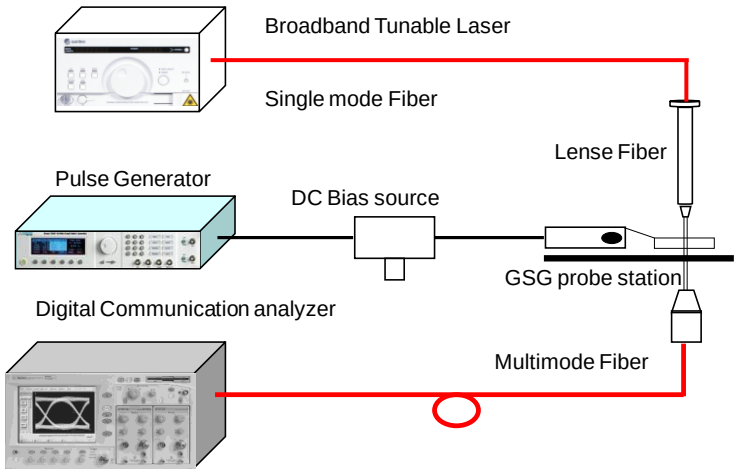


Figure 5.1: High speed measurement setup

The AC response of different sized devices, ranging from 100μm to 6μm, was measured. The incident laser power was about 1mW. A high-frequency RF signal was sent onto the device through RF cables that operate up to 26GHz. The DCA sampling rate can reach 13GHz. We used two function generators, one of which can generate square wave pulses up to 3.5GHz; the second can generate sine waves up to 20GHz.

5.1.2 Large Signal Measurements

Fig.5.2 shows the optical eye diagram of the modulator at 3.125GHz. The laser output power is 1mW, at a wavelength of 1408nm. The operating characteristics and wavelength response vary from device to device on the wafer, mostly due to non-uniformity of the device structure and materials introduced during thin-film deposition and device fabrication. The diode dark current is at a level of 10nA at low reverse bias. At -5V, the device shows soft breakdown and the dark current increases to ~1μA for the 100μm device, the dark current gradually decreases to about~800nA as the device size decreases to 100μm. However, the optical absorption current is always at ~60μA, from 100 μm to 10μm. With 1mW input power, the dark current is almost two orders of magnitude lower than the optical absorption current and thus can be neglected in the measurement. The modulation depth is roughly 12% and the period is 320ps.

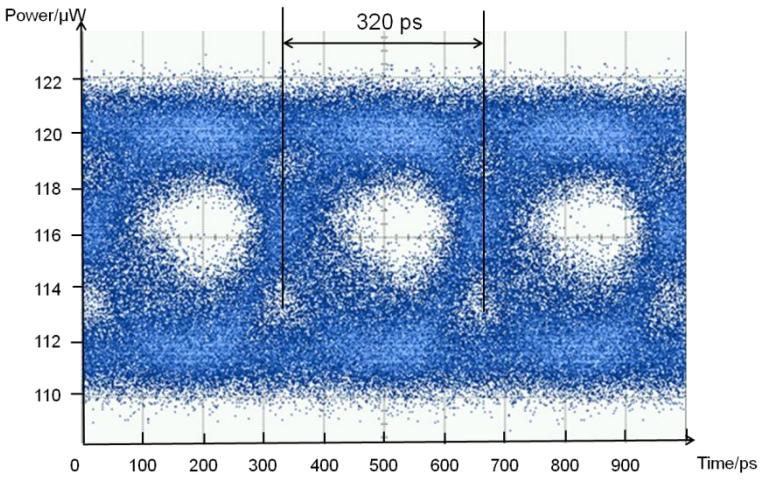


Figure 5.2: Optical eye diagram of the 40μm device at 3.125GHz (Measured in HP Labs, Palo Alto, CA)

Fig 5.3 shows the 10GHz E-O response of 40μm device. It can be seen that the period is 100ps, and the modulation depth is lower than 2%. It can be seen that the noise level is very high, most likely due to n-type contact resistance problems in the fabrication. 10GHz E-O response test was performed on devices with different mesa sizes; it is observed from the readings of the DCA that the modulation amplitude has little variation from 10μm to 50μm and decays significantly when the mesa size is larger than 50μm.

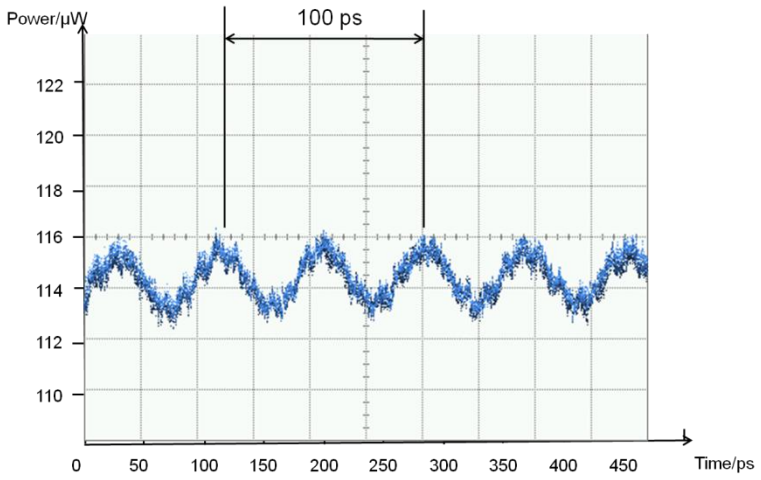


Figure 5.3: High Speed Electrical-Optical Response at 10GHz for 40μm device (Measurement reference)

5.1.3 Small Signal Measurements

Accurate modeling of the equivalent circuit of the fabricated devices will help us to understand the physical limitations of the high-speed operation. By combining the modeling with real data we can reach conclusions that allow future improvement in material deposition and device fabrication.

5.1.3.1 Basic Model

The two port system shown in Figure 5.4 can be characterized by Z (impedance) parameters at low frequencies. The equations for the impedance parameters can be written as:

$$V_1 = \quad Z_1 + {}_1 I \quad {}_1$$

(5.1)

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \tag{5.2}$$

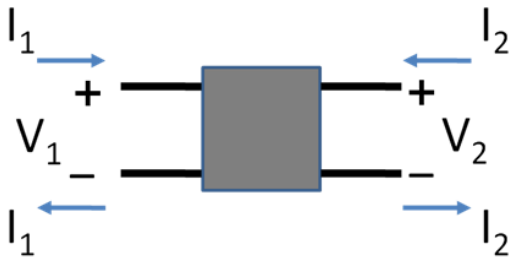


Figure 5.4: Two-port system model: variable definitions

Open-circuit ports need to be used to determine the Z parameters experimentally, For example, Z_{11} is determined easily once output port 2 is open-circuited (I_2=0), and measuring voltage V_1 and current I_1 allows direct computation of Z_{11}, which is

$$Z_{11} = \left. \frac{V_1}{I_1} \right|_{I_2=0} \tag{5.3}$$

At high frequencies, the approach mentioned above does not work. Since it is impossible to have open or short circuits, a different method needs to be used. Another set of parameters, called scattering parameters (or S-parameters), can fit into the high frequency scenario very well. They relate the incident and reflected voltage waves rather than port voltages and currents, as shown in Figure 5.5. The source and load terminations are Z_0. The high frequency two port relation using S-parameters can be expressed as

$$E_{r1} = s_{11} E_{i1} + s_{12} E_{i2} \tag{5.4}$$

$$E_{r2} = s_{21} E_{i1} + s_{22} E_{i2} \tag{5.5}$$

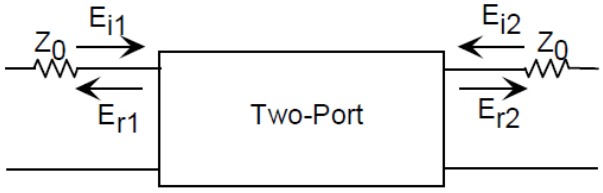


Figure 5.5: High frequency two-port system model

The S parameters can be found by driving one port and measuring at the other port. They can be determined from the following equations:

$$s_{11} = \frac{E_{r1}}{E_{i1}} = \Gamma_1 \tag{5.6}$$

$$s_{21} = \frac{E_{r2}}{E_{i1}} \tag{5.7}$$

S_{11} is the input reflection coefficient and S_{21} is the gain relating the output reflected wave to the input wave. S_{12} and S_{22} can be deduced in a similar way. Also, the reflection can be written as

$$\Gamma = \frac{Z_1 - Z_0}{Z_1 - Z_0} \tag{5.8}$$

where Z_1 is the load impedance. With this model, a more intuitive picture can be used to model the behavior of the device.

5.1.3.2 Measurement Results

The setup of the small signal measurement is very similar to that of the large signal electro-optical response. The only difference is that the exciting optical signal is very small in amplitude and the response was collected and analyzed by a network analyzer.

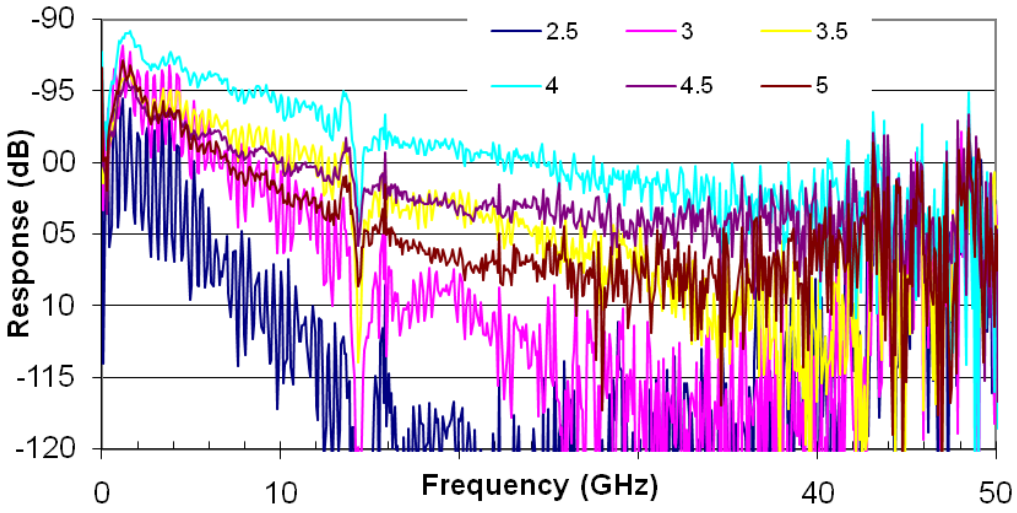


Figure 5.6: Small signal measurement for 6μm×6μm device (Experimental data taken by Lars Thylen)

Fig. 5.6 shows the measurement results for the small signal electro-optical response under different biases. The wavelength of the input laser is tuned at 1420nm, and the bias ranges from 2.5 to 5V. The device size is 6μm.

It can be seen from the graph that the best optical response is obtained at 4V of reverse bias. The modulation bandwidth can be roughly estimated at ~30-35GHz. This is reasonably consistent with rough estimation of the capacitance of the diode and the resistance of the test circuit.

There is an abrupt dip at 13GHz, regardless of the bias voltage. The same behavior was observed in devices with different sizes ranging from 6μm to 100μm. This lack of dependence on device size is potentially due to the measurements being limited by the coupling of the high speed probe. Also, the resonant effect can be seen under different bias voltages. This factor of unknown origin is modeled in the small signal model as well. The most probable reason for this is high resistance in the N-contact. The metal Fermi level can possibly be pinned near the valence band maxima of Ge, making the contact behave more like a Schottky barrier contact instead of an Ohmic contact. This will create parasitic inductors and capacitors, as seen in the model. In order to eliminate these the Ohmic contact must be improved, possibly by

either Fermi level de-pinning [91] in the N-type Ge or more heavily doping the Ge to produce a thinner barrier through which tunneling can occur.

5.1.3.3 Real Device Model

An initial attempt to find an equivalent circuit for the SiGe modulators was based on measurements of electrical reflection (S_{11}) by connecting a microwave network analyzer to the pad (Refer to the circuit of Fig. 5.7) via a high-frequency probe. The following information and assumptions are used. (Refer to the circuit of Fig. 5.7):

- The probe pad is modeled as a transmission line with finite length to take into account the phase shift of the measurement signal. The transmission line has been chosen as a coplanar waveguide (CPW) with signal conductor width 100 μm and gaps between signal conductor and each ground plane of 50 μm. These are the standard dimensions for GSG probe. The CPW length has been chosen in the range 200-300 μm based on the layout and the fact that the exact probing point may change slightly between probings.

- A LCL-network is introduced to model any parasitic effects due to the geometry change (taper) from the pad to the modulator.

- The intrinsic characteristics of the modulator are described by two capacitors and one resistor. C_{add2} is used to model the intrinsic capacitance of the absorption layer while R_{add2} is a series resistance which could be due to the contact. The values of C_{add2} and R_{add2} are obtained from the low-frequency part of the measurement range. A smaller extrinsic capacitance C_{p2} starts to influence the behavior at slightly higher frequency. A second series resistance R_{sub2} can be obtained from the fit of the model to the measured response up to about 14GHz by allowing a circuit simulation program to iteratively find the best values of the device parameters. This resistance is assumed to be due to finite isolation in the silicon substrate of the leads and pads.

- Fitting the CPW and taper model parameters to reflection measurements up to 70GHz provides a fairly good overall result, but a small deviation between model and measurements remains in the region approximately from 10 to 40 GHz with an

apparent resonant frequency independent of the device area. As the area of the device decreases, the resonant frequency stays the same. The area independence indicates that the effect is probably intrinsic to the device; this is because the contact resistance between the metal and the semiconductor is high and the response is RC limited.

There is thus a remaining uncertainty about the reason for the deviation between model and measurement, but the main characteristics of the modulator frequency response are otherwise well modeled by this fitting procedure.

Fig 5.7 below shows the equivalent circuit of the high-speed modulator based on the assumptions and information from above. It can be seen later in Fig 5.8 that intrinsic modulator properties, taper transmission line and probe pad can be modeled reasonably accurately. However, there are some unknown resonances in the measurement that cannot be integrated to any of the categories listed; this will be discussed later.

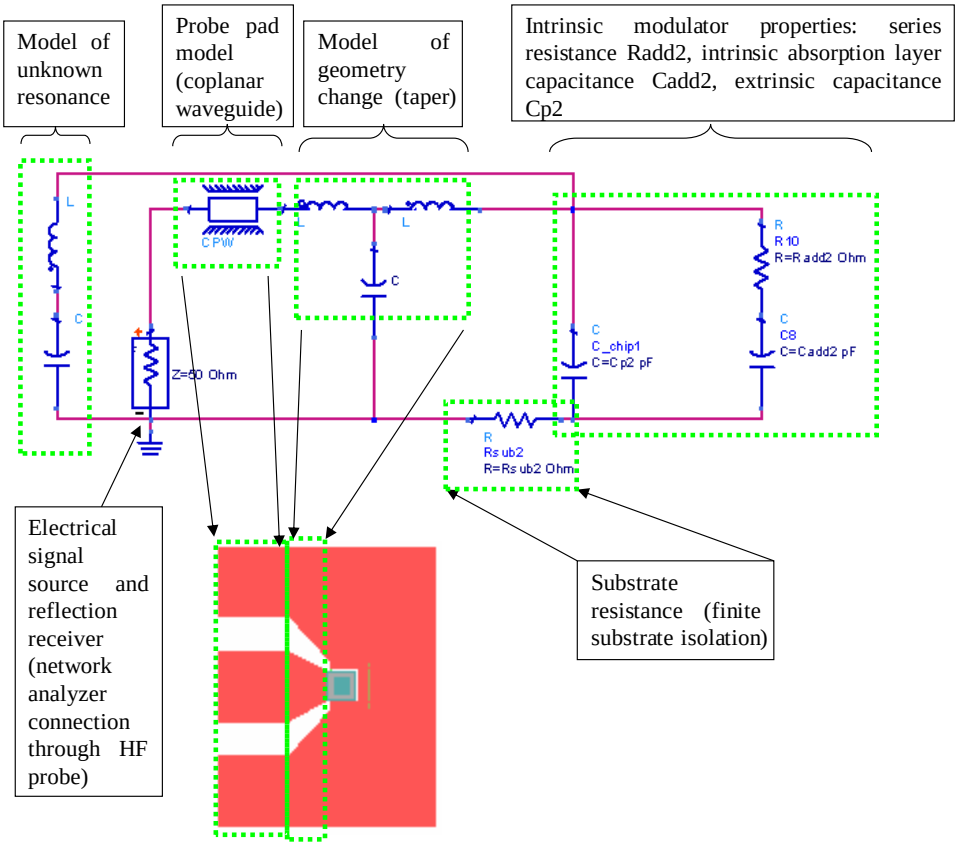


Figure 5.7: Equivalent circuit with comparison to modulator layout

Fig 5.8 shows the measured and simulated behavior of S_{11} for a 20μm×20μm modulator diode with integrated probe pads at V_{bias}=-2.5V in the frequency range from 100MHz to 70 GHz. The modeled curve agrees reasonably well with the measured results. This shows that, generally, the device is well simulated.

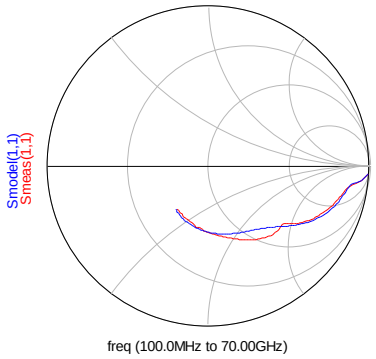


Figure 5.8: Smith chart of measured and modeled results for 20μm×20μm device (blue fitted, red measured)

Equivalent circuit models will provide valuable information to help improve the high-speed performance of the devices. The physical basis and the circuit model values will provide feedback to modify the device design and fabrication processes. From the data and analysis above, we can see that in order to have clearer signal, we need to improve the signal-to-noise ratio and understand the irregularities, such as the resonant behavior that occurs at 13GHz.

5.2 Pump Probe Measurement

Multiple quantum well (MQW) structures have applications in modulators, high-speed photodetectors and all-optical switching elements. The potential for high operating speed is essential. As MQW related devices are scaled to high optical powers and speeds, it is becoming increasingly important to understand the dynamics of photo-generated carriers in the active region. Determining the carrier transit time will help us know the fundamental operating speed limit. Because the measurements described above were probably limited by the measurement technique, rather than the

intrinsic device properties, a measurement method that determines the intrinsic behavior of the device was needed.

5.2.1 Method

Optical pump–probe measurements can be used to obtain information on ultrafast phenomena. The general principle is the following. A sample is pumped by a very short pump pulse, which generates some distribution of carriers (or other modification) in the sample. After an adjustable time delay (controlled with an optical delay line), a probe pulse is incident on the sample, and its transmission or reflection is measured. By monitoring the probe signal as a function of the time delay, it is possible to obtain information on the decay of the pump-generated excitation or on other processes initiated by the pump pulses. The probe signal is typically averaged over many pulses, and a fast photodetector is not required. The temporal resolution is fundamentally limited only by the pulse duration. The pump-probe technique is normally used to determine the carrier lifetime and optical nonlinearity of a semiconductor material. [92-97].

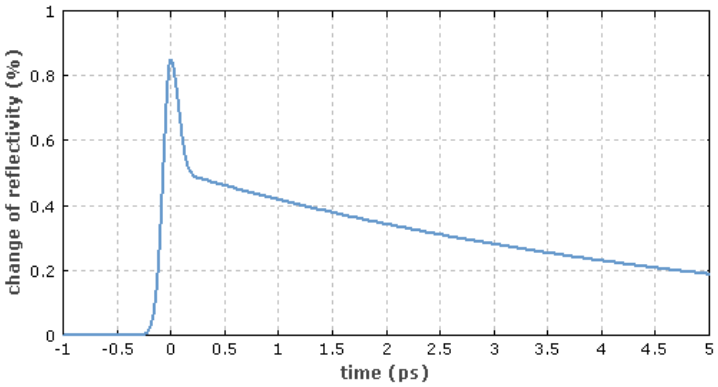


Figure 5.9: Pump probe measurement of reflectivity change

The wavelengths of pump and probe beam do not need to be identical. A so-called two-color pump–probe measurement, based on two synchronized sources of short pulses (e.g. a laser and an optical parametric oscillator, or two parametric oscillators pumped with the same laser) has additional capabilities in ultrafast spectroscopy. Pump–probe measurements can be used, for example, to monitor the recovery of a

saturable absorber after its excitation, the speed of diffusion of photoexcited carriers, or the melting of a sample after being hit by an intense pulse.

5.2.2 Experimental Setup

There are several pump probe techniques available today. They include non-linear, collinear, and heterodyne pump probe measurements. The heterodyne method is an ingenious modification of the pump–probe technique developed recently. The pump and probe pulses are distinguished by inducing a small frequency shift between them and by the use of a heterodyne detection scheme. This technique allows separate extraction of the gain and refractive index dynamics in the waveguide and works for orthogonally, as well as parallel, polarized pump and probe pulses.

The heterodyne detection scheme works by imposing a small (MHz) frequency shift between the pump and the probe beam. By mixing the output mode of the device with a third, reference pulse at yet another frequency, the probe beam can be separated by detecting at the proper beat frequency between probe and reference. Acousto-optic modulators (AOMs) are appropriate for frequency shifting the beams in the range of tens of MHz. In the case of laser systems with repetition rates larger than the AOM frequency shifts, the detection process can be understood by considering the shifts imposed by the AOMs on each of the laser mode frequency components individually. In the case of a laser system with a repetition rate much lower than the AOM induced frequency shifts, the beat frequency acquires a large number of lower sidebands, closely spaced by the repetition rate. Also, the duty cycle is much lower. Both issues require a higher selectivity and sensitivity for the detection process. We show here, that the use of balanced detection in combination with lock-in frequency filtering satisfies these demands and additionally provides a direct measurement of phase and amplitude.

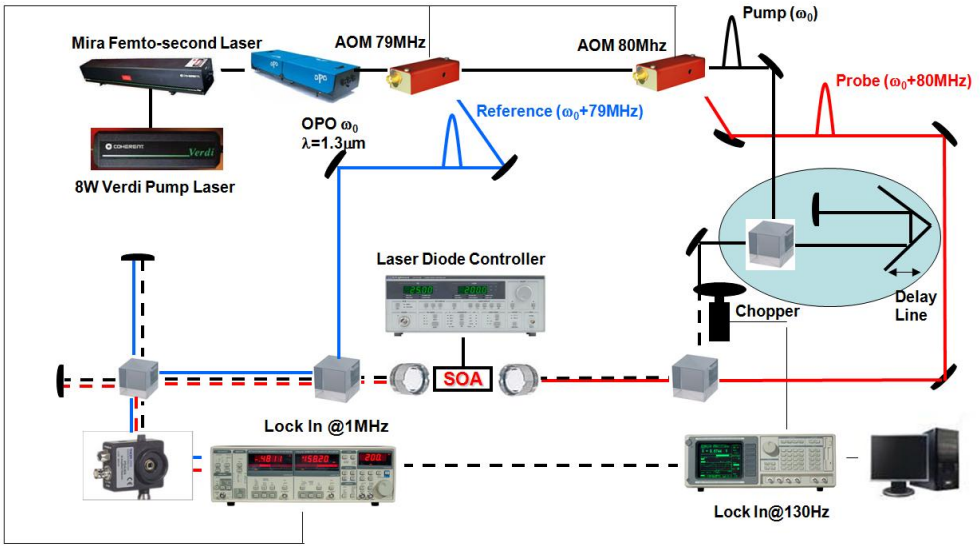


Figure 5.10: Pump probe measurement setup

Fig 5.10 shows the measurement setup. The laser source is a Mira™ 900 Modelocked Titanium:Sapphire(Ti:S) Laser pumped by an 8W Verdi pump laser. It acts as an idler for the Optical Parametric Amplifier at 1.2-1.4um and produces 350 fs pulses. The system has a reference pulse. The pump and probe frequencies are based on the reference frequency. The pump pulse is obtained by deflecting the laser beam with an AOM driven at 79 MHz. By controlling the radio-frequency (RF) power driving the AOM, the intensity of the pump pulse can be adjusted with high precision. The probe pulse is obtained by deflecting the beam transmitted through the first AOM with a second AOM driven at 80 MHz. The probe intensity is controlled by the RF power driving the second AOM. Pump and probe beams are recombined by a non-polarizing cube beam-splitter and focused onto the device by a high numerical-aperture (NA) aspheric lens. The light at the output of the device is collected with an equally high NA lens, focused onto an aperture (A) for spatial selection, collimated by a lens (L) and directed into a Mach-Zehnder interferometer. The transmitted beam from the second AOM is the reference beam that can be optionally injected onto the device by a second cube beam-splitter (which has to precede the pump and probe by 1ns in order not to perturb the semiconductor optical amplifier(SOA)), or can travel outside the device and be combined, using cube beam-splitters, in the Mach-Zehnder interferometer with the signal from the device.

The probe signal transmitted through the device, which is frequency shifted by 80 MHz, interferes with the reference beam.

5.2.3 Measurement Result

In this characterization, we used the actual modulator structure for the pump probe measurement in the setup described above, however, the measured response was not limited by the device parasitics. After propagating through the SiGe modulator with suitable delays, the probe and reference beams were simultaneously incident on a slow detector. The amplitude of the difference frequency (1 MHz) was detected using a high-frequency lock-in amplifier. This signal is proportional to the transmission of the modulator. The energies of the pump and probe pulses were 650fJ and 20fJ, respectively.

The response of the modulator depends strongly on the pump wavelength and bias voltage, Typically, the modulator transmission varies abruptly over a few picoseconds and recovers to its initial transmission value within several tens of picoseconds. Fig 5.11 shows the relative transmission variation of the modulator, immediately after perturbation from the pump pulse vs. the bias voltage for various pump wavelengths. For low bias voltage (typically below 4 V), the modulator response is weak. For large bias voltage, the response depends on the pump wavelength. It can be seen that at 1.4μm wavelength, the transmission variation is strongest.

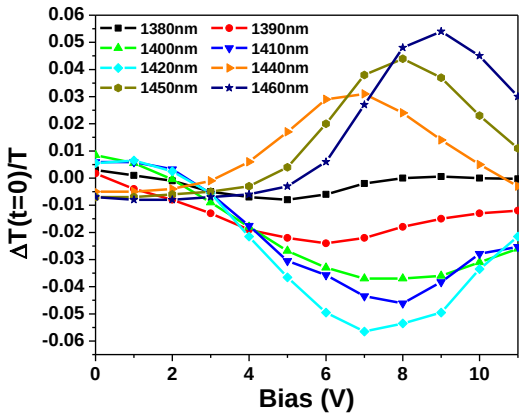
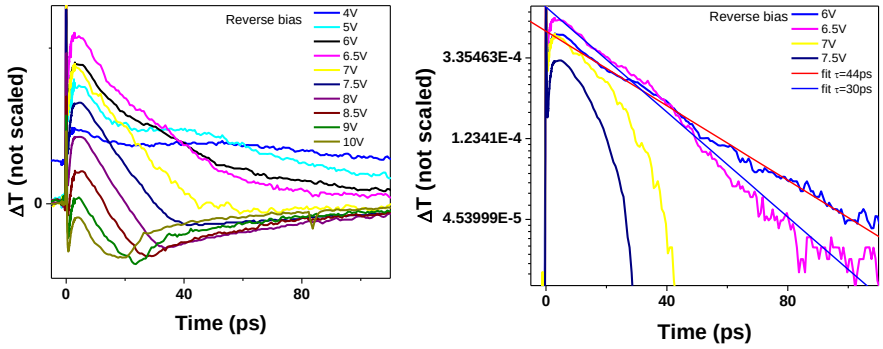


Figure 5.11: Relative transmission variation of the modulator, immediately after perturbation from the pump pulse, vs the bias voltage for various pump wavelengths.

When the pump wavelength is fixed at 1.4μm, the modulator exhibits a significant response for bias voltages larger than 4V, and the recovery time decreases with increasing bias. The minimum value of the recovery time obtained was 20ps at 11V. At this particular wavelength, photo-carriers (generated by the pump pulse) reduce transmission of the absorber.

For a wavelength of 1.43μm, the response is similar. In this case, the transmission initially increases before recovering to its initial value. For voltages between 4 and 8 V, the recovery time decreases with increasing voltage. For the higher bias voltages we observe a smaller response and overshoot of the transmission change. This can be explained by the large QCSE and detuning pump and probe wavelength with the modulator absorption peak.



(a) (b)

Figure 5.12: (a) Differential transmission spectroscopy at 1.43μm (b) Fitting for lifetime at 6V and 6.5V

Fig 5.12 (a) shows the differential transmission spectroscopy at 1.43μm, it can be seen that the lifetime of the carriers decreases as the voltage/electric field intensity increases. The signal is very weak when the voltage is lower than 4V. This is because the modulator material structure is not yet optimized. There are intrinsic spacers, a thick buffer layer and too many quantum wells in the structure, leading to low electric field on each quantum well. An improved device design including better selection of parameters such as thickness and number of quantum wells can enable better measurement results. Fig 5.12 (b) shows the fitting curve of the carrier recovery time. The fitting curves show that under 6V, the carrier lifetime is 44 ps and under 6.5 V it reduces to 30ps. It can be seen on the plot that at 11V the lifetime is under 10ps, indicating >100GHz modulation capacity in the Ge/SiGe quantum well materials system.

5.2.4 Summary

High-speed measurements of both large and small signal are taken and the data is displayed and analyzed in this chapter. 3.125GHz eye diagram is observed. Also small signal measurement indicates 30-35GHz of modulation bandwidth. However, due to the limitation of the material structure design and the imperfections in device fabrication, the measurement results are not optimized. Pump-probe measurement shows that the modulation capability of the SiGe quantum well structure can further extended.

Chapter 6 Conclusions

6.1 Summary

Innovative SiGe optical devices are a very important part of the optical interconnect technology roadmap. This dissertation extends previous experimentation of the potential and fundamental challenges of optical interconnect technology. SiGe is the best material system in terms of compatibility, speed, power and cost. One of the critical issues for SiGe-based photonics has been the lack of an effective high-speed optical modulator. Several silicon based devices based upon index modulation have been reported, but none of them are adequate to make a compact, low power, low cost modulator. Our work focuses on the modulator utilizing quantum confined Stark effect (QCSE), the strongest mechanism of optical modulation in order to get the optimum solution for the interconnect systems.

Chapter 2 discussed the theoretical background of SiGe bandgap engineering. In order to design a suitable structure, a thorough discussion on the band structure of Si, Ge and SiGe alloys was presented. Even though Si and Ge are indirect band gap materials, Ge-rich SiGe still has a local minimum at zone center and has a sharp absorption edge with a high absorption coefficient just above the direct bandgap. By designing the structure properly, a type-I aligned quantum well system can produce strong QCSE for modulation applications.

Chapter 3 explored the thin film deposition of SiGe and its associated properties. The material is deposited in a commercially available RPCVD system manufactured by Applied Materials. Specific growth topics regarding lattice relaxation, surface roughness, dislocation generation and selective growth were studied. Growth rate was characterized under a range of growth conditions, such as temperature, pressure, gas flow which are rather specific to our quantum well applications. High quality Ge-rich SiGe thin-films were successfully grown on Si substrates. 2D XRD mapping showed

the buffer to be fully relaxed. Relaxed buffer thicknesses as thin as 400 nm and low surface roughness suitable for quantum well growth were achieved with our novel growth technique. Multiple quantum well structures were deposited directly on the relaxed buffer layer. TEM images indicated that low dislocation density and sharp quantum well profiles were achieved, indicating high quality quantum well structures. Also, selective growth of SiGe on Si substrates with patterned oxide mask was studied. A high-quality multiple quantum well modulator was successfully grown for waveguide modulator applications.

Chapter 4 discussed the fabrication and DC characterization of QCSE modulators. Simple p-i-n diodes were fabricated to measure the photo absorption current. A high contrast ratio with low voltage swing was achieved by material growth and device fabrication improvements. Also surface normal high-speed coplanar optical modulators were fabricated. All the fabrication processes are CMOS compatible and cost effective.

Chapter 5 discussed high-speed E-O response measurements of the modulator and a pump probe measurement to test the intrinsic high-speed potential of these devices. In a large signal measurement, an eye diagram of 3.125 GHz was observed. Large signal modulation up to 15GHz was detected as well. Small signal measurement of the S_{11} parameter showed modulation up to about 35 GHz. Pump probe measurements of the carrier dynamics showed that recovery time decreased as bias voltage increased. Under 11V bias, the carrier recovery time decreased to less than 10 ps, indicating >100GHz modulation capability. The high voltage needed for optimal response was a result of the undoped buffer layers, large number of quantum wells and moderately thick quantum well barrier layers. With further optimization of these parameters, operational voltages <2V should be possible.

6.2 Future Work

The demonstration of high-speed optical modulation of SiGe based devices is just the beginning of research in the area of Si-based photonics for optical interconnects. This

opens the doors to novel design and fabrication of high-speed optical modulators that can be practical for system integration in on-chip optical interconnections. More work on device structures and relevant materials growth and device fabrication needs to be done.

6.2.1 Material Growth Improvements

As many problems emerged from our measurement results, a number of them came from the materials: (1) n type doping is ineffective. There is a need to have higher doping levels with a high activation rate to engineer the Fermi level. Better doping control with arsenic and phosphorous needs to be achieved. (2) High quality thin buffer layers. Practical applications in optical communications require single optical mode waveguide and cavity structures. The former needs thinner buffer layers for stronger coupling and the latter needs higher quality material with fewer dislocations to reduce absorption. Moreover, high quality quantum well material also improves the I-V characteristics and reduces signal to noise ratio (3) Better control over selective area growth.

6.2.2 Cavity Modulator

The Asymmetric Fabry-Perot (AFP) modulator cavity allows increased interaction between light and active material in a smaller form factor. After the Ge/SiGe QW QCSE electroabsorption, α, is experimentally determined for each sample, a range of acceptable front and back mirror reflectances, R_f and R_b, can be determined from the AFP design equation [98].

Currently, the DC characteristics of the fabricated device showed clear and high contrast with low voltage swing. The next step is to improve the monolithic device fabrication process and material deposition to match the cavity parameters.

6.2.3 Waveguide Device

One of the natural evolutions of modulator device design is a waveguide structure. It has several advantages: (1) Small dimension and potentially high speed (2) Easy to integrate (3) Easy to control the absorption length and get high contrast ratio There are several designs for low operating voltage, high-speed waveguide modulators. Currently we are working on selective growth based waveguide structures [93].

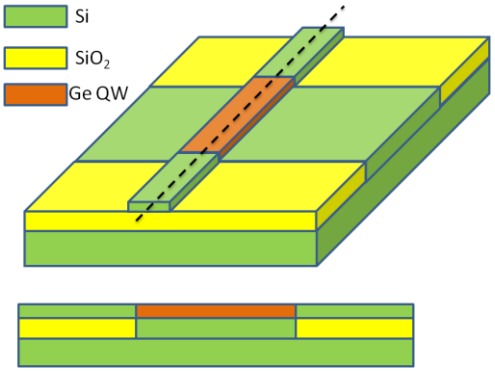


Figure 6.1: Ge quantum well waveguide modulator with SOI bus waveguide

The schematic of a newly proposed device is illustrated in Fig 6.1. The input and output passive waveguides are single mode SOI waveguides, 500nm wide and 300nm high. Between the input and output SOI waveguides is the active modulator section. In this region, the top Si layer and the buried oxide layer (BOX) of the SOI substrate are removed completely. Si is grown selectively from the bottom handle substrate of the SOI wafer to fill the BOX region and act as the bottom cladding for the waveguide modulator. The active waveguide modulator core in our design consists of 10 pairs of Ge/SiGe quantum wells sandwiched in the intrinsic region of a vertical p-i-n structure.

Currently the optical properties of the structure have been simulated, and the material growth has been calibrated as well. Further fabrication and measurement efforts need to be carried out.

6.2.4 Group IV Laser Integration

An off-chip laser is the solution for today's optical interconnect. However, this will eventually be a cost barrier and performance limitation for optical interconnect

technology development. Searching for the solution of efficient light emission from group IV based materials is still one of the utmost important missions. Among the multiple possible solutions, we believe that Ge-rich, tensily strained GeSn alloy is the most promising path to pursue based on theoretical calculations and experimental results [100-104]. Most of the challenges in GeSn alloy material are the low solubility of Sn in Ge and thermodynamic instability. The lattice mismatch between Sn and Ge is even larger than that of Ge and Si. Our effort is to grow a Ge-rich GeSn alloy on a Si substrate with low dislocation density relaxed structure. If we can make that type of structure direct bandgap, it will truly open the door to group-IV based integrated optical interconnects.

Appendix A

The description below is the full description of the SiGe multiple quantum well structure.

Operating pressure: 40 Torr Carrier gas flow: hydrogen 12.5 slm

Step 001: 1000^{o} C oxide blow-off bake for 5 minutes

Step 002: Cool down to 740^{o} C and stabilize the temperature and gas source for 60 seconds

Step 003: SiH_2Cl_2 flow 100 and deposit Si for 120 seconds

Step 004: Cool down to 395^{o} C for $Si_{0.1}Ge_{0.9}$ alloy growth

Step 005: GeH_4 flow 40 sccm, SiH_4 flow 35.8 sccm, 100ppm B_2H_6 mixed dopant flow of 100 sccm with mixed ratio of 50%. Growth temperature 395^{o} C. Grow 200 nm of p-doped $Si_{0.1}Ge_{0.9}$ alloy for 25 minutes

Step 006: Temperature ramp up to 850^{o} C and anneal for 30 minutes

Step 007: GeH_4 flow 40 sccm, SiH_4 flow 35.8 sccm, 100ppm B_2H_6 mixed dopant flow of 100 sccm with mixed ratio of 50%. Growth temperature 395^{o} C. Grow 200 nm of p-doped $Si_{0.1}Ge_{0.9}$ alloy for 25 minutes

Step 008: Temperature ramp up to 750^{o} C and anneal for 30 minutes

Step 009: Purge all gases for 5 minutes

Step 010: GeH_4 flow 40 sccm, SiH_4 flow 35.8 sccm, Growth temperature 395^{o} C. Grow 100 nm of intrinsic $Si_{0.1}Ge_{0.9}$ alloy for 12.5 minutes

Step 011: GeH_4 flow 40 sccm, SiH_4 flow 60 sccm, Growth temperature 395^{o} C. Grow 16 nm of intrinsic $Si_{0.15}Ge_{0.85}$ alloy for 243 seconds

Step 012: GeH_4 flow 40 sccm, Growth temperature 395^{o} C. Grow 16 nm of intrinsic Ge alloy for 49 seconds

Repeat step 011-012 for 10 times to grow 10 pairs of quantum wells.

Step 013: GeH_4 flow 40 sccm, SiH_4 flow 35.8 sccm, Growth temperature 395^{o}C. Grow 100 nm of intrinsic $Si_{0.1}Ge_{0.9}$ alloy for 12.5 minutes

Step 014: GeH_4 flow 40 sccm, SiH_4 flow 35.8 sccm, 100ppm AsH_3 mixed dopant flow of 100 sccm with mixed ratio of 50%. Growth temperature 375^{o}C. Grow 200 nm of p-doped $Si_{0.1}Ge_{0.9}$ alloy for 25 minutes

Appendix B

This appendix gives the full fabrication process of high-speed modulator device.

Optical Two-level Mesa Lithography (Mask Mesa)

20 min singe at 120 ℃

Wafer prime for 40sec

Spin 3612 photoresist at 5000rpm for 40sec

2 min bake @ 90 ℃

Expose 1.2 sec @ 30mW/cm2 using Karl Suss Aligner Develop 60sec in LDD26W (1.2 μ m thick),

CF_4 Plasma etch, 100sccm O_2, 190mT, 500W, for 120seconds

PRX127 clean at 25 ℃ for 20 min

LPCVD Deposition

Tylan BPSG use recipe LTO400 at 400 ℃. The pressure is roughly 350mtorr. Silane and oxygen are used in this process without phosphine doping. Deposition time is 30 min

Back Etch

20 min singe at 120 ℃

Wafer prime for 40s

Spin 3612 photoresist at 5000rpm for 40sec

2 min bake @ 90 ℃

Dip in 20:1 buffered oxide etchant (BOE) for 6 min.Monitor the residual oxide thickness every 2 minutes during the wet etch. Use Nanospec to measure the thickness

Oxide window etching (Oxide Window Mask)

20 min singe at 120 ℃

Wafer prime for 40sec

Spin 3612 photoresist at 5000rpm for 40sec

2 min bake @ 90 ℃

Expose 1.2 sec @ 30mW/cm^2 using Karl Suss Aligner

Develop 60sec in LDD26W (1.2 μm thick),

Dip in 20:1 buffered oxide etchant (BOE) for 6 min.Monitor the residual oxide thickness every 2 minutes during the wet etch. Use Nanospec to measure the thickness

PRX127 clean at 25 ℃ for 20 min

Contact deposition (Contact Mask)

20 min singe at 120 ℃

Wafer prime for 40sec

Spin 3612 photoresist at 3000rpm for 40sec

2 min bake @ 90 ℃

Expose 1.7 sec @ 30mW/cm^2 using Karl Suss Aligner

Develop 60sec in LDD26W (1.2 μm thick),

Dip in 50:1 HF for 30 sec

Use e-beam evaporator to deposit 30nm of titanium (Ti) and 1μm of Aluminum (Al)

Rapid thermal anneal (RTA) at 375 ℃ for 30 seconds.

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