SI NANOWIRES FOR ADVANCED MICROELECTRONICS: MBE GAS-SOURCE GROWTH AND *in situ* DEVICES

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING
AND THE COMMITTEE OF GRADUATE STUDIES
OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

By

Qiang Tang

July 2003

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

_____

James S. Harris, Jr.
(Principal Adviser)

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

_____

Theodore I. Kamins

I certify that I have read this dissertation and that in my opinion it is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

_____

Bruce M. Clemens

Approved for the University Committee on Graduate Studies:

_____

Abstract

As devices in modern integrated circuits become smaller and smaller, the required sub-100nm feature sizes become difficult and expensive to produce. New nano-scale assembly technology, such as catalyzed or self-assembled growth of nanowires and quantum dots, may benefit integrated-circuit production by eliminating critical lithography steps. In these self-assembled systems, small features are formed using chemical reactions and/or crystal growth with limited or coarse lithography. Many metals have been used to catalyze Si nanowire growth. Among them, Ti exhibits a diffusivity and solubility in silicon at least two orders of magnitude lower than that of Au, Fe, Zn, Ni, or Co at the same temperature. Therefore, Ti-catalyzed silicon nanowires are more compatible with integrated-circuit components and applications.

Using $TiSi_2$ islands as a catalyst, we have grown Si nanowires by molecular-beam epitaxy (MBE) with Si_2H_6 as a gas source. Approximately one monolayer of Ti was deposited on Si substrates and then annealed at high temperature to form $TiSi_2$ islands, which can nucleate Si nanowires in the subsequent growth, with diameters mainly between 20 nm and 40 nm.

Analysis of images produced by reflection high-energy electron diffraction (RHEED), transmission electron microscopy (TEM), and scanning electron microscopy (SEM), show that most $TiSi_2$ islands are identified as C49-$TiSi_2$ with the orientation: Si[110]//$TiSi_2$[100] (~ 6% lattice mismatch) and Si(001)//$TiSi_2$(010). These islands do not nucleate Si nanowires, possibly due to a highly defective and strained interface with the Si substrate. Growth of Si nanowires is associated with nucleation by $TiSi_2$ islands with orientations other than C49. In these wires, better lattice matching at the $TiSi_2$/Si interface is observed for major crystallographic planes. This is likely due to a lower energy barrier and/or a

smaller driving force for Si atom attachment at the $TiSi_2$-Si resulting from the better lattice match. Additionally, abrupt changes in growth direction (kinking) frequently occur, typically accompanied by crystal twinning. Strain at the $TiSi_2$/Si interface is posited to be the main reason for the frequent twinning and kinking of nanowires.

The dopants As (donor) and B (acceptor) have been introduced during growth of Si nanowires. The *in-situ* p-n junctions produced by this technique, both inside the Si nanowire and between the Si nanowire and the substrate, display diode-like *I-V* behavior. A tungsten layer has also been deposited as a gate (electrically isolated) between the top contact of a wire and the substrate. The gated structures show modulation of the current through the wire, which demonstrates that surrounding-gate field-effect transistors made from Si nanowires are possible.

Acknowledgment

This work would have been impossible without the tremendous contributions of many individuals.

First and foremost, I would like to thank my advisor, Professor James. S. “Coach” Harris, for his support, guidance, and encouragement over the years. By sharing his broad knowledge of MBE and processing, and his profound insight into electronic devices, the years in his group have been a great learning experience. He has created an open research environment that gives incredible freedom to students in pursuit of their research objectives, fostering creative ideas, independent thinking, and self-guidance. This has been an invaluable experience that I will always cherish.

I would like to thank Dr. Theodore I. Kamins from the Quantum Research Group at HP Labs for generously sharing his broad knowledge of Si devices and processing with me. For more than two years, he has given me insightful advice in our many discussions on Si nanowires. I would also like to thank Dr. Kamins and Professor Bruce Clemens for reading my dissertation, Professor William D. Nix for serving on my oral committee, and Professor Stacey Bent for chairing my oral examination.

This work has benefited from many scholars and fellow students in our group. Xian Liu spent a tremendous amount of effort in converting system II from III-V growth to gas-source Si growth and in maintaining the system, without which this work can’t even start. I am indebted to Dr. Glenn Solomon, Dr. Dan Grupp, Dr. Byung Gook Park, and Barden Shimbo for very helpful and motivating discussions in “quantum meetings”. I want to express my extra gratitude to Dr. Grupp for his wonderful help on improving my oral presentation and writing of this thesis. C.C. Lin first brought the hands-on experience to our MBE systems and spent a lot of time on maintainance. Vincent Gambin and Mark

Wistey both not only served as resources of MBE machine knowledge, but also helped to keep our group computer server and the MBE computer controlling running smoothly. I also would like to thank Kai Ma, Xiaojun Yu and Junxian Fu for helping to maintain our MBE systems with enormous time and painstaking effort and for making the screw-tightening hours inside MBE lab happy time. My gratitude goes to Seth Bank and Homan Yuen for forcing the lab tidy, to Vince Lordi for help me with constructing various reciprocal lattice, to Hyunsoo Yang and Hopil Bae for fixing the RTA machine, to Yu-Hsuan Kuo for taking over system II, and to the rest of the Harris group, including Xin Jiang, Rafael Aldaz, David Jackrel, Alireza Khalili, Paul Lim, Vijit Sabnis, Ke Wang, Luigi Scaccabarozzi, Zhigang Xie, etc., for making my time in the group a wonderful memory.

I am also grateful to Gail Chun-Creech and Miho Nishi for keeping the huge Harris group running ruly and smoothly, to Dr. Ann Marshall for patiently teaching me the art of TEM, to Dr. Bob Jones for his help on SEM, to Professor Mike Kelly for his help on XPS, to Tim Brand for doing CMP on my wafers, and to the staff of CIS for their great job of keeping the cleanroom running.

My time at Stanford would not have been as enjoyable without the company of many friends. Thanks go to: Yaocheng Liu, Guanxiong Li, Zhi Liu, Dachen Chu, Nianxiang Sun, Roy Wu, Kevin C. Weng, Bernard Liu, Ruey-ven Wang, and many others.

Last and most, I would like to thank my parents, my parents-in-law, my wife, my sister, and my brother-in-laws, not only for their unending love and encouragement, but also for inspiring me to attain goals which I thought to be beyond my grasp.

Table of Contents

List of Tables

List of Illustrations

Chapter 1

Introduction

1.1 Motivation

Nanomaterials are found in both biological systems and manmade structures. In nature nanomaterials have existed for millions of years. Scientific work on nanomaterials can be traced back over 100 years. In 1861, the British chemist Thomas Graham coined the term "colloid" to describe a solution containing 1 to 100nm diameter particles in suspension. Around the turn of the last century, such famous scientists as Rayleigh, Maxwell, and Einstein studied colloids. In 1930, the Langmuir-Blodgett method for developing monolayer films was developed. By 1960, Uyeda had used electron microscopy and diffraction to study individual particles. At about the same time, arc, plasma, and chemical flame furnaces were employed to produce submicron particles. Magnetic alloy particles for use in magnetic tapes were produced in 1970. By 1980, a team led by Smalley and Kroto found spectroscopic evidence that C_{60} clusters were unusually stable. In 1991, Iijima reported studies of graphitic carbon tube filaments.

Research on nanomaterials has been stimulated by their technological applications. The first technological uses of these materials were as catalysts and pigments. The large surface area to volume ratio increases their chemical activity. Because of this increased activity, there are significant cost advantages in fabricating catalysts from nanomaterials. The properties of some single-phase materials can be improved by preparing them as nanostructures. For example, the sintering temperature can be decreased and the plasticity increased of single-phase, structural ceramics by reducing the grain size to several nanometers. Multiphase nanostructured materials have displayed novel behavior resulting from the small size of the individual phases.

Technologically useful properties of nanomaterials are not limited to their structural, chemical, or mechanical behavior. Confining electrons to small geometries gives rise to 'particle in a box'-type energy levels. This quantum confinement creates discrete energy states and can result in the modification of the electronic and optoelectronic properties of

semiconductors. In microelectronics, the need for faster switching times and ever-larger integration has motivated considerable effort to reduce the size of electronic components. Increasing the component density increases the difficulty of satisfying cooling requirements and reduces the allowable amount of energy released on switching between states. It would be ideal if the switching occurred with the motion of a single electron. One kind of single-electron device is based on the change in the Coulombic energy when an electron is added to or removed from a particle. For a nanoparticle this energy change can be large enough that adding a single electron effectively blocks the flow of other electrons. This nanoscale application of electron Coulomb repulsion is referred to as the Coulomb blockade.

Si nanowires refer to wire-like silicon crystals with cross-section dimensions of less than 100nm and length of more than several hundred nanometers. The small lateral size of the nanowires makes them very suitable for studying fundamental size and dimensionality effects in optical, electrical, mechanical applications [1,2]. Crystalline silicon does not show efficient light emission at room temperature, because of its band structure with an indirect band gap of ~1.1 eV and a small exciton binding energy (~15meV). One theoretically possible approach to enhance the optical transition in silicon is the relaxation of the k conservation rule due to the lateral spatial confinement in Si nanowires [3-10].

Si has been the most widely-used semiconductor material for integrated circuits, which is powering hundreds of millions of computers and other electronic appliances in the world and greatly influencing our life. As devices in modern integrated circuits become smaller and smaller, the fabrication processes, especially optical lithography, becomes increasingly difficult and expensive. Optical lithography is a printing method that used a light source and masks to transfer the layout of an integrated circuit onto Si wafers. As integrated circuits shrink, the smallest feature on the mask become smaller and smaller, and is now below 100 nm. The most advanced lithography in mass-production nowadays uses 193nm-wavelength light. As the shrinking continues, the deep-sub-100nm features will become difficult to produce, primarily due to the hurdles of deep ultraviolet optics and materials. Si nanowires, whose diameter can be smaller than 10nm, if assembled into integrated circuits (IC), will make IC transistors with feature sizes far below 100 nm possible. This will relax

the requirements of the lithography, helping to extend Si technology into future generations.

1.2 Silicon Nanowire Growth Review

1.2.1 Earliest Silicon Nanowire Growth: the Vapor-Liquid-Solid (VLS) Mechanism

1.2.1.1 Growth Methods

About 40 years ago, Wagner *et al.*. first discovered the Vapor-Liquid-Solid (VLS) mechanism[11-16], which seeded the recent boom of research attention on silicon nanowires and other semiconductor nanowires. They grew silicon whiskers by disproportionation of SiI_2 or by the hydrogen reduction of $SiCl_4$, both with small particles of metal, such as Au, Pt, Ag, Pd, Cu, Gd, Mg, Os, or Ni, as a catalyst. Since they used relatively large metal particles (normally larger than 100nm), the grown whiskers normally have cross-section dimensions of larger than 100nm. The VLS growth by hydrogen reduction of $SiCl_4$ was subsequently studied by Givargizov[17,18] and James[19].

Growth of silicon whiskers with $SiCl_4$ using gold as a catalyst occurs as follows[11]: A small particle of Au is placed on a {111} surface of a Si wafer and heated to 950°C, forming a small droplet of Au-Si alloy according to the phase diagram of Fig. 1-1. This is also schematically shown in Fig. 1-2 (a). A mixture of hydrogen and $SiCl_4$ is then introduced. The liquid alloy acts as a catalyst for the chemical process involved. The Si enters the liquid and deposits at the interface between solid Si and the liquid alloy, with a very small concentration of Au in solid solution. As this process continues, the alloy droplet becomes displaced from the substrate crystal and remains on top of the growing whisker, as shown in Fig. 1-2 (b).

Growth of silicon whiskers with SiI_2 using nickel as a catalyst occurs as follows[16]: approximately 1g of high-purity silicon, 1mg of nickel, and 0.84g of high-purity iodine are put into a reaction tube. The reaction tube is then evacuated to about 10^{-6} Torr, sealed and placed in a furnace with a temperature profile that has a gradient from 1000°C to 800°C.

The silicon source material and the impurity are located in the high-temperature region. Whisker growth was observed after about 10 minutes.

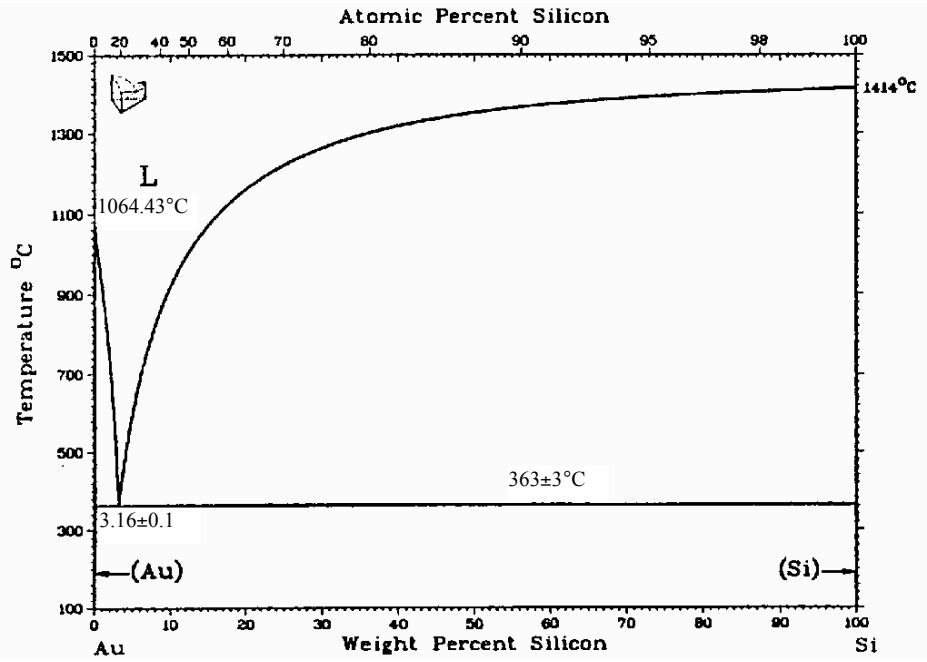


Figure 1-1. Au-Si phase equilibrium diagram[20].

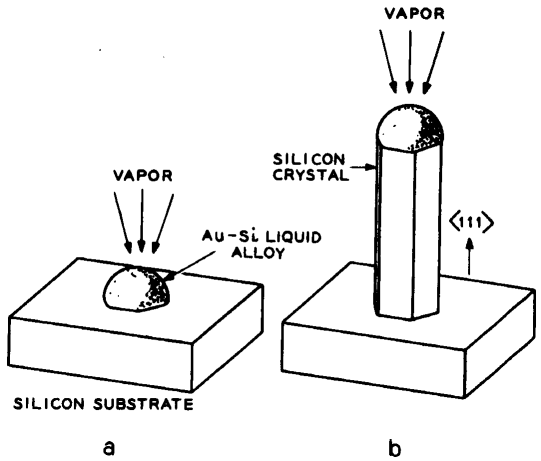


Figure 1-2. Schematic illustration describing silicon whisker growth by VLS. (a) Initial condition with liquid droplet on substrate. (b) Growing crystal with liquid droplet at the tip. [11]

The process uses the following disproportionation reaction[16]:

$$2SiI_2(g) \rightarrow Si(s) + SiI_4(g) \quad (1.1)$$

The reaction goes from right side to left side, with the production of SiI_2, at a temperature about 1050°C and a pressure of the iodine species above 80 Torr. The SiI_2 moves to a region of lower temperature, typically 900°C -1000°C, where the reaction goes to the right. Silicon is deposited and SiI_4 returns to the higher temperature region to combine with additional source silicon. It is assumed that the relatively small concentrations of added impurities do not affect the chemistry of the transfer process significantly.

1.2.1.2 Growth Direction and Nanowire Sidewalls [16]

The typical whiskers in the early VLS process were micron-sized needles growing in the <111> direction, with hexagonal cross-sections and {211} lateral faces, as shown in Fig. 1-3. There were also sub-micron whiskers with a growth direction of <111>, but they most frequently had {110} side faces, even though circular cross-sections or {211} side faces were also found. Whiskers growing along a [110] direction, with four {111} planes as the prismatic side faces, and twinned whiskers growing along a [211] direction were also observed[16].

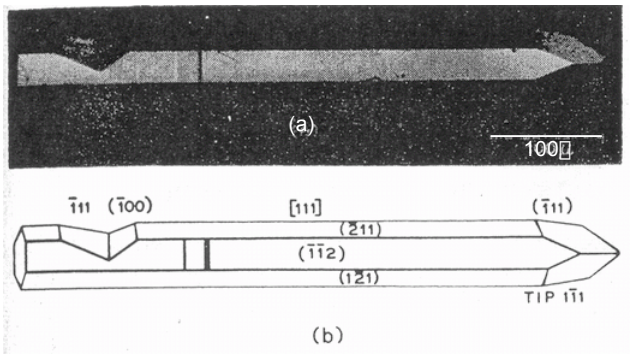


Figure 1-3. Silicon whisker morphology: (a) A typical silicon whisker. (b) Schematic drawing of the morphology of a <111> whisker. [16]

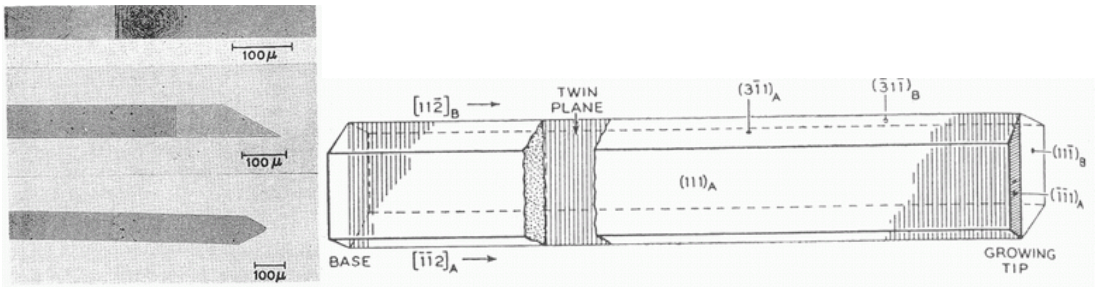


Figure 1-4. Silicon ribbon morphology. (a) Photographs of typical ribbons. (b) Schematic drawing of ribbon morphology. [16]

Other than whiskers, ribbon-shaped crystals with growth direction of <211> were also grown at the same time. The typical examples are shown in Fig. 1-4. Ribbons are twinned crystals, and a difference in morphology was also observed between small and large crystals. The submicron twinned crystals have large flat {110} faces, normal to the twin plane, which is one of {111}. The large twinned crystals, formed by the thickening of the smaller crystals, had large flat {111} external surfaces parallel to the twin plane[16].

These differences in morphology support a two-stage growth process. The first stage is very rapid, when the whisker lengthens without change in cross-section. Wagner *et al*. believed that the lateral faces of the whisker are determined by three factors: surface energy relationships, the growth kinetics at the solid-liquid (S-L) interface, and the direct vapor-solid (V-S) deposition on the sidewalls which may occur simultaneously during VLS growth[16]. Wagner *et al*. think these lateral faces probably have a minimum surface free energy. The subsequent thickening of the whiskers is a much slower process, when the exposed side faces are determined by the relative rates of nucleation and growth of steps on these faces[16].

According to Eaglesham *et al*.,[21] the surface energy of Si {110} planes is the highest, at 1.43 J/m^2, while the surface energy of Si {111} planes is the lowest, at 1.23 J/m^2, and that of Si {211} planes is in between, at about 1.30 J/m^2 as derived from [21]. Thus, a more likely explanation of the differences in morphology might be that the appearance of {110} planes at the earliest stage is due to the kinetics and thermodynamics of Si condensation at the S-L interface, such as a possible low interface energy between the liquid metal droplet and {110} planes, or that the precipitation of Si from the liquid metal droplet prefers {110} planes. During the subsequent thickening, the equilibrium shapes of the Si crystals were reached, which were bound by the lowest energy surfaces. This is in accordance with the fact that if the growth temperature is increased from 850 to 1050, the {110} side faces rapidly disappear by side-wall vapor-solid (V-S) deposition until the crystal is bound by six {211} planes.[12]

Further study[13] found that VLS whiskers with 24 or 3 side faces can also be grown, as shown in Table 1-1. The decrease of the number of side faces for increase of growth temperature is probably mainly due to the fact that {110} planes grow faster than {211},

which eventually cause the {110} planes to disappear, and the growth rates and their difference are higher at higher temperature. The transition from 6 side {211} faces to 3 {211} side faces is due to the different surface bonding configuration between $(\bar{2}11)$, $(1\bar{2}1)$, $(11\bar{2})$, and their opposites, $(2\bar{1}\,\bar{1})$, $(\bar{1}2\bar{1})$, $(\bar{1}\,\bar{1}2)$, which causes one set of the planes to grow faster.[18]

Table 1-1. Morphology of prismatic growth faces as a function of VLS deposition temperature. [13]

Temperature range (°C)	Number of side faces	Index of faces
< 850	24	{110}, {211}, ~{311}
~ 850 - 1000	12	{110}, {211}
~ 1000 - 1100	6	{211}
> 1100	3	{211}

It was also shown that whisker crystals of silicon do not contain axial screw dislocations or other line defects during growth, contrary to the traditional "Frank mechanism" explanation of whisker crystal growth. The Frank mechanism is based on the concept of crystal growth with the aid of a structural defect. The self-perpetuating steps for adding new layers are offered by a screw dislocation, which emerges at the growth interface. It is not necessary for two-dimensional nucleation and it is possible for growth to occur at a relatively small supersaturation. Also, the number of the dislocations in the substrate crystal does not affect the VLS growth observably. Even more interesting is that, dislocation-free crystals can be grown any substrate from dislocation-free to those plastically deformed with dislocation densities of up to 10^7 dislocations/cm^2. Silicon whiskers grown from dislocations terminating at the substrate surface are not observed. [12]

1.2.1.3 Growth Rate

A simple model of the calculation of the VLS growth speed is as follows[12]: A simple model of the calculation of the VLS growth speed is as follows[12]: At steady state VLS growth, the number of silicon atoms that enter the liquid from the vapor is equivalent to the number that are deposited at the solid-liquid interface. The driving force of this Si

atom flux is a concentration difference ΔC across the liquid alloy of thickness L. It is assumed that the shape of the liquid alloy is disk-like and convective mixing in the liquid is negligible. Fig. 1-5 shows a section of the silicon liquidus, Si_L, along with the deposition isotherm, T_E. Without vapor deposition, the composition of the liquid will be C_E, which is the equilibrium concentration. While under steady state VLS growth, the composition of the liquid is C_L at the liquid-vapor interface and C_g at the liquid-solid interface. The difference between C_E and C_g is the supersaturation required for nucleation and growth of new crystal layers, although it may be very small.[12]

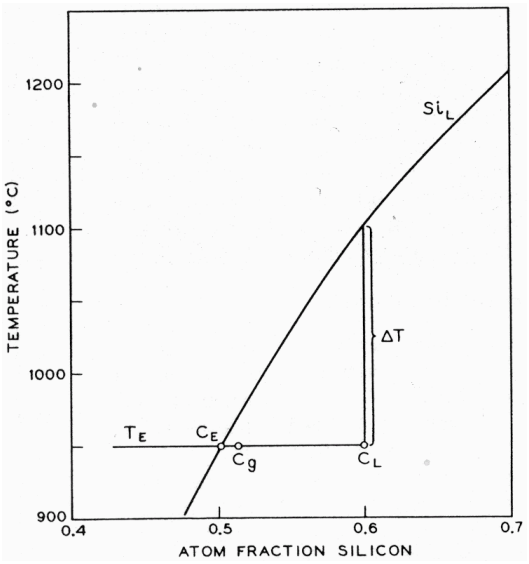


Figure 1-5. Section of the Au-Si phase diagram. [12]

The concentration gradient in the liquid disk is given by

$$\Delta C / L = v / D \tag{1.2}$$

where v is the speed of advancement of the Solid-Liquid interface and D is the diffusion coefficient of silicon in the liquid alloy[12]. As is shown by Fig. 1-5, for a given v, D, and L, the concentration difference in the liquid ΔC (C_L-C_E) (atom fraction) refers to a liquidus supercooling ΔT. According to homogeneous nucleation theory, maximum ΔT is about 300°C for pure Si or a liquid Si alloy. If ΔT is greater than 300°C, homogeneous nucleation in the liquid alloy may happen because the supercooling is high enough. For this maximum

□T, □C can be about 0.25 for T = 950°C during VLS growth. For example, given L = 10^{-2} cm, D = 5 _ 10^{-5} cm^2/sec, and T_E = 950°C, the critical growth velocity v_{max} is approximately 3.5 mm/hr [12].

For a given total gas flow f (cm^3/sec), a $SiCl_4/H_2$ mole ratio m_R and a reaction tube of cross section A (cm^2), the VLS growth rate v (cm/sec) can be estimated by the following equation:

$$v = (f\, m_R\, M) / (\square\, A\, V_0) \tag{1.3}$$

where M = molecular weight of $SiCl_4$, V_0 = standard volume of perfect gas, and □ = density of solid silicon[12]. Eq. (1.3) implicitly assumes that the flow rate of a dynamic system is high, the condensation coefficient for the liquid alloy is one and the disproportionation reaction is absent. It also assumes that silicon atoms on the side faces of the growing crystal do not migrate to the liquid. For f = 6 cm^3/sec, m_R = 0.014, and A = 5 cm^2, the VLS growth rate v is calculated as 0.3 mm/hr. For these conditions in the temperature range from 950°C to 1100°C, the calculated growth rate is only slightly smaller than the observed value for these conditions and the temperature between 950°C and 1100°C.

From the above discussion, it is evident that a sudden decrease in deposition temperature, T_E, during VLS growth results in a sudden increase in □C and therefore □T. During the transient, the □T can become large enough for homogeneous or heterogeneous nucleation. Fig. 1-6 shows a silicon crystal which was originally grown at 1000°C. During growth, the temperature was suddenly reduced to 600°C for about 30 sec and subsequently raised to 950°C. The breakup of the liquid alloy is so dramatic that it leads to the formation of a large number of small crystals which are in random orientation relative to the main crystal[12].

A more detailed study regarding the growth rate of VLS growth on a (111) Si substrate with the chloride ($SiCl_4$+H_2) process and with Au showed that thin whiskers grow slower than thick ones, which was plotted in Fig. 1-7 (a) [18]. Curves 1 to 4 correspond to different molar concentrations of $SiCl_4/H_2$, therefore to different supersaturations. Fig. 1-7 (a) reveals that there is a critical whisker diameter at which growth totally stops. In other

words, the growth rate reduces due to the decrease of supersaturation [18]. According to the Gibbs-Thomson effect the decrease of supersaturation as a function of whisker diameter d can be given as

$$\Delta\mu_{wire} = \Delta\mu_{bulk} + 4\Omega\gamma/d \quad (1.4)$$

where

$\Delta\mu_{wire} = \mu_{wire} - \mu_{vapor}$ and $\Delta\mu_{bulk} = \mu_{bulk} - \mu_{vapor}$.

μ_{wire}, μ_{bulk}, and μ_{vapor} are the effective chemical potentials of Si in a whisker, in the bulk, and the vapor phase, respectively[18]; d is the whisker diameter, γ is the specific surface free energy of the whisker, and Ω is the atomic volume of Si. For very small alloy droplets, growth is impossible. The reason is that the large wire surface-area-to-volume ratio gives rise to higher effective chemical potential for a whisker than for the vapor phase. However, when the droplets agglomerate and grow until the critical diameter is reached, the growth becomes possible.

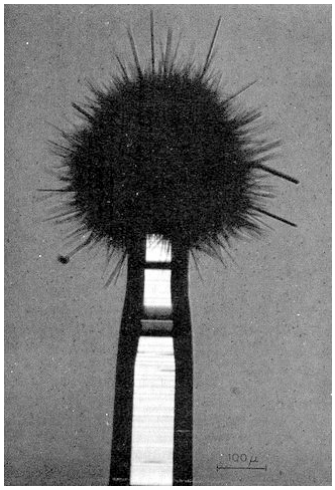


Figure 1-6. Uncontrolled VLS growth resulting from nucleation of silicon crystals in liquid alloy by sudden decrease of growth temperature. [12]

The data in Fig. 1-7 (a) are well-described by a model of the form

$$v = b\,(\Delta\mu_{wire} / kT)^2, \quad (1.5)$$

where v is growth rate, and b is a kinetic coefficient independent of supersaturation[18]. The fit is plotted in Fig. 1-7 (b). The temperature dependence of the kinetic coefficient gives the activation energy of VLS process, which is about 48 kcal/mole[18].

In Fig. 1-7 (b), the extrapolated intercept of the 1/d axis determines the critical diameters d_c. For these diameters and for the given overall supersaturation in the gas phase the real supersaturation in the droplet near the L-S interface becomes zero and the VLS process stops.

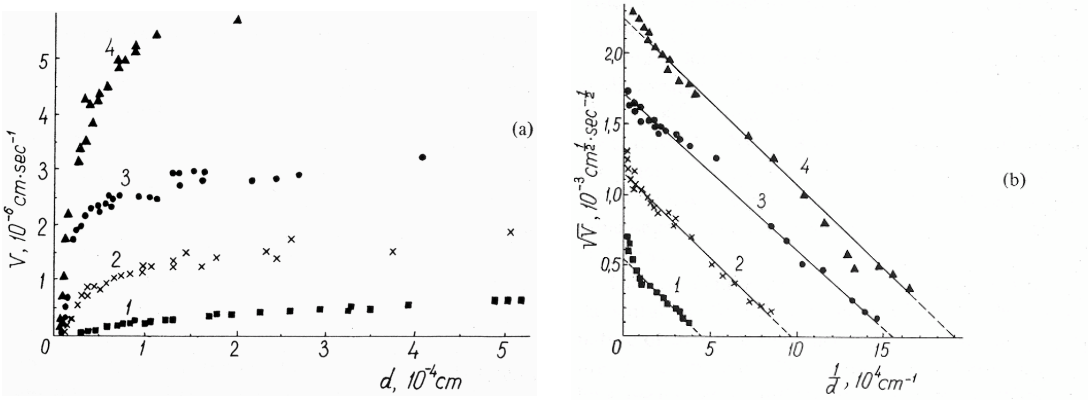


Figure 1-7. (a) Measured growth rate of VLS silicon whiskers as a function of their diameter for various molar ratios of $SiCl_4/H_2$; the ratio increases in the order 1 to 4. (b) Fitting the data of (a) in coordinates $v^{1/2}$ versus 1/d. [18]

Bootsma and Gassen studied the growth rate of Si whisker VLS growth with silane and Au[22], presumably for whiskers which were thick enough so that the last term in Eq. (1.4) is negligible in comparison with $\Delta\mu_{bulk}$. Therefore, no correlation between whisker thickness and growth rate needs to be considered. They used the expression from the kinetic theory of perfect gases in which the growth rate v, due to the number of effective collisions of vapor molecules on a surface is given by

$$v = \alpha (p/\sigma) \quad (M/2\pi RT). \tag{1.6}$$

For the case of decomposition of SiH_4 molecules and the formation of a solid phase Si, with a vapor pressure much smaller than the pressure of the impinging SiH_4 molecules, the variables are defined as follows:[22]

p, T - pressure and temperature of SiH_4,

M - M_{Si}^2/M_{SiH4},

M_{Si}, M_{SiH4} - molecular weight of Si, SiH_4,

ρ - density of solid Si,

R - gas constant.

In Equation (1.6) the factor α represents the efficiency of the collision process or the fraction of the impinging molecules SiH_4 yielding Si. The factor depends on the substrate surface temperature, T_s, and is generally written as

$$\alpha = \alpha_0 \exp(-E / RT_s), \quad (1.7)$$

where the activation energy, E, and the temperature-independent factor, α_0, are characteristic for the decomposition reaction[22]. The growth rates of the whiskers in the length direction, dl/dt, are of the order of 100 times higher than those in width, dw/dt. Values of α_0 and the activation energy, E, were calculated from log(v) – $1/T_s$ plot and are listed in Table 1-2. As expected, the activation energy for longitudinal growth is significantly smaller than that for width growth, which confirms that the alloy droplets at whisker tips do act as a catalyst[22].

Table 1-2. Values of E and α_0 calculated from the rates of growth of the whiskers in the length direction and of the thickness growth of substrate and whisker[22].

	v	E (kcal/mole)	α_0
Si	dl/dt	11.9	1.0
Si	dw/dt	15.5	0.031

1.2.1.4 Rate-limiting Step

Identification of the rate-limiting step is of great importance in crystal growth. The problem is a very complicated one in the VLS process because it involves three phases and

at least two interfaces (vapor-liquid and liquid-solid), and because the materials are deposited by chemical reactions.

The VLS process is schematically shown in Fig. 1-8. There are four steps: (1) mass-transport in the gas phase; (2) chemical reaction on the vapor-liquid interface; (3) diffusion in the liquid phase; (4) incorporation of the material in a crystal lattice[18]. Step (3) is not a potential rate-limiting step because thick whiskers do not grow more slowly than thin ones although the diffusion length is longer for thicker whiskers. Step (1) is also not a rate-limiting step because the kinetic coefficient depends heavily on temperature, while the mass transport in the gas phase usually obeys a power law (n ≈ 1.5 – 2). Thus either step (2) or step (4) can either or both be the rate-limiting step(s) [18].

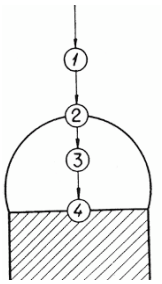


Figure 1-8. Various steps of the VLS process. [18]

Bootsma and Gassen[22] claim that step (2) is the rate-limiting step, based on the observation that the longitudinal growth rates of Si and Ge whiskers were proportional to the partial pressures of the hydrides. However, the above argument can not exclude the possibility that step (4) is the rate-limiting step. Another argument in favor of step (2) as rate-limiting was the observation that the longitudinal growth rates of SiC whiskers were dependent on the nature of the liquid-forming agent[18].

One the other hand, there are one argument in favor of step (4) as the rate-limiting step. It is that the rare <211> growth direction whiskers grow faster than the thick <111> direction ones. The <211> direction whiskers are supposed to have stepped liquid-solid interfaces, which is known to be able to increase growth rate compared with the smooth {111} interfaces[18], because of a reduction in the activation energy of nucleation.

1.2.1.5 Branching and Kinking[14]

The majority of silicon crystals prepared by the VLS technique, under isothermal conditions, grow in a [111] direction. It has been proposed[11] and confirmed[14] that this particular growth direction arises because the solid-liquid interface is a single (111) plane, as shown in Fig. 1-9. It has been shown that the interface can be very stable during VLS growth[13]; the stabilizing factor is very likely a result of interface kinetics.

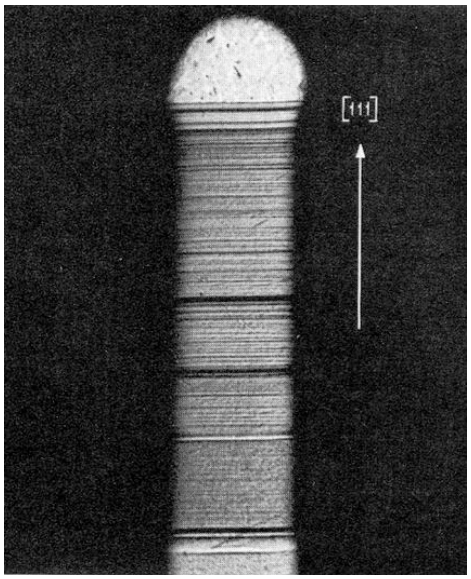


Figure 1-9. Etched section of a [111] oriented Si crystal doped with phosphorus during isothermal growth. Magnification approximately 50X. The pronounced bands indicate the introduction of dopant during growth, whereas the fine bands are produced by fluctuations in growth rate. [14]

The most likely process of branch and kink formation during vapor phase growth is due to codeposition of impurities. Impurities which satisfy the conditions of VLS growth may condense on an already grown whisker crystal and then new whiskers can be grown from there. An alternate model for kinking has been proposed. The model is based on the assumption that a lateral temperature gradient can change the morphology of the S-L interface and therefore change the direction of crystal growth. In the experiments which verified this theory, the temperature conditions during VLS growth were changed from isothermal to nonisothermal. The crystals were doped with phosphorous before, during, and

after completion of the kinking process, and etched on a plane which contains the axial directions of the kinked crystal. A [111] to [$\bar{1}$11] kink is shown in Fig. 1-10, where the kinking was caused by exposing the right side of the growing crystal to a higher temperature than the left side. From the position of the doping striations, it is obvious that during isothermal conditions, the crystal grew perpendicular to the (111) plane. However, the introduction of a lateral temperature gradient caused a change in interface morphology. In addition to the original interface, the ($\bar{1}$11) plane forms the other facet of the interface. The growth rate perpendicular to the newly formed ($\bar{1}$11) interface is slower than on the (111) plane because the new interface is in a region of higher temperature. The new interface grew in area while the old one shrank until finally the old (111) interface disappeared. During this process, the interface shifts from the (111) plane to the ($\bar{1}$11) plane. Further VLS growth proceeds in the [$\bar{1}$11] direction. Both the (111) and the ($\bar{1}$11) interface planes remain planarity during the kinking process. [14].

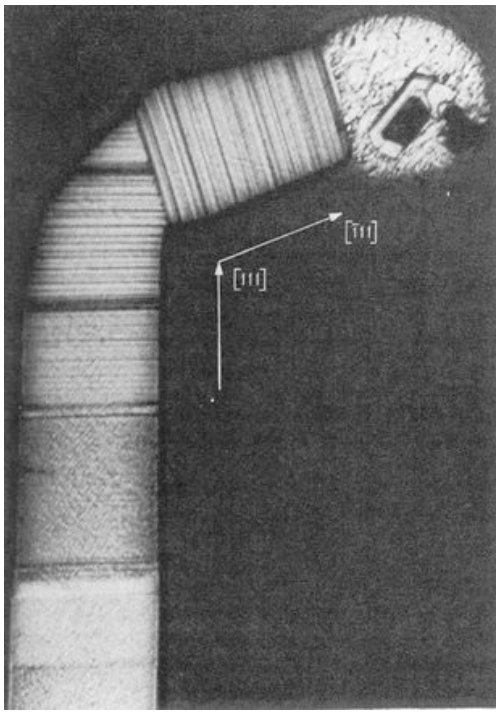


Figure 1-10. Etched section of a [111] to [$\bar{1}$11] kinked silicon crystal doped with phosphorous. Magnification approximately 100X. [14]

It is evident from Fig. 1-10 that the area of the S-L interface changes during the kinking process. This area expands at first and then returns to its original value after kinking is completed. The change in interfacial area imposes a restriction on the contact angle of the liquid alloy droplet, which can cause rupture of the droplet and, hence, lead to the formation of branch crystals. A time-lapse sequence of one such process was shown in [14].

It was also shown that a sudden increase or decrease in temperature can cause branching[14]. The volume of the liquid droplet during the VLS growth process is dependent on the deposition temperature as a result of the liquidus phase relationship of the particular alloy system. This feature has been used to change the diameter of silicon crystals during VLS growth by proper changes of the deposition temperature[12]. It has been noted that such changes must be made gradually in order to avoid instability of the liquid droplet. A sudden increase in temperature, for example from 1000°C to 1100°C in 10 sec, will usually cause instability. For such a big temperature change, the volume of the droplet will expand by about 13%. The vapor-phase reaction cannot provide the required amount of silicon sufficiently rapidly to satisfy the new phase equilibrium. As a result, the extra amount of Si will be dissolved from the VLS crystal, while the S-L interfacial area remains the same as that for the 1000°C growth condition. Because of this and the fact that the contact angle between the alloy droplet and VLS crystal is larger at higher temperature, the liquid alloy will extrude over the side of the crystal. Eventually it will wet the side faces for the purpose of increasing the interfacial area and maintaining a stable contact angle configuration. The individual droplets will cause formation of branch crystals or kinks as VLS growth continues. A typical example of this process is shown in the time-lapse sequence in Fig. 1-11, where two crystals were initially grown at 1000°C, then the temperature was rapidly raised to about 1100°C[14]. Fig. 1-11(a) shows the droplet configuration during the rise in temperature. In Fig. 1-11(b), taken at maximum temperature, the droplet has increased its contact area by wetting the side faces of the crystal. Subsequently, the temperature was reduced to about 1000°C. The next two photographs (Fig. 1-11 (c-d)) show the resulting growth morphology at different times. The liquid broke into smaller droplets giving rise to branch growth. Similarly, a sudden

decrease in temperature can also cause the alloy droplet at the tip of the VLS crystal to be unstable and small droplets to be separated from the meniscus region of the droplet. These small droplets then give rise to formation of branches during subsequent VLS growth[14].

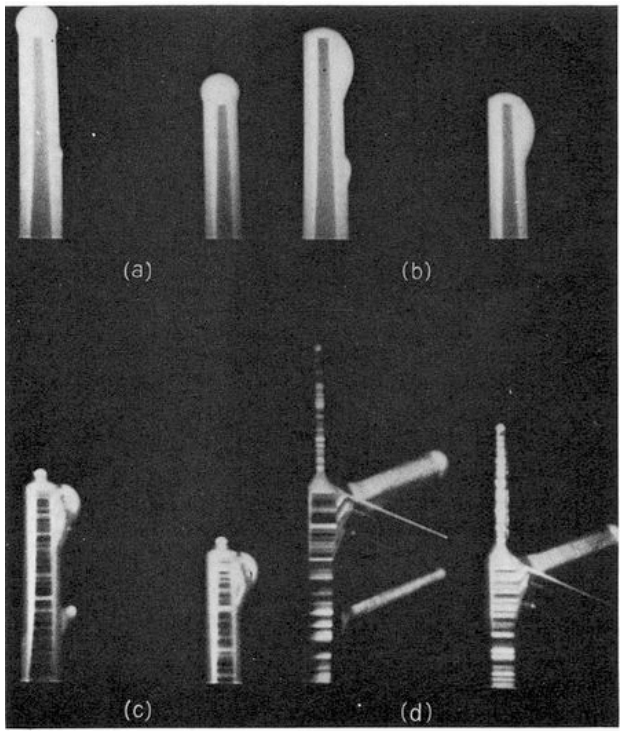


Figure 1-11. Time-lapse sequence of kinking and branching caused by a sudden temperature increase. Magnification approximately 13X. [14]

The majority of the kinked and branched crystals did not contain any observable defects. A few specimens contained islands of Au-Si entrapments which are known to give rise to the generation of defects, as will be shown in the next section. Crystalline defects, such as dislocations, are not considered to be essential for the kinking process [14]. Another significant aspect is that the crystallography of the branch and kink crystals is the same as that of the main crystal, which is different from our observations. In chapter 4, this work will show that kinking of $TiSi_2$ nucleated nanowires is caused by twinning, different from what is observed for micrometer-scale whiskers grown from the liquid.

1.2.1.5 Defects in Silicon Crystals Grown by the VLS mechanism

Inside the grown VLS whiskers, it was shown that the region close to the substrate, i.e., the initial growth region, is imperfect[13]. Crystalline defects can be both generated in this zone or extended into it from an imperfect substrate crystal. Dislocations and stacking faults which terminate at the substrate-liquid alloy interface may continue to grow during the VLS process. Fortunately, the preferred direction of dislocations in silicon are <211> and <110>, and stacking faults are parallel to {111} planes. All these defects are therefore inclined or parallel to the {111} S-L interface. Defects may continue to grow until they eventually terminate at the side faces of the growing crystals. The extension of dislocations from an imperfect substrate is illustrated in Fig. 1-12. The remainder of the crystal, not shown in the photograph, was found to be dislocation-free[13].

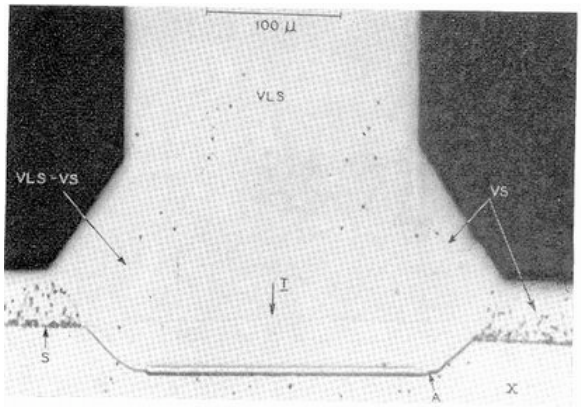


Figure 1-12. Etched section of a VLS crystal grown on an imperfect silicon substrate. (X = substrate; S = original substrate surface; A = alloying interface; I = impurity y striations; VS = directly deposited crystal from vapor-solid reaction; VLS-VS = interface between VLS and VS crystals.) [13]

In this region, entrapment of liquid alloy, possibly caused by S-L interface instability, may happen as shown in Fig. 1-13. An island of liquid surrounded by solid silicon may generate many dislocations. The reason is that if pressure change is not counted, the silicon content of the liquid decreases by about 25 at.% during cooling from 1000°C to the eutectic temperature. There is a considerable change in density and volume associated with the freezing process, which results in a buildup of a hydrostatic pressure in the liquid and huge

stresses in the Si crystal surrounding the alloy island. The resulting stress in the surrounding Si crystal may become large enough for generation and motion of dislocations, as shown in Fig. 1-13. For silicon, which is plastic above 500°C, the generation of defects due to entrapment occurs when a crystal is cooled from the growth temperature to 500°C. On cooling from 500°C, the pressure may generate cracks[13].

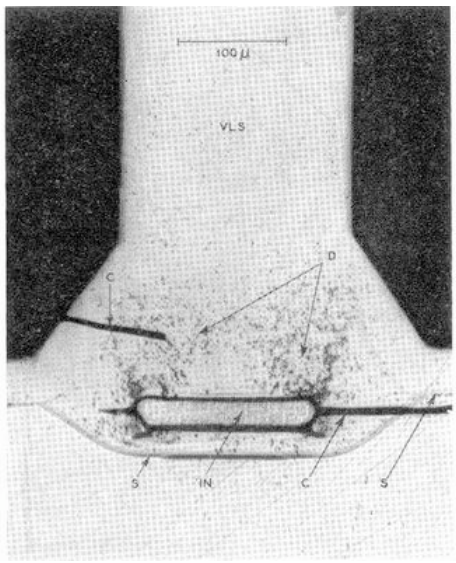


Figure 1-13. Formation of defects due to entrapment of liquid alloy during VLS growth. (In = Au-Si entrapment; C = cracks; D = dislocation pits.) [13]

It was found that in the majority of the grown VLS crystals, the upper growth regions were perfect. But entrapped Au-Si eutectic was also observed, as shown in Fig. 1-14. The islands of eutectic are surrounded by dense networks of dislocation etch pits[13].

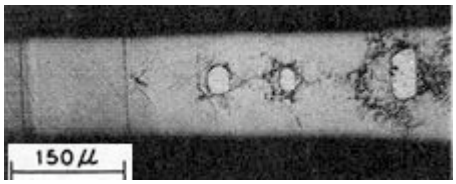


Figure 1-14. Defect formation due to entrapment of liquid alloy. The etched section is parallel to [111] growth direction. [13]

At the region just beneath the alloy droplet, where a short regrowth happens when the temperature is decreased during the termination of the growth, defects may occur, as shown in Fig. 1-15. During fast cooling, the edges of the crystal and of the liquid are colder than

their interiors, which may cause enhanced regrowth at the outer portion of the growth interface and therefore lead to entrapment of the liquid. The stress caused by the entrapment may cause defects and plastic deformation upon further cooling.

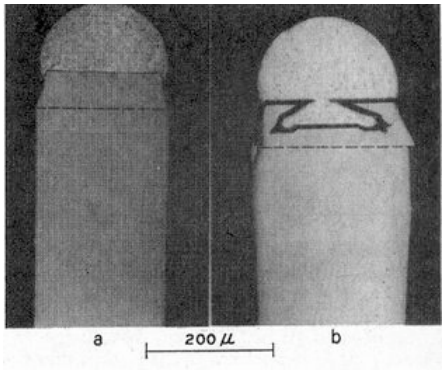


Figure 1-15. (a) Good termination obtained by slow cooling. (b) Defected termination obtained by fast cooling. [13]

Another kind of defect is the entrapment of Au-Si alloy at the branching or kinking position, as shown in Fig. 1-16. The entrapment is due to the sudden temperature increase and the subsequent unstable initial branch growth[14]. For nanowire growth, which has much smaller diameter, entrapment has not been observed, although it is still possible.

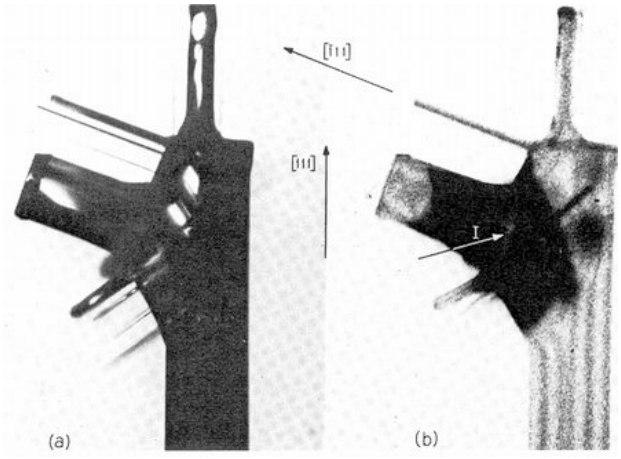


Figure 1-16. (a) Photograph and (b) X-ray topography (showing entrapped Au-Si alloy), of a branched crystal. The alloy tips were removed by etching. [14]

1.2.2 Recent Semiconductor Nanowire Growth Methods

1.2.2.1 Recent VLS Growth

With the VLS method developed by Wagner *et al*., the lower limit of the diameter is generally >100 nm and is limited by the minimum diameter of the liquid metal catalyst that can be achieved under equilibrium conditions at the typical growth temperature of the order of 1000°C[15]. The common characteristic of the recent semiconductor nanowire growth methods is that they can produce a large number of nanoscale-cross-section (diameter <100 nm) wires. A VLS method has been used to grow Si nanowires by confinement of Au on a surface, resulting in InAs and silicon nanowires with diameters of larger than 20 nm and larger than 10 nm respectively[23,24]. In [23], silane, instead of $SiCl_4/H_2$ was used in order to achieve lower growth temperature of between 320°C and 600°C, which is critical for obtaining small liquid Au-Si alloy droplets and minimum sidewall growth of Si nanowires. The growth results are shown in Fig. 1-17.

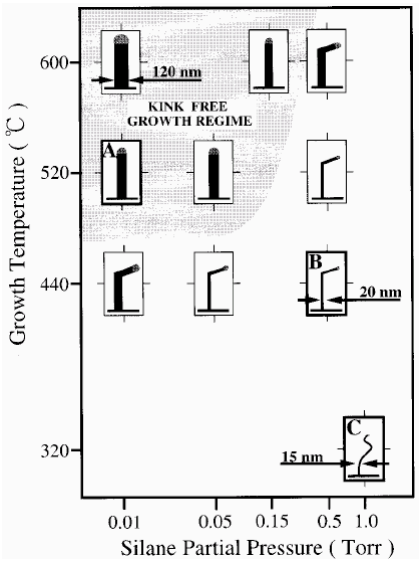


Figure 1-17. Growth modes of Si wires on Si(111) indicating the dependence of wire morphology and width on the growth temperature and pressure. [23]

The wires initially grow along the [111] direction perpendicular to the (111) substrate surface and then switch growth direction spontaneously to one of the other {111} directions by kinking if the silane partial pressure is too high or growth temperature is too low. In the VLS reaction, wire kinking is believed to be associated with instabilities at the liquid/solid interface. As the pressure is increased, the rate of Si incorporation into the molten Au/Si

alloy at the tip of the Si wire also increases because silane decomposition at the vapor/liquid interface is at least one of the rate limiting steps in the wire growth from silane[22]. Also, according to Eq. (1.4), if the silane pressure is increased, μ_{vapor} increases leading to more negative $\Delta\mu_{bulk}$ allowing wire growth to initiate for thinner wires. This effect is clear in Fig. 1-17, similar to what was found by Givargizov[18].

The silicon nanowires grown by silane can be much thinner than those grown by $SiCl_4$. The wires in [23] were grown under nonisothermal conditions (dc current sample heating) at low temperature, whereas the work on wire growth from $SiCl_4$ was done under isothermal conditions at high temperature (hot wall furnace). High temperature is necessary because $\Delta\mu_{bulk}$ for the $SiCl_4$ reduction reaction becomes negative only at high temperatures[25]. Under typical $SiCl_4$ wire growth conditions there is, therefore, little margin thermodynamically to offset the effect of the wire surface energy because $\Delta\mu_{bulk}$ is small. The silane decomposition reaction, on the other hand, is thermodynamically very favorable at all temperatures (down to room temperature), i.e., $\Delta\mu_{bulk}$ is large and negative[25]. The decomposition reaction is limited by the kinetics of the reaction, which are modified by the catalytic activity of the molten alloy surface. The effective chemical potential of Si in silane under similar pressure and temperature conditions is significantly higher than in $SiCl_4$ because the silane molecule is less stable (the bond energies in silane and $SiCl_4$ are 3.9 and 4.8 eV, respectively[26]). Therefore, thinner wires grow more favorably using silane as the Si source gas.

Morales and Lieber[27] reported an approach to the synthesis of single-crystal nanowires that exploits laser ablation to prepare nanometer-diameter catalyst clusters that subsequently define the size of wires produced by a VLS mechanism. This method overcomes the limitation of equilibrium cluster sizes in determining minimum wire diameters. They demonstrated this method with the synthesis of single-crystal Si and Ge nanowires with diameters as small as 6 and 3 nm, respectively, and length > 1000 nm[27].

They used a pulsed, frequency-doubled Nd-YAG laser (wavelength, 532 nm) to ablate targets that contain the element desired in the nanowire and the metal catalyst component. This target was located within a quartz furnace tube, as shown in Fig. 1-18. A transmission

electron microscope (TEM) image of a typical Si nanowire product obtained after laser ablation of a $Si_{0.9}Fe_{0.1}$ target at 1200°C contain primarily wirelike structure with remarkably uniform diameters on the order of 10 nm, as shown in Fig. 1-19 (a). The TEM image shows that virtually all of the nanowires terminate at one end in nanoclusters with diameters 1.5 to 2 times that of the connected nanowire[27]. The difference in diameter is due to the equilibrium of Si chemical potential between the spherical alloy droplet and cylindrical Si nanowire at the growth temperature. High-resolution TEM images on individual nanowires are shown in Fig. 1-19 (b) and (c). The convergent beam electron diffraction (CBED) inset and the lattice image suggests that the nanowire growth occurs along the [111] direction. Electron-induced x-ray fluorescence (EDX) analysis shows that the amorphous coating has an approximate composition of SiO_2[27].

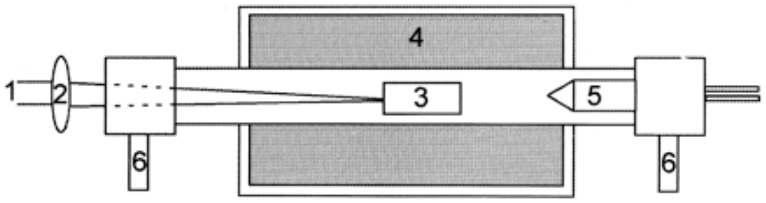


Figure 1-18. Schematic of the nanowire growth apparatus. The output from a pulsed laser (1) is focused (2) onto a target (3) located within a quartz tube; the reaction temperature is controlled by a tube furnace (4). A cold finger (5) is used to collect the product as it is carried in the gas flow that is introduced (6, left) through a flow controller and exits (6, right) into a pumping system. [27]

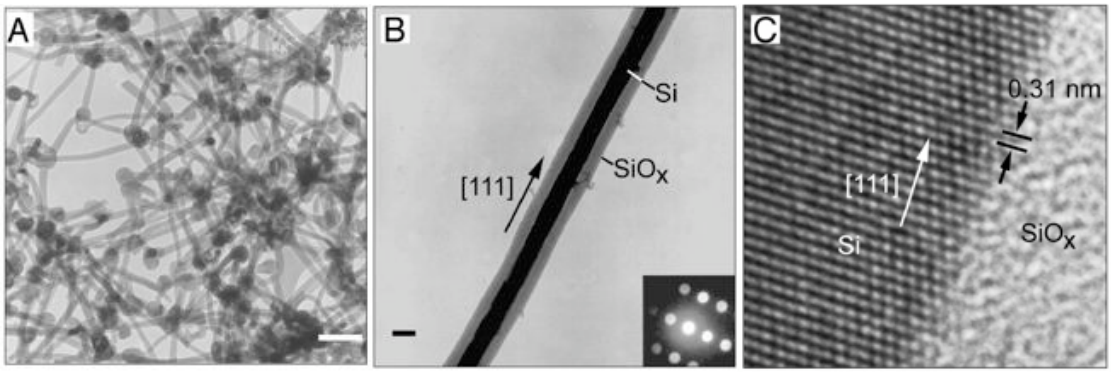


Figure 1-19. (a) A TEM image of the nanowires produced after ablation of $Si_{0.9}Fe_{0.1}$ target. Scale bar, 100 nm. (b) Diffraction contrast TEM image of a Si nanowire; crystalline material (the Si core) appears darker than amorphous material (SiO_x sheath). Scale bar, 10 nm. (Inset) CBED pattern recorded along the [211] zone axis perpendicular to the nanowire growth axis. (c) High-resolution TEM image of the crystalline Si core and amorphous SiO_x sheath. [27]

A VLS mechanism was proposed according to the presence of nanoparticles at one end of nearly all of the nanowires. The growth model is as follows: A supersaturated Si and Fe vapor generated by laser ablation first forms Si-rich liquid nanoparticles, and then the Si phase precipitates as crystalline nanowires due to the driving force of chemical potential difference. The growth stops when the gas flow carries the nanowires out of the hot zone of the furnace. Two observations support this model. First, the terminating solid nanoclusters are □-$FeSi_2$, which is the stable Fe-Si compound in the Si-rich region of the phase diagram. Second, the growth of the Si nanowires occurred only for temperatures greater than 1150°C with the Fe catalyst. The observation of Si nanowire growth at temperatures below the bulk solidus line at 1207°C is reasonable, because the melting points of nanoclusters are lower than the corresponding bulk solids[27].

Wang, Zhang, and their coworkers[28,29,30] also produced Si nanowires by laser ablation, as shown in Fig. 1-20. They used a very similar apparatus to Morales and Lieber[27], with the same chamber temperature (1200°C) the same chamber pressure(500 Torr), and the same gas flow(50 sccm) . The only significant difference is that they used targets containing much less metal catalyst, < 1 wt.% Fe, while in the precious work, 10 at.% Fe was used. As a result, they didn't detect any metal at the tips of the nanowires. Furthermore, they observed that Si nanowires could even be produced by using Si targets containing 5% to 99% SiO_2. Therefore, they concluded that SiO_2 acted as a special catalyst and greatly enhanced the one-dimensional growth of Si nanowires. [28,29,30].

They also found that the axes of the nanowires was generally along the <112> direction, while the Si crystal core near the tip contains a high density of defects, such as stacking faults and microtwins. The stacking faults are generally along the axis of the nanowire in the <112> direction. They pointed out three key factors for their Si nanowire growth. (1) The thick Si oxide shell, which formed during the nanowire growth, retards the sideways or lateral growth of nanowires. This is also likely a key factor for producing nanowires in [27]. (2) The main defects in the Si nanowires are stacking faults and microtwins. These defects at the tip should result in the fast growth of Si nanowires. (3) The appearance of the {111} surfaces, which has the lowest surface energy among all Si surfaces, parallel to the axes of the nanowires tends to reduce the system energy, since

when the crystal size is reduced to nanometer scale, the surface energy becomes increasingly important[28,29,30].

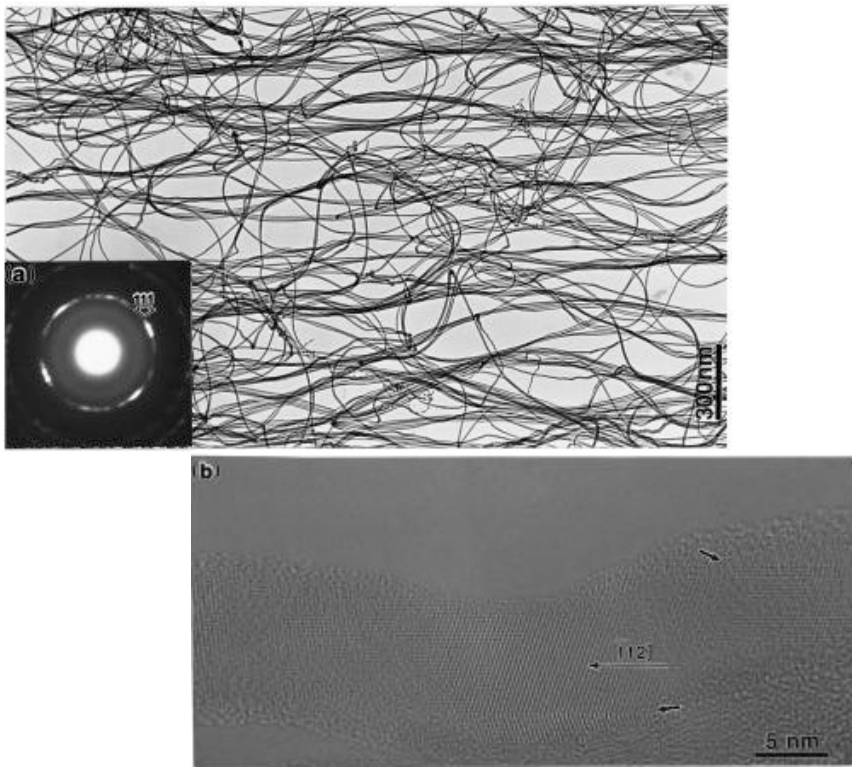


Figure 1-20. (a) TEM image and selected-area electron diffraction (SAED) pattern taken from the nanowires. (b) The microstructure of Si nanowires synthesized from 30% SiO_2 containing target. The arrows mark the stacking fault and twin. [28]

1.2.2.1 Recent Vapor-Solid-Solid (VSS) Growth

Kamins *et al*. [31-34] used Ti as a catalyst to grow Si nanowires by chemical vapor deposition (CVD) with SiH_4 or SiH_2Cl_2. As shown in Fig. 1-21, both long and straight wires and irregular wires are observed. Irregular wires contain twins and/or stacking faults, often correlated with irregularities in the shape of the wire.

In most wires, a nanoparticle is seen at the free end of the wire, with a diameter similar to the wire diameter. A TEM image shows that in the nanoparticle the lattice fringe spacing correspond to the lattice spacing of C49 $TiSi_2$. Energy dispersive x-ray spectroscopy (EDS) also shows that a significant concentration of Ti is in the nanoparticle.

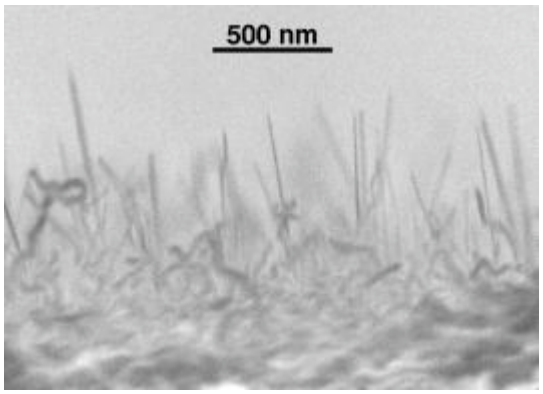


Figure 1-21. Grazing angle scanning electron micrograph of dense wires grown at 670°C on unannealed Ti-containing islands on Si (001) substrate. [32]

The proposed growth mechanism is similar to VLS: the silicon-containing gas decomposes with a higher rate at the $TiSi_2$ island surface. A very thin, Si-rich layer forms on the surface of the $TiSi_2$ island at the growing end of the wire as a result of the catalytic reaction. The excess Si near the surface results in a concentration gradient and this causes the excess Si to diffuse towards the $TiSi_2$-Si interface which acts as a sink of Si atoms. When the Si atoms reach the $TiSi_2$-Si interface, they precipitate on the underlying Si, pushing the $TiSi_2$ island up and forming a wire. It was also estimated that the mass transport of Si-containing gas to the $TiSi_2$ island surface and the transport of Si atoms to the $TiSi_2$-Si interface should be fast enough that the overall formation process is likely to be limited by the reaction of the Si precursor or by the precipitation of Si at the $TiSi_2$-Si interface.

1.3 Semiconductor Nanowire Applications

Si nanowires have been used to fabricate various electronic devices and sensors[35-38]. Yu and Chung *et al*. built 4- and 6- terminal contacts to Si nanowires [39], and put side gates[40], to measure their electric transport behavior. Huang *et al*.[41] even managed to build logic gates, as complex as XOR and half adder, by assembling p-Si and n-GaN nanowires from solution. Sawada *et al*.[42] have used a silicon nanowire array for field electron emission devices. Finally, Lauhon *et al*. produced core-multishell heterostructure nanowires by using both Si and Ge as the building materials, and used them to build a

coaxially-gated nanowire transistor. Due to their superior carrier mobilities or optical properties, compound semiconductor nanowires have been used to build GaN field effect transistors (FETs)[43], InP light-emitting diodes (LEDs)[44,45], ZnO[46] ,GaN[47] and CdS[48] optically pumped lasers, CdS electrically driven lasers[48], and for some other applications[49].

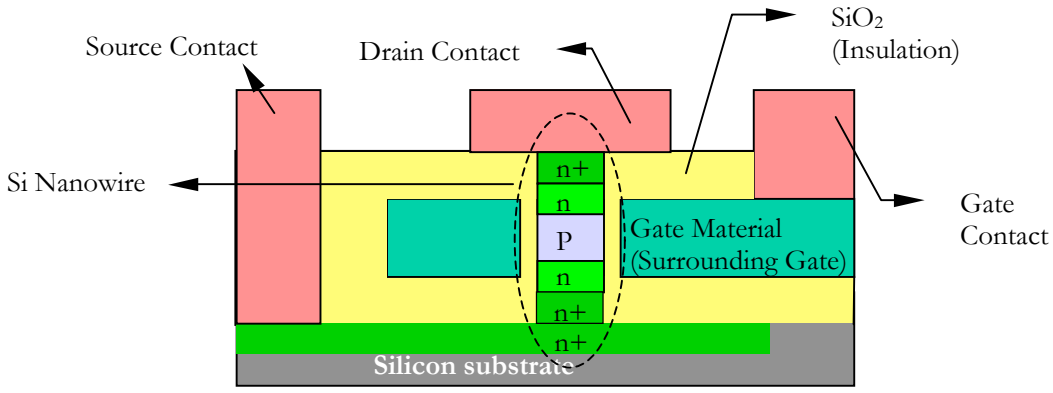


Figure 1-22. Schematic of an in-situ MOSFET device built from a Si nanowire.

A very significant issue is that, to the best of my knowledge, all the published electronic devices built from nanowires, except [40], are not *in situ*. That is, devices are fabricated from nanowires that have been removed from the growth substrate and relocated onto the target wafer. This requires tremendous location accuracy, especially if a compact active device is to be built to fully utilize the small size of nanowires. This process is generally not expected to be manufacturable, as it may be time-consuming, costly, and result in low yield. Therefore, to make practical use of nanowires for building integrated circuits, *in situ* device and *in situ* processing are definitely necessary. The schematic of an in-situ vertical Metal Oxide Semiconductor Field Effect Transistor (MOSFET) built from a Si nanowire is shown in Fig. 1-22. This work will show some results in this direction.

1.4 Why $TiSi_2$-nucleated Si Nanowires?

The most common catalysts used to grow silicon nanowires are Au, Fe, Zn, Ni, Co, and Ti. Although all these transition metals form deep levels in silicon, which are

detrimental to device functionality, the diffusivity and solubility of Ti in silicon are at least two orders of magnitude lower than that of Au, Fe, Zn, Ni, and Co, as shown in Fig. 1-23, where one dominant diffusion mechanism is chosen for each element[50]. Furthermore, Ti has been widely used in integrated-circuit (IC) processing to form low-resistance contacts to silicon and polysilicon, so is more widely utilized and less detrimental in IC processing. Actually, of these metals only Ti and W are allowed in most of the IC processing equipment in the Stanford Nanofabrication Facility where the post-MBE processing of this work was performed. Therefore, the Ti-catalyzed silicon nanowire system is far more compatible with IC components and applications than other approaches and is a prime motivation for this work.

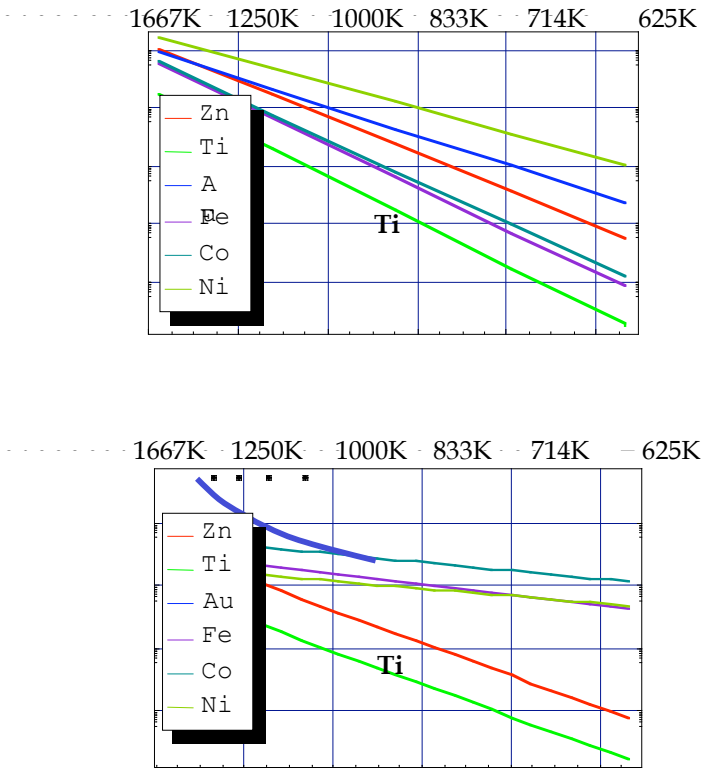


Figure 1-23. Diffusivity and solubility curves of Zn, Ti, Au, Fe, Co, and Ni.

Chapter 2

Equipment for and Process of Ti-Catalyzed Si Nanowire Growth

Almost all researchers working on semiconductor nanowires use CVD or laser ablation as the growth method. We took a different route. In this work, a Varian Gen II molecular beam epitaxy (MBE) system with Si_2H_6 gas source, Si and Ti filament sources, and B and As effusion cells is used. This unique combination of gas and solid sources in our MBE system provide the ability to grow Si nanowires with good growth and doping control[51].

2.1 Molecular Beam Epitaxy (MBE) Introduction

MBE was developed in the early 1970's as a technology to grow high-purity epitaxial layers of compound semiconductors[52,53]. Since then, it has evolved into a popular technique for growing compound semiconductors, Si,[54-57] and Ge, as well as several other materials, such as oxides. MBE can produce high-quality single crystal layers with very abrupt interfaces, monolayer control of thickness, precise doping and compositional accuracy. Because of the high degree of control and flexibility using MBE, it is a valuable tool in the development of sophisticated electronic, magnetic, and photonic devices.

The schematic of a typical MBE system is shown in Fig. 2-1. An MBE system is basically an ultra-high vacuum (UHV) chamber equipped with wafer transfer and rotation mechanisms, a heated sample mount, source cells, which provide molecular flux beams for each needed component, *in situ* monitoring tools, which are used to monitor the initial surface cleaning and successive growth, and pumps, which provide and keep the UHV

necessary for growing high quality materials. Source cells can be effusion cells, which generate component molecular fluxes by evaporating or sublimating high purity source materials, or gas cells, which generate component hydride or plasma fluxes controlled by a mass flow controller (MFC). The hydrides decompose at the substrate surface and incorporate into grown materials without extra hydrogen atoms. Growth from hydrides is quite different from growth from elemental effusion cells because with hydrides, the substrate surface will be covered by hydrogen and this makes surface reaction kinetics different from the cases without surface-H coverage. In hydride gas source growth, source hydrogen desorption is normally the rate limiting step, as is believed in Si growth from disilane (Si_2H_6). The *in situ* monitoring tools include reflection high-energy electron diffraction (RHEED), which provides information about substrate surface configuration and flatness; pyrometry, which provides *in situ* growth temperature calibration; and residual gas analyzer (RGA), which provides information about chamber vapor composition for chamber leakage detection and/or even growth monitoring. In our case, the titanium flux can only be monitored by RGA because it is very small and ion gauge can not isolate it from other background fluxes, such as H, Si, and As. More complex MBE systems probably also contain Auger electron spectroscopy (AES), electron energy-loss spectrometry (EELS), and low-energy electron diffraction (LEED), which provide composition and chemical status analysis, localized vibrational modes of adsorbed molecules as well as surface phonon analysis, and two-dimensional surface configuration analysis, respectively. The pumps include ion pumps, cyro-pumps, turbo pumps, and a liquid nitrogen cyro-shroud, which is maintained below nitrogen boiling point (77.36 K) and surround the hot source furnaces and inner growth space to decrease chamber outgassing.

The base pressure of an MBE system in stand-by mode is normally 10^{-11} to 10^{-9} Torr. This UHV condition is necessary for the source fluxes to stay in the molecular flow regime and for the substrate surface to stay clean. In a molecular flow, molecules do not collide or react with each other on their way to the substrate and the molecules that miss or desorb from the substrate will be pumped away without coming back. This condition is achieved if the molecules' mean free path in the flow is much larger than the distance they need to

travel. Under UHV pressure, the mean free path for evaporated molecules is on the order of tens of meters, much larger than the typical dimension of a vacuum chamber. With source fluxes in the molecular regime, the growth of one source material can be stopped with minimum memory effect if a clean shutter blocks the line-of-sight between the source cell and the substrate. And because of very low background flux striking the substrate surface, the substrate can keep a clean surface for hours, while in the atmospheric environment it will be covered by a monolayer of adsorbed gas within one microsecond.

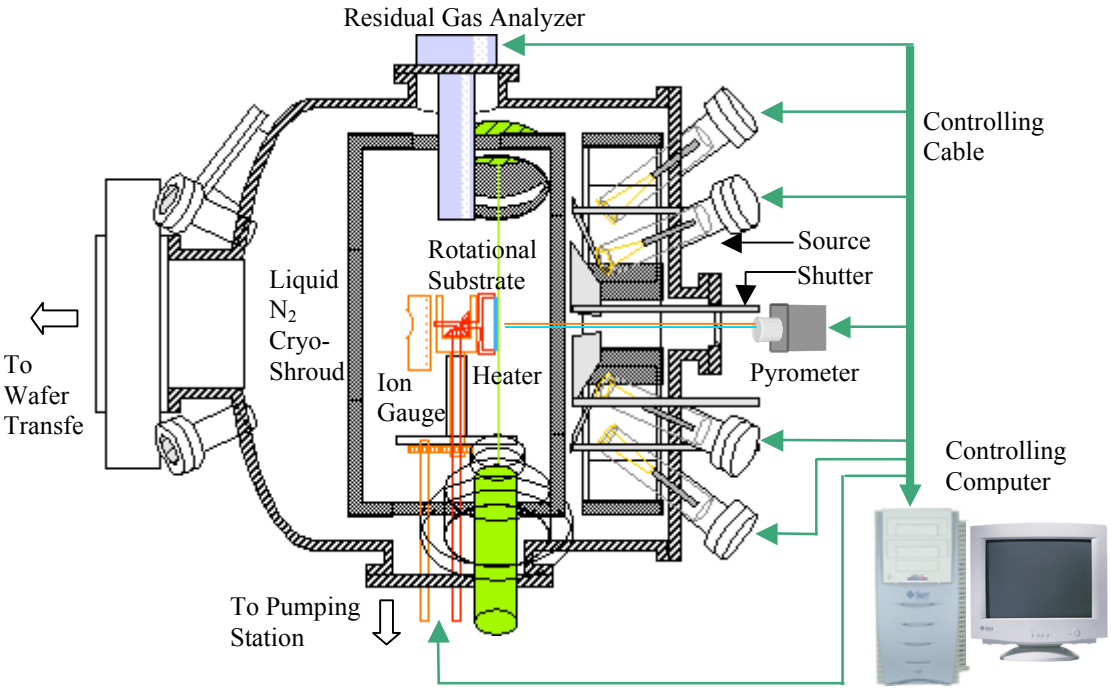


Figure 2-1. Schematic diagram of a MBE system.

Because of the UHV, MBE growth is carried out under conditions far from thermodynamic equilibrium and is governed mainly by the kinetics of reaction between the impinging molecules and the topmost atomic layers of the substrate crystal. In typical MBE growth, a series of surface processes are involved, as shown in Fig. 2-2. First, the molecules impinging on the substrate surface are adsorbed through chemisorption for group III atoms and Si_2H_6, or physisorption for As_2 and As_4[58]. For Si_2H_6 growth, this step is a second-order dissociative chemisorption as follows[59-61]:

$$Si_2H_6 + 2db \rightarrow 2SiH_3 \qquad (2.1)$$

where db stands for "dangling bonds". Then the absorbed atoms or molecules migrate and dissociate on the surface, with surface diffusivity determined by substrate temperature and surface conditions. For Si_2H_6 growth, this step involves two surface decomposition reactions as follows:

$$SiH_3 + db \rightarrow SiH_2 + H \quad (2.2$$

$$2SiH_2 \rightarrow (SiH)_2 + H_2\uparrow \quad (2.3$$

Then when the atoms or molecules find a low energy site, normally at ledges or kinks for layer-by-layer growth, they may incorporate into the substrate lattice. For Si_2H_6 growth, the remaining hydrogen is lost in this step in a first-order reaction, due to π-bond-induced pairing of dangling bonds on single Si dimers. This is normally the rate-limiting step, represented as follows:

$$(SiH)_2 \rightarrow Si_2 + H_2\uparrow \quad (2.4)$$

The species not incorporated in the substrate lattice will re-evaporate due to thermal desorption.

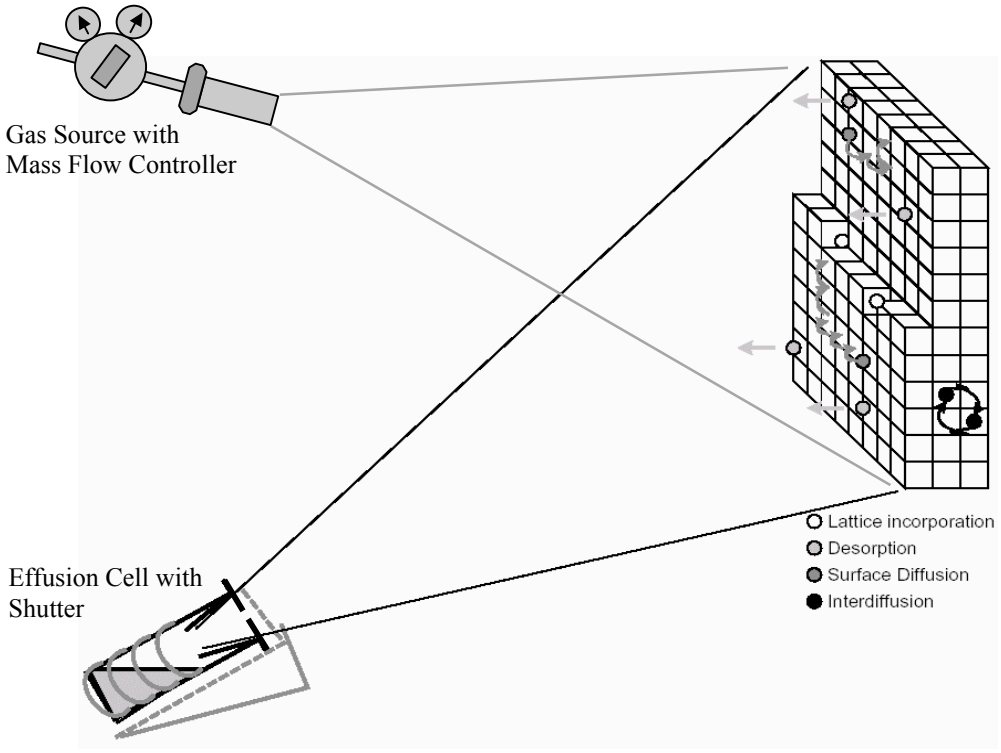


Figure 2-2. Schematic illustration of the surface processes involved in a MBE growth.

2.2 Our Si Nanowire Growth Process

2.2.1 Wafer Wet Cleaning

Before being transferred to the MBE growth chamber, the wafer needs to be baked in the load chamber, which is pumped by an ion pump and a cryo-pump at 200°C for one hour in order to remove most of the H_2O on the wafer and the holder. Prior to introducing the wafer into the load chamber, the wafer needs to go through a wet-bench clean procedure. After many iterations, the following modified RCA-clean [51] procedure works best for obtaining a clean Si substrate surface for epitaxy growth.

Step 1: 4:1 (98% H_2SO_4) : (30% H_2O_2) at 90°C for 10 min. Then dump rinse for 6 cycles.

Step 2: 5:1:1 H_2O : (30% H_2O_2) : HCl at 70°C for 10 min. Then dump rinse for 6 cycles.

Step 3: 50:1 H_2O : HF at room temperature for 15-30 s. Then dump rinse for 6 cycles.

Step 4: 5:1:1 H_2O : (30% H_2O_2) : HCl at 70°C for 10 min. Then dump rinse for 6 cycles.

Step 1 decomposes the organic contaminants and oxidizes group IB and IIB and some other metals. Step 2 completes the removal of metallic contaminants such as Au, Fe^{+3}, and Al^{+3} that may not have been completely removed by step 1. Step 3 removes the thin oxide layer formed during the first two steps and any contaminants attached. This step will leave the Si wafer surface H-terminated. Step 4 is the same as step 2. We used this extra step to form a clean thin layer of oxide to cover the wafer surface because we found when moving the cleaned wafers to the MBE machine, surface carbon contamination is very hard to avoid. If we leave the Si wafer surface H-terminated, surface C contamination will not be removed even if we bake the wafer at 850°C in vacuum[63]. While with oxide covered surface, the C contamination will come off together with evaporated oxide at above 800°C. An atomic Force Microscope (AFM) image of the surface of the cleaned wafer is shown in Fig. 2-3. The measured roughness for this 100 nm × 100 nm area is 0.107 nm, which is very good considering that the Si lattice constant is even 0.543nm.

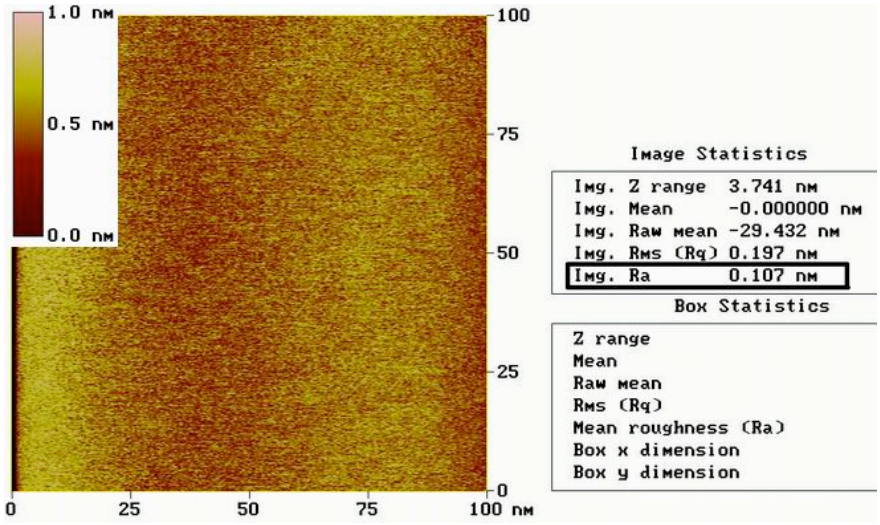


Figure 2-3. AFM image of the cleaned Si wafer surface.

2.2.2 Wafer In-Situ Cleaning

After wet cleaning and baking in the load chamber, the wafer is transfered into the growth chamber shown in Fig. 2-1. Then the wafer is heated to 850°C to desorb the surface oxide. This step is observed in-situ with a VG Scientific LEG110 RHEED system. The RHEED electron beam has an energy of 14 keV (□=0.01nm) and an incidence angle of ~1°. The base pressure of the MBE system is 4□10^{-11} torr.

The RHEED pattern of the (001) substrate surface taken at about 300°C before desorbing the surface oxide is shown in Fig. 2-4 (a). We can see the zero-order Laue diffraction (L0) stripes without surface reconstruction[64,65]. Seeing stripes shows that the silicon surface is flat while seeing silicon a diffraction pattern shows that the top oxide layer covering the Si substrate is very thin because with the low incidence angle, the penetration depth of the RHEED electron beam is less than 2 nm. We see a reasonably bright Si diffraction pattern, which means that the oxide thickness is much less than 2 nm. Fig. 2-4 (b) shows the RHEED pattern after the Si substrate is heated at 700°C for 10 min, from which we see not only the regular Si pattern, but also the silicon (2□1) surface reconstruction stripes (-1/2, 0), (1/2, 0), etc. which are in the middle between the regular Si stripes. The reconstruction stripes (-1/2, 0) and (1/2, 0) are less bright than the regular stripes (-1, 0) and (1, 0). Previous theory and experiments showed

that if the (001) silicon surface is clean, the surface atoms should form a (2□1) reconstruction. Therefore Fig. 2-4 (b) shows that the surface oxide has started to desorb and part of the surface is clean and reconstructured. Fig. 2-4 (c) shows the RHEED pattern after the substrate is heated at 850°C for 10 min. The pattern is less bright because the RHEED beam was less bright at that moment. What should be noted is that the reconstruction stripes (-1/2, 0) and (1/2, 0) have about the same brightness as the regular stripes (-1, 0) and (1, 0). This means that the entire substrate surface is clean and reconstructed. Fig. 2-4 (d) shows the RHEED pattern after growth at 811°C with Si_2H_6 for 10 min, which is not part of the in-situ cleaning. It shows a generally better surface diffraction pattern, which means better surface cleanness and crystalline state. For Fig. 2-4, the electron-beam incidence direction is substrate [-110]. All four images show Kikuchi lines, which means that the top few atomic layers have good crystal quality.

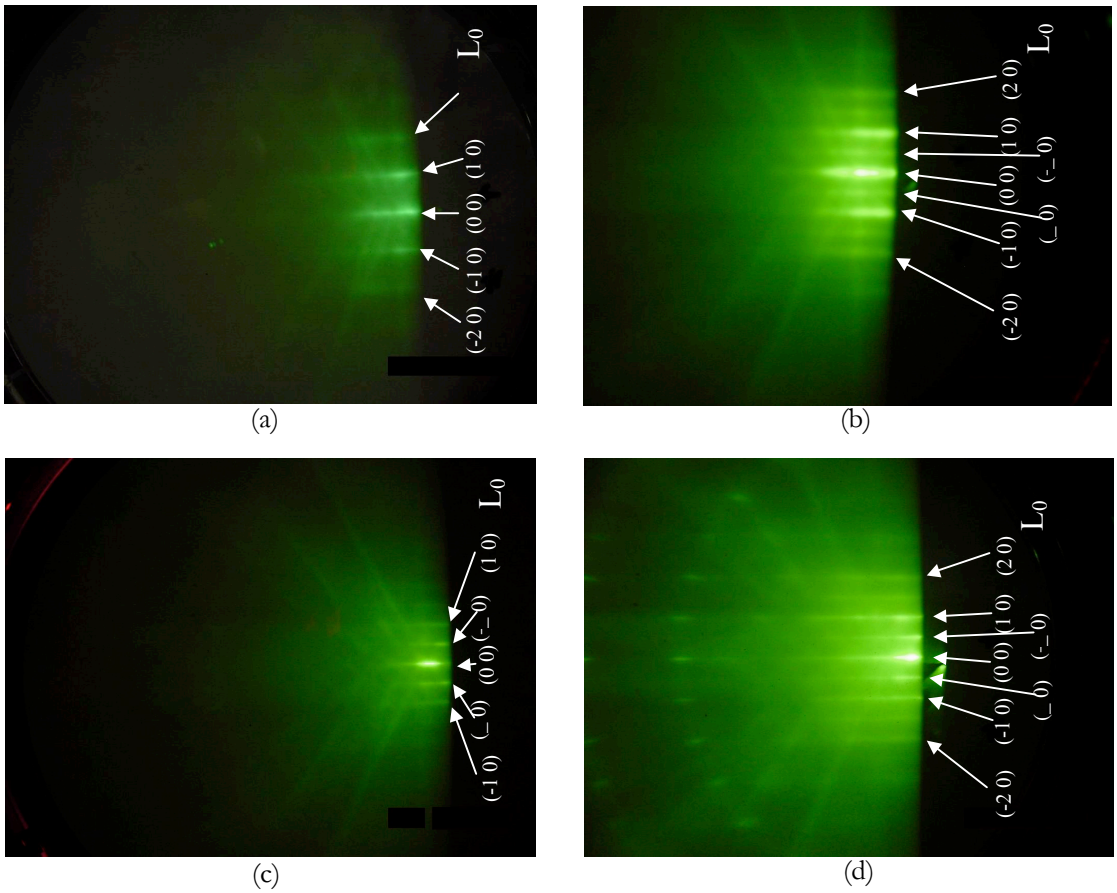
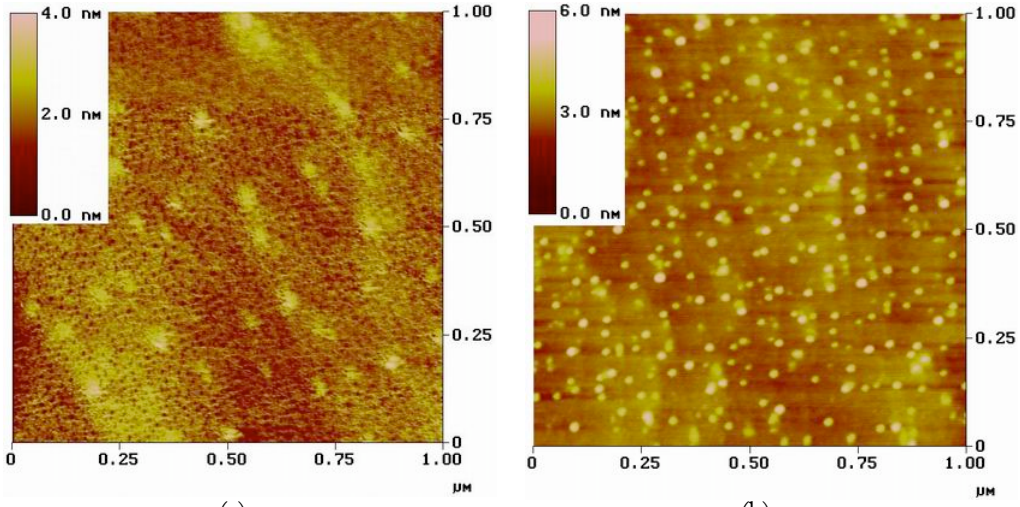


Figure 2-4. RHEED images of the Si substrate surface. (a) At 300°C. (b) After heating at 700°C for 10 min. (c) After heating at 850°C for 10 min. (d) after growth at 811°C with Si_2H_6 for 10 min.

2.2.3 Titanium Deposition and Annealing

After the Si substrate is in-situ cleaned by desorbing the surface oxide, of the order of one monolayer of Ti is deposited at 538°C by a current-heated Ti filament source. Then the substrate is annealed at higher temperature to form titanium silicide islands. Fig. 2-5 (a) shows the AFM image after Ti is deposited at 538°C, without further annealing, where only relatively low and not clearly identified islands with sizes between 20 nm and 100 nm are found. The silicon surface is rough and a little textured, probably due to the deposition of Ti atoms. As shown in Fig. 2-5 (b), after further annealing at 772°C for 10 min, the islands become smaller (sizes between 10 nm and 40 nm) and the area density increased about 10 times. Some islands are much taller (note the larger vertical scale). Fig. 2-5 (b) also shows the surface atomic terraces and that the silicide islands tend to nucleate at the edge of the terraces. This is reasonable because atoms tend to diffuse quickly on terraces but when they reach the ledge side of the terraces with ad-atoms, they tend to find lower energy sites and nucleate there. When atoms reach the cliff side of the terraces, they do not diffuse down to the lower terrace because of the higher energy barrier for diffusing over the edge, therefore they can also accumulate and nucleate near the cliff edge.[66,67,68]



(a) (b)

Figure 2-5. AFM images of (001) Si substrate surface (a) after Ti deposition at 538°C and (b) after further annealing at 772°C for 10 min.

The deposition and nucleation of Ti is similar to the metal catalyst deposition and nucleation in VLS growth. But according to the phase equilibrium diagram shown in Fig. 2-6, titanium should remain in the solid state for our annealing temperature of 811°C ~ 928°C and growth temperature of 520°C ~ 655°C, even if the Gibbs-Thompson effect is considered[69] because the lowest eutectic point between titanium silicides and Si is 1330°C, much higher than our annealing and growth temperatures. This is the main factor which causes our grown nanowires to have more kinking and twinning.

2.2.4 Nanowire Growth with Si_2H_6

After Ti deposition and annealing, the substrate temperature is decreased to between 538°C and 616°C for nanowire growth. Then Si_2H_6 is introduced into the growth chamber, with a mass flow controller to control its flow. The Si_2H_6 flow is normally between 2.5 and 25 standard cubic centimeters per minute (sccm). If the growth temperature is low (538°C), the normal non-catalyzed Si epitaxial growth rate is low, about 0.35 nm/min[59]. Then the cross-section dimensions of the grown Si nanowire are comparable to the island sizes after annealing. The lengths of the nanowires are very nonuniform and depend on the growth temperature and Si_2H_6 flux. Fig. 2-6 shows growth on (001) Si substrate at 538°C for 60 min with the Si_2H_6 flow rate of 2.5 sccm. The detailed growth behavior will be discussed in the next chapter.

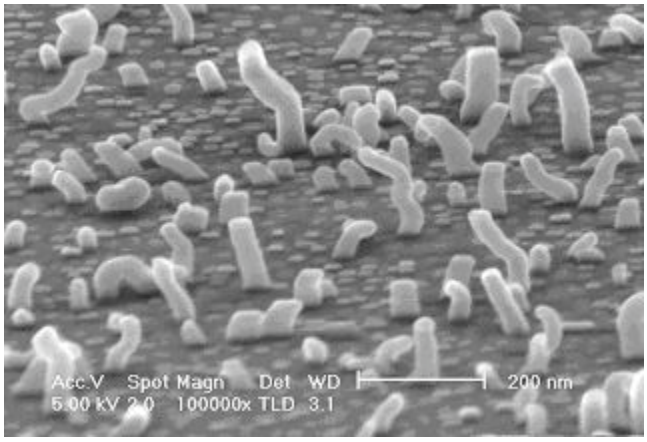


Figure 2-6. SEM images of a growth on (001) Si substrate at 538°C for 60 min with the Si_2H_6 flow rate of 2.5 sccm.

Chapter 3

Growth Behavior and Twinning

The growth behavior of Si nanowires is very important to obtain desired nanowires for nano-device or other applications. The growth behavior is complex, mainly due to the fact that the titanium silicide islands are always in the solid state. I will show some discussion about it in this chapter. Twinning is common to crystal growth, but probably never as omnipresent as in Ti-catalyzed Si nanowire growth, which will be discussed in detail in this chapter.

3.1 Ti-Catalyzed Si Nanowire Growth Behavior

3.1.1 Influence of Growth Temperature

Proper temperature is critical to Ti-catalyzed Si nanowire growth. The images of growths at 500°C, 538°C, and 655°C are shown in Fig. 3-1. At 500°C, normal Si epitaxial growth is in the surface reaction limited regime and $TiSi_2$ island catalyzed growth is in a surface reaction or interface condensation rate limited regime. Interface condensation rate means how fast the Si atom coming from $TiSi_2$ island surface can incorporate into the Si nanowire crystal. Both mechanisms have very low growth rate. Therefore, Si nanowires didn't grow. At 538°C, normal epitaxial growth is still surface reaction limited, while $TiSi_2$ island catalyzed growth is also surface reaction or interface condensation rate limited or close to be supply limited growth, which has a much higher growth rate. As a result, the nanowires grow up. At 655°C, both growths are supply limited, so they have similar growth rates. As a result, the nanowire diameters grow larger because of sidewall epitaxial

growth. But they do not grow up because they are buried by growth of the normal epitaxial silicon layer.

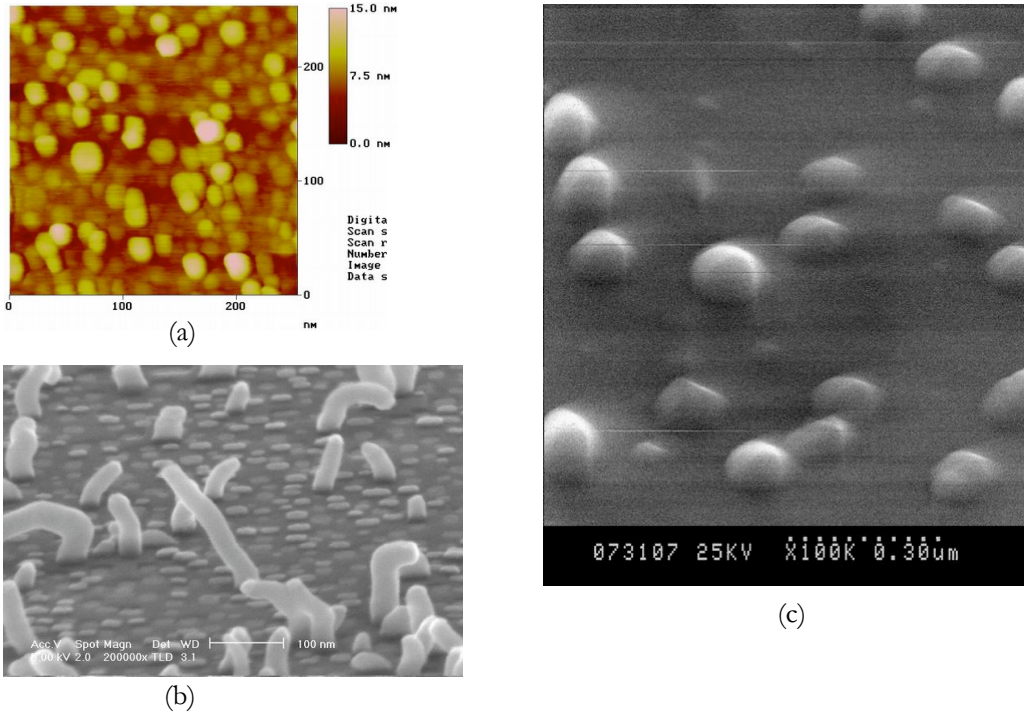


Figure 3-1. (a) AFM image of growth at 500°C with Si_2H_6 flow rate of 2.5 sccm. (b,c) SEM images of growths at 538°C and 674°C, with Si_2H_6 flow rates of 2.5 sccm and 12.5 sccm, respectively.

For Si epitaxial growth with Si_2H_6, the activation energy is 2.52 eV[59]. The activation energy for titanium silicide catalyzed growth should be smaller. Therefore, a schematic of their relative growth rate can be drawn as Fig. 3-2.

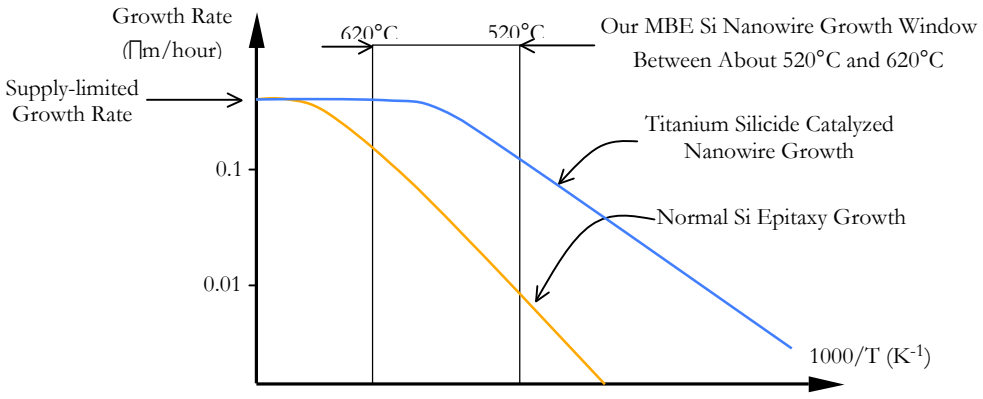


Figure 3-2. Schematic of relative growth rates of normal Si epitaxy growth and titanium silicide catalyzed nanowire growth.

3.1.2 Influence of Titanium Silicide Island Sizes

VSS growth of Si nanowires with titanium silicide as the catalyzing islands is similar to VLS growth in many aspects. One of these is the observation that smaller diameter nanowires grow slower than larger diameter nanowires, which is explained by Givargizov by correlation between supersaturation and growth rate[18]. In our VSS growth case, since the catalyzing islands are in the solid state, their crystalline qualities, orientation and interfaces with the Si crystal are not as uniform as the liquid catalysts in the VLS cases. These will influence the rate limiting steps, such as the island surface decomposition, the Si atom transportation, or the condensation at the interface, therefore making the growth rate nonuniform. Despite these complexities, we still observe a dependence of growth rate on nanowire diameter. One of these observations is shown in Fig. 3-3.

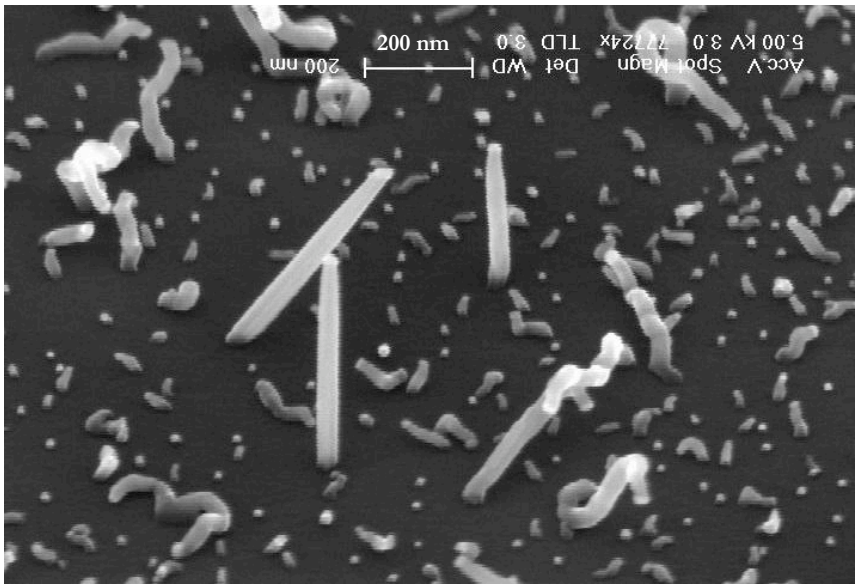
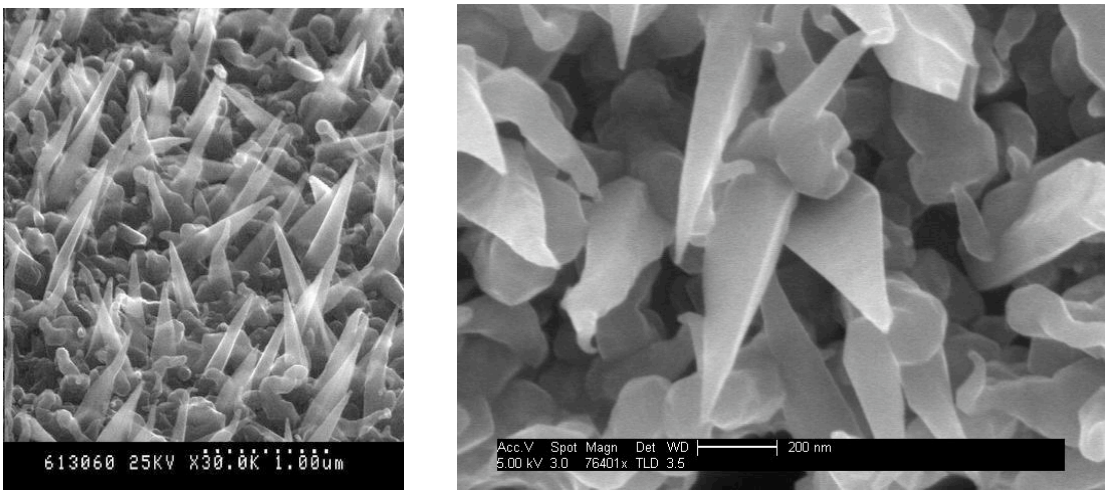


Figure 3-3. A SEM image showing growth rate dependence on nanowire diameter sizes. Larger diameter nanowires grow faster. The growth temperature is 577°C.

The above observation is only valid for growths with temperatures around 577°C, where the critical diameter is about 10nm. $\Delta G = \Delta H - T\,\Delta S$, so at higher growth temperature, $\Delta\Delta_{bulk}$ in Eq. (1.4) is more negative. Therefore, the nanowire diameter, d, can be smaller, while still thermodynamically feasible to grow, at higher growth temperature. In this case, the very small islands tend to nucleate longer and straighter nanowires than big islands do, as shown in Fig. 3-4 (a) and (b). From Fig. 3-4 (a) we can see that the long

straight cone-shaped nanowires are all nucleated from small islands at their tips, while the nanowires nucleated from larger islands are kinked and generally shorter. The cone shape comes from the visible sidewall Si epitaxial growth at this temperature, with the lower part of the nanowire wider because it is exposed to sidewall growth longer. Fig. 3-4 (b) shows that the tip island sizes of the long cone-shaped nanowires are mostly less than 10 nm, close to the resolution of the SEM.



(a) (b)

Figure 3-4. SEM images of a growth on (112) substrate at 655°C for 10 min with Si_2H_6 flow rate of 12.5 sccm, (a) taken at an angle of about 43° from plain view and (b) taken at an angle close to plain view.

Fig. 3-5 shows a growth with similar conditions except a lower growth temperature of 577°C, where only the islands larger than 20 nm nucleate nanowires. I think that the difference of the growth behavior of small islands comes from the change in growth mechanism. Compared with larger islands, smaller islands have less stress because of easier relaxation at positions away from the interface. For islands smaller than 10 nm, surface diffusion may also contribute to maintain the high interface supersaturation for high growth rate. If interface Si condensation is the rate-limiting step, which could be true at higher temperature and with high Si_2H_6 pressure, then these improvements should lead to higher growth rate. The possibility that the smaller islands have a different surface, which offer a higher catalyzing rate compared with larger islands, can not be excluded, but seems less likely.

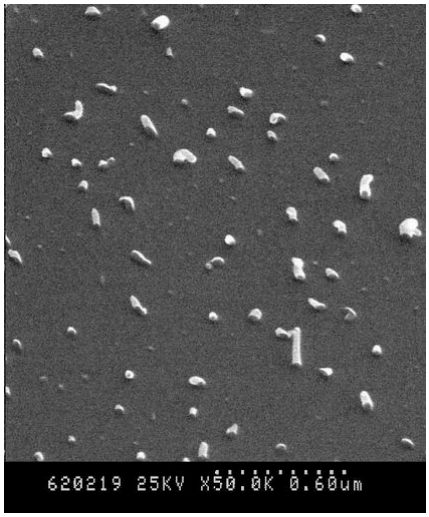


Figure 3-5. SEM images of a growth on (112) substrate at 577°C for 10 min with Si_2H_6 flow rate of 12.5 sccm, taken at an angle of about 43° from plain view.

3.1.3 Influence of Titanium Deposition Temperature

Since the formation of titanium silicide is influenced by temperature[70,71], the nanowire growth behavior is influenced by the titanium silicide formation temperature. Fig. 3-6 shows the SEM images of growths on Si (001) substrates after the same amount of Ti is deposited at different temperatures. An SRS 2000 RGA, which has the manufacture default calibration, is used to monitor the Ti flux in situ. The normal Ti deposition is done with the Ti partial pressure of 1.0_10^{-11} Torr. In Fig. 3-6 (a), the Ti is deposited at 694°C and annealed at 850°C for 10 min, then the nanowire growth is done at 538°C with 1.25 sccm Si_2H_6 for 3 hours. In Fig. 3-6 (b), the Ti is deposited at 850°C and annealed at 850°C for 2 min, then the nanowire growth is done at 561°C with 5 sccm Si_2H_6 for 1 hour. In Fig. 3-6 (c), the Ti is deposited at 928°C and annealed at 928°C for 2 min, then the nanowire growth is done at 538°C with 5 sccm Si_2H_6 for 1 hour. The growth difference caused by the different growth temperatures of 538°C and 561°C is not significant. Comparing the three images, we can easily see that as the Ti deposition temperature increases, the island density decreases and the island sizes increase. Although the sample in Fig. 3-6 (a) is also annealed at 850°C, even longer than the sample in Fig. 3-6 (b), it seems that the Ti deposition temperature is a more important determinant on the islands and ensuing growth. This

means that the nucleation of stable titanium silicide islands is mainly determined when Ti is deposited. The annealing at 850°C is not kinetically long enough to change it.

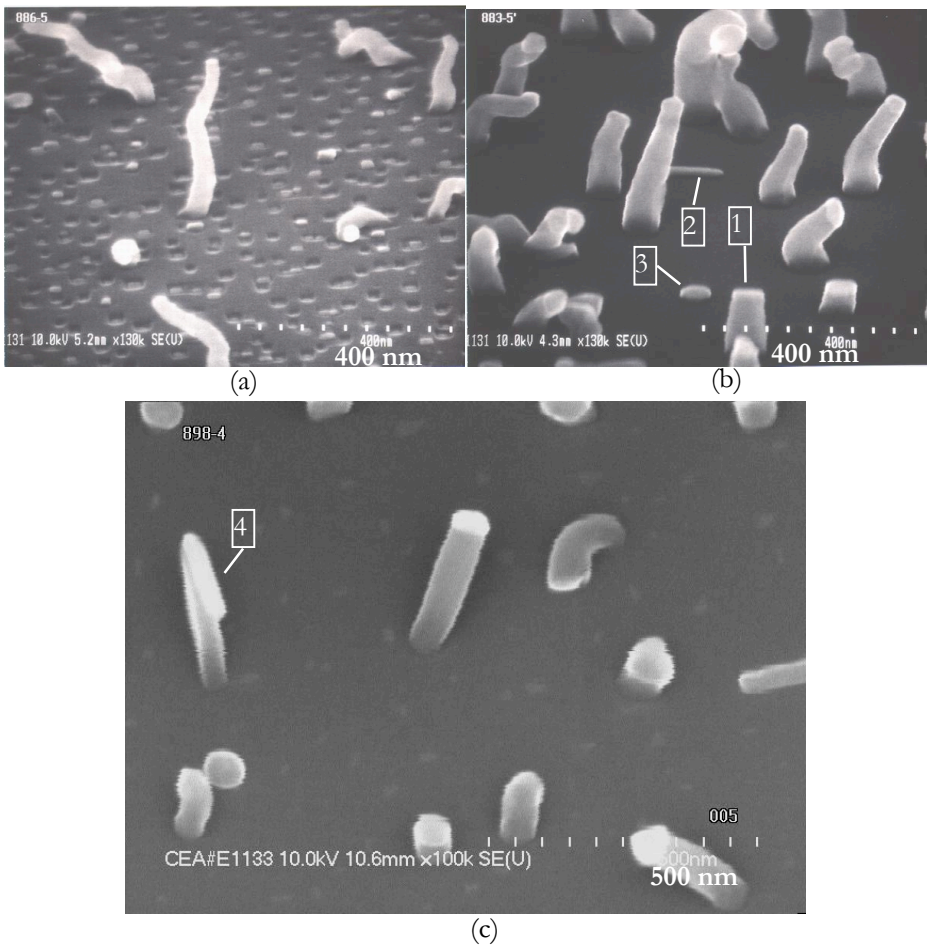


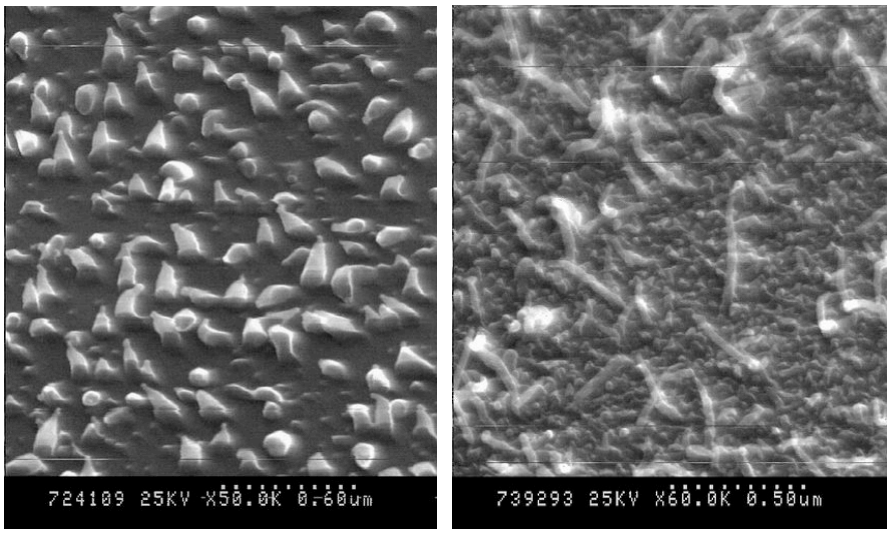
Figure 3-6. (a) The Ti is deposited at 694°C and annealed at 850°C for 10 min, then the nanowire growth is done at 538°C with 1.25 sccm Si_2H_6 for 3 hours. (b) The Ti is deposited at 850°C and annealed at 850°C for 2 min, then the nanowire growth is done at 561°C with 5 sccm Si_2H_6 for 1 hour. (c) The Ti is deposited at 928°C and annealed at 928°C for 2 min, then the nanowire growth is done at 538°C with 5 sccm Si_2H_6 for 1 hour.

Another big difference is that in Fig. 3-6 (a), only a very small portion of the islands nucleate nanowires, while in Fig. 3-6 (b) and (c), a majority of the islands do so. A closer observation of Fig. 3-6 (a) sample shows that over 90% percent of the nanowires have dome-shaped tall islands at their tips and over 90% percent of the non-nucleating islands have a flat topped surface, in agreement with the observation by Kamins *et al*.[32]. (See the island surface profiles in Chapter 4.) But in Fig. 3-6 (b), a nanowire nucleated by a flat-topped island (denoted by "1") is clearly seen. Moreover, a non-nucleating equaxial flat-

topped island (denoted by "2") and an non-nucleating flat-topped island elongated along one of the <110> directions (denoted by "3") are also seen. In Fig. 3-6 (c), an elongated flat-topped island even grew up (denoted by "4"), resulting in a nano-slab. Why is such a difference? As will be shown in Chapter 4, in the case of Fig. 3-6 (a), the majority of the islands (flat-topped) are C49 $TiSi_2$ with an orientation of Si[110]//C49-$TiSi_2$[100] (about 5.7% lattice mismatch), Si[$\bar{1}$10]//C49-$TiSi_2$[001] (about 6.3% lattice mismatch), and Si(001)//C49-$TiSi_2$(010), or the orientation of Si[110]//C49-$TiSi_2$[001], Si[$\bar{1}$10]//C49-$TiSi_2$[100], and Si(001)//C49-$TiSi_2$(010). C49-$TiSi_2$ has a orthorhombic structure with a=0.362 nm, b=1.376 nm and c=0.360 nm. The mismatch between Si<110> (0.384 nm) and C49-$TiSi_2$[100] is smaller than that between Si<110> and C49-$TiSi_2$[001]. Therefore, at high temperature, the $TiSi_2$ islands will tend to elongate along C49-$TiSi_2$[100] direction[72,73], as shown in Fig. 3-6 (b) and (c), possibly together with orientation change in the perpendicular C49-$TiSi_2$[001] direction. Higher deposition temperatures also allow other $TiSi_2$ islands to nucleate with many other orientations, with no dominating orientations, as revealed by RHEED observation. But these orientations do tend to nucleate nanowires. The other possible reason for better nucleation might come from better $TiSi_2$-Si interfaces resulting from higher deposition temperatures because annealing at high temperature might not be kinetically long enough to anneal out the defects. These might explain why the elongated flat-topped islands nucleate nanowires in Fig. 3-6 (c).

3.1.4 Influence of Chamber Outgas

Normally at growth temperature higher than 616°C, the nanowire sidewall growth is clearly visible and the grown nanowires are cone-shaped, as shown in Fig. 3-7 (a). Fig. 3-7 (b) shows a similar growth, but with the MBE growth chamber cryo-shroud warming up during the growth. Fig. 3-7 (b) shows nanowires with much less sidewall growth compared with Fig. 3-7 (a). I think As, H_2O, and other contaminants out-gassing from the cryo-shroud are responsible for the reduced sidewall growth because they can cause the sidewall covered with O or As, blocking sidewall Si epitaxy growth. Actually, I think this is also the reason that little sidewall growth occurs at high growth temperature in some laser ablation or CVD growth, where the oxygen from chamber leakage might be blocking nanowire sidewall growth.



(a) (b)

Figure 3-7. SEM images of growths at 750°C for 10 min with a Si_2H_6 flow of 20 sccm (a) with cryo-shroud cold and (b) with cryo-shroud warming up. The viewing angle is about 45° for both images.

To testify this hypothesis, a sample is grown at 655°C with a Si_2H_6 flow of 12.5 sccm and an As flux of 1.1 E-8 Torr, which is shown in Fig. 3-8. Compare Fig. 3-8 with Fig. 3-1 (c), it is obvious that the sidewall growth is suppressed by the As flux, although not stopped as the nanowires in Fig. 3-8 are still cone-shaped. This is similar to the observation in planar Si epitaxy.

Figure 3-8. SEM image of a growth at 655°C with a Si_2H_6 flow of 12.5 sccm and an As flux of 1.1 E-8 Torr.

3.1.5 Nanowire Growth Direction and Sidewalls

Nanowire growth direction is an important parameter for most applications. For example, to make vertical MOSFETs using nanowires, we prefer nanowires to be perpendicular to the wafer surface to make the subsequent processing easier and better controlled, such as minimizing shadowing effects for lithography and metal and insulator deposition. Typical Si nanowires grown by the VLS method have <111> growth directions, but the ribbons shown by Wagner *et al*.[16] are possibly nanowires that first grown in a <112> direction, then become ribbon-shaped during sidewall growth because for Si, (111) planes grow slower than other crystal planes. Moreover, oxide-assisted Si nanowire growth is found to be mainly in <112> directions[28]. Tan *et al*.[74] explained the preferred growth directions of <112> and <110> by counting most heavily on the Si surface stability and surface lateral growth, which I think is not suitable for VLS and VSS growth. As shown by Wagner[14], for Si VLS growth using gold as a catalyst, the interface between the liquid droplet and Si underneath it is (111) and the interface is normally stable. Therefore, the condensation of Si atoms on the (111) interface causes the Si nanowire to grow in the <111> direction. For VSS growth, the catalyst islands are in the solid state, thus the interface is hardly just one nearly-perfect plane because the lattice-mismatch between the silicide island and Si normally causes the interface to be faceted and/or defected and the supersaturation of Si atoms across the interface is quite non-uniform. Therefore, we rarely observed a single interface plane between titanium silicide and Si. However, I think the growth direction of VSS growth is kinetically determined by the Si atom condensation at the $TiSi_2$-Si interface.

<112> is the preferred growth direction of the $TiSi_2$ nucleated Si nanowire observed by SEM and TEM. Fig. 3-9 shows two SEM images at different angles. Fig. 3-9 (a) is taken when the substrate [110] direction is at 35° to the horizontal plane, and Fig. 3-9 (b) is taken when that angle is –55°. Fig. 3-9 (a) shows the cross-sectional area of the nanowire, and Fig. 3-9 (b) shows almost the full length of the nanowire. From the angle relationship, we can easily figure out that the growth direction is [112], if we assume the nanowire is epitaxial to the Si substrate.

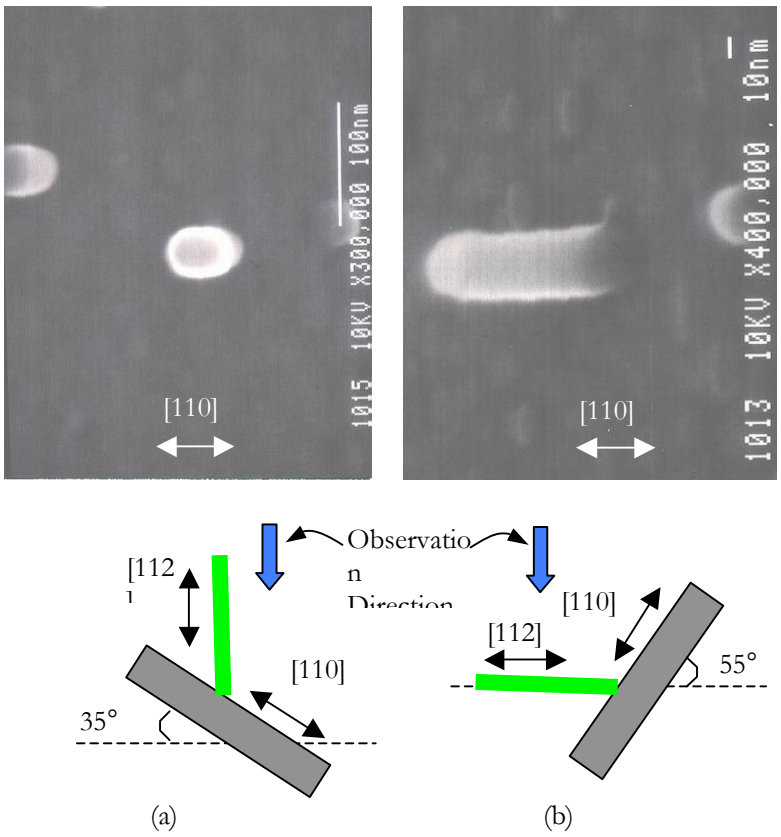


Figure 3-9 SEM images and schematic diagrams show the growth direction of a straight nanowire.

This observation is further proved by TEM observations, which show that most straight stems of Si nanowires demonstrate two types of alignments between {111} planes and the growth direction if observed from <110> directions. They are shown in Fig. 3-10. The two of {111} planes are at about the same angle (~ 35°) to the growth direction in Fig. 3-10 (a), so the growth direction should lie in the (110) plane between the two {111} planes. In Fig. 3-10 (b), one of the {111} planes is parallel to the growth direction, so the growth direction should lie in this (111) plane. If we assume that the two TEM images show the same growth direction, then the only possible growth direction is the cross-section between the (110) plane and the (111) plane, i.e. one of the <112> directions, as explained by the simple crystallographic relationship shown by the schematic diagrams in Fig. 3-10.

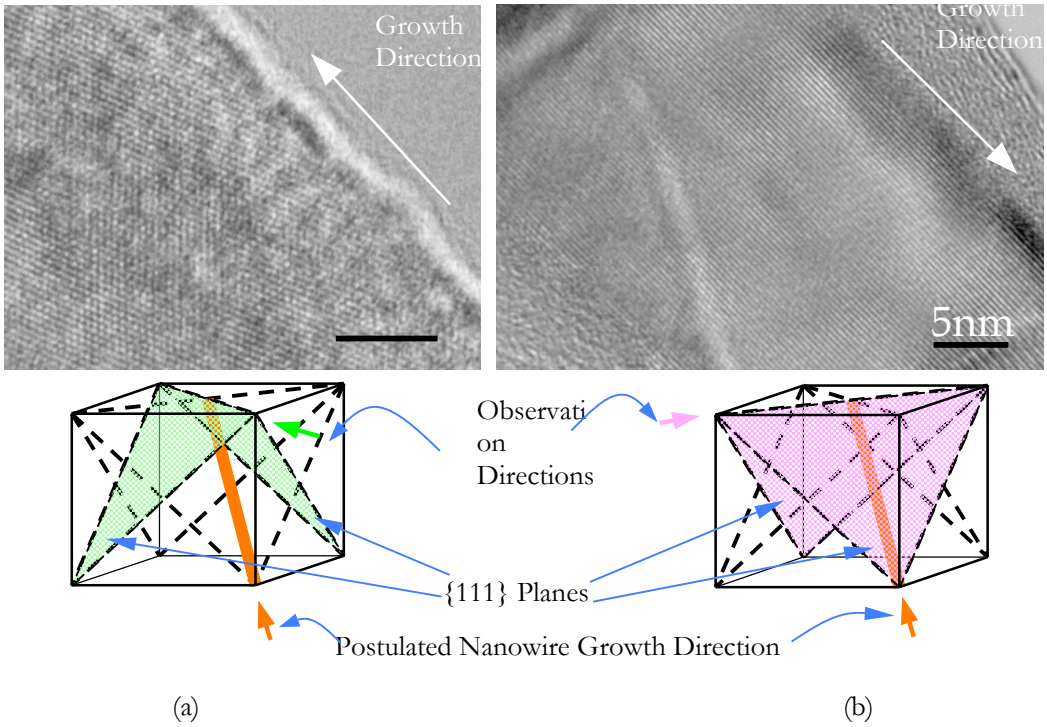
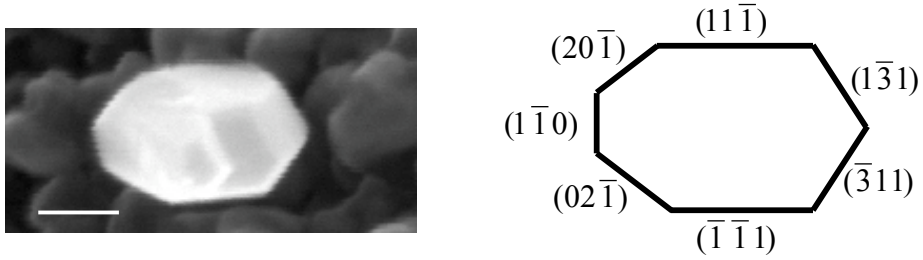


Figure 3-10. TEM images and schematic diagrams show the alignments between {111} planes and the growth direction.

For the growth direction of <112>, the sidewalls are most likely {111}, {110}, {021}, and {113}. Without sidewall growth or annealing, the nanowires are most likely not faceted. After sidewall growth, the final sidewall facets depend on the growth speed of every crystal plane: the fastest growing planes, such as {110}, will disappear first, leaving the slowest growing planes, such as {111}. Fig. 3-11 (a) shows a nanowire with sidewall facets after sidewall growth. With the two {111} facets determined by their alignment with the substrate flat, the other facets are determined by their angular relationship to the flats and are shown schematically in Fig. 3-11 (b). Here we see large {111} facets, while only a small {110} facet.



(a) (b)

Figure 3-11. (a) SEM image and (b) schematic of Si nanowire sidewall facets. Scale bar 40 nm.

3.2 Kinking and Twinning

Many of the Si nanowires shown above are kinked. The ratio of kinked nanowires to the total number of nanowires is much higher than the case of VLS growth. With our MBE chamber cleaner than the apparatus used by Wagner *et al.*[11-14,16] and Givargizov[18,75], and no temperature change during the growth, the kinking shouldn't be caused by either impurities or temperature instability. I believe that kinking is due to the stress at the $TiSi_2$-Si interface, where the new Si crystal growth happens.

The RHEED image of the grown nanowires exhibits very regular pattern, but different from the single crystal Si pattern, as shown in Fig. 3-12.

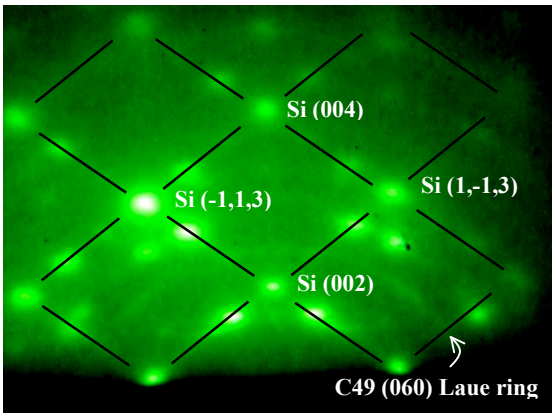


Figure 3-12. Typical RHEED pattern after Si nanowire growth.

In the figure, we see the Si spots from the epitaxially oriented nanowires (connected by black lines), and other spots, which will be verified below to arise from the twinned silicon crystal in the nanowires. In addition, we see a diffuse Laue ring corresponding to C49 $TiSi_2$ {060}, originating from the $TiSi_2$ islands at the nanowire tips, which are almost randomly oriented due to the kinking of nanowires and the change of $TiSi_2$-Si relative orientation

during growth. Other C49 Laue rings are too weak to be clearly observed. For this measurement, the electron-beam is incident along the [-110] substrate direction.

A simulation is used to verify whether the extra spots in Fig. 3-12 come from silicon twins. First, the orientation relationships between epitaxial silicon and twinned silicon are established; then, the RHEED pattern simulation for epitaxial silicon together with twinned silicon is generated using Mathematica.

Fig. 3-13 (a) shows four nonequivalent {111} planes in a substrate silicon unit cell. This original lattice is called lattice O, and the twinned lattices relative to the original orientation along the four {111} planes and are called lattices A, B, C, and D, which are all first-order twins. The twins formed from the first-order twins are second-order twins, and so forth. Fig. 3-13 (b) shows the relative orientation between the original silicon lattice and the four first-order twinned silicon lattices, and Fig. 3-13 (c) shows how a second-order twinned silicon lattice orients relative to one first-order twin and the substrate, where the actual lattices shown are lattice B1 (second-order twin), lattice B (first-order twin), and lattice O (substrate). Since all the coordinates are Cartesian, we can change a vector in the old coordinates to one in the new coordinates by multiplying by a transformation matrix M. M is found by writing expressions for the old x-, y-, and z- unit vectors in the new coordinates; they form the columns of the matrix M[76]. For our case, the transformation matrices relating lattices A, B, C, and D to lattice O are the four matrices listed in Table 3-1, i.e., MA, MB, MC, MD. The transformation matrices relating the second-order lattices to the first-order lattices are the same four matrices shown in Table 3-1 because, for example, the relationship between lattice A and its second-order twins is the same as that between lattice O and lattice A, B, C, and D. And one second-order twin of lattice A is lattice O (also can be viewed as a result of transformation matrix MA·MA=I, the identity matrix), so lattice A's second-order twin only generates three new lattice orientations, which are called lattice A-1, A-2, and A-3, and their transformation matrices relative to lattice O are (MA·MB), (MA·MC), and (MA·MD). By analogy, the other second-order twins are lattices B-1, B-2, B-3, C-1, C-2, C-3, D-1, D-2, and D-3. The higher the order of the twins, the more lattice orientations they include. Also, for our case, the higher the order of the twins, the less abundant they are in the nanowires because a third-order twin has to be generated

from a second-order twin, which has to be generated from a first-order twin, and not every twin crystal generates the higher-order twins. For example, if 100 first-order twin crystals with lattice A generate 60 second-order twin crystals, which should statistically contain equal numbers of lattices A-1, A-2, and A-3, then only 20 twin crystals will have lattice A-1, which should produce a weaker A-1 RHEED pattern compared with A RHEED pattern generated from 100 crystals. Therefore, the intensity of the RHEED pattern decreases as the order increases. Consequently, the third- and higher- order twins are neglected in the following discussion.

Table 3-1. Transformation matrices between the original lattice and the first-order twins. These matrices are bi-directional for silicon lattice, i.e., they equal their inverse.

Orientation relationship	Lattice A to lattice O: MA	Lattice B to lattice O: MB	Lattice C to lattice O: MC	Lattice D to lattice O: MD
Transformation matrix	$\frac{1}{3}\begin{bmatrix} -2 & 1 & -2 \\ 1 & -2 & -2 \\ -2 & -2 & 1 \end{bmatrix}$	$\frac{1}{3}\begin{bmatrix} -2 & 1 & 2 \\ 1 & -2 & 2 \\ 2 & 2 & 1 \end{bmatrix}$	$\frac{1}{3}\begin{bmatrix} 1 & 2 & 2 \\ 2 & -2 & 1 \\ 2 & 1 & -2 \end{bmatrix}$	$\frac{1}{3}\begin{bmatrix} -2 & 2 & 1 \\ 2 & 1 & 2 \\ 1 & 2 & -2 \end{bmatrix}$

To generate the simulated RHEED pattern for the electron-beam incident in the [-110] substrate direction, we need to know the relationship between the substrate [-110] direction and the twin lattices to determine how the RHEED patterns of the twins appear. This can be done by multiplying the substrate direction ([-110]) by the corresponding transformation matrix. In addition, how the RHEED pattern for each twin rotates relative to the original lattice (lattice O) pattern is determined by finding out what a major RHEED spot in the twin pattern corresponds to in the lattice O pattern. This is achieved by multiplying the twin pattern spot index vector by the inverse of the corresponding transformation matrix. All the relationships between lattice O and its first- and second- order twins are listed in Table 3-2.

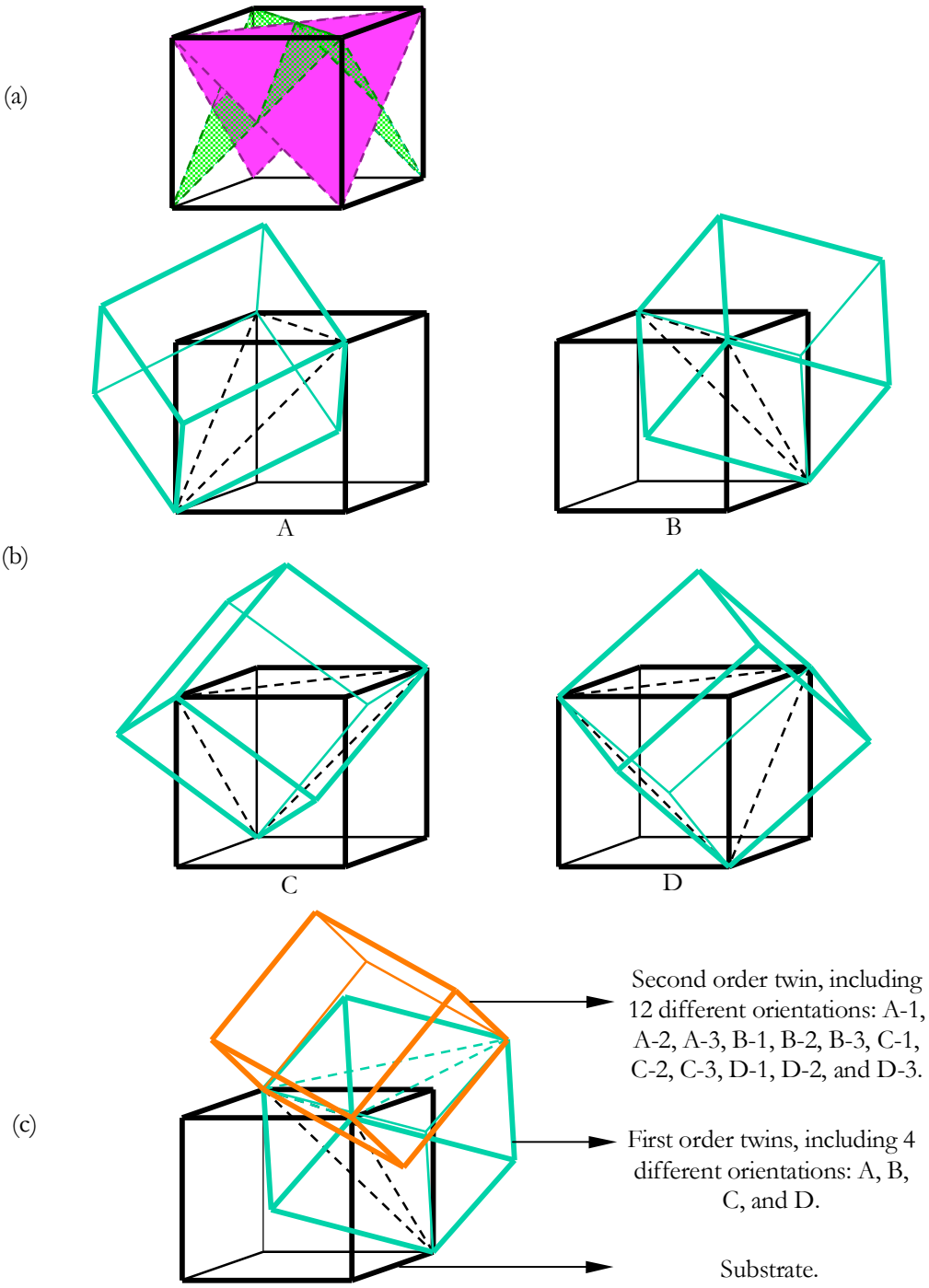


Figure 3-13. (a) The four nonequivalent {111} planes. (b) Relative orientation between original silicon lattice and the first-order twinned silicon lattices, which are named A, B, C, and D. (c) Relative orientation between original silicon lattice, one first-order twinned silicon lattice, and one second-order twinned silicon lattice. The dotted lines outline the {111} planes, relative to which the twin lattices (substrate and first-order twin, or first-order twin and second-order twin) are mirror images.

Table 3-2. The relationships between lattice O and its first- and second- order twins for determining the relative position of their RHEED patterns.

twin	substrate [-110] corresponds to this direction in the twin	what a twin major spot (sub t) corresponds to in lattice O (sub o)	twin	substrate [-110] corresponds to this direction in the twin	what a twin major spot (sub t) corresponds to in lattice O (sub o)
A	$[1, -1, 0]_t$	$(1, 1, 0)_t \Rightarrow \frac{1}{3}(-1, -1, -4)_o$	**B-2**	$[-4, 1, -1]_t$	$(0, 1, 1)_t \Rightarrow \frac{1}{3}(-1, -1, 4)_o$
B	$[1, -1, 0]_t$	$(1, 1, 0)_t \Rightarrow \frac{1}{3}(-1, -1, 4)_o$	**B-3**	$[-1, 4, 1]_t$	$(1, 0, 1)_t \Rightarrow \frac{1}{3}(-1, -1, 4)_o$
C	$[1, -4, -1]_t$	$(1, 0, 1)_t \Rightarrow (1, 1, 0)_o$	**C-1**	$[-8, 7, -7]_t$	$(0, 1, 1)_t \Rightarrow (1, 1, 0)_o$
D	$[4, -1, 1]_t$	$(0, 1, 1)_t \Rightarrow (1, 1, 0)_o$	**C-2**	$[-11, -4, -5]_t$	$(1, 1, -3)_t \Rightarrow (1, 1, -3)_o$
A-1	$[-1, 1, 0]_t$	$(1, 1, 0)_t \Rightarrow \frac{1}{9}(-7, -7, 8)_o$	**C-3**	$[-4, 11, 5]_t$	$(1, -1, 3)_t \Rightarrow (-1, -1, -3)_o$
A-2	$[-1, 4, 1]_t$	$(1, 0, 1)_t \Rightarrow \frac{1}{3}(-1, -1, -4)_o$	**D-1**	$[-7, 8, 7]_t$	$(1, 0, 1)_t \Rightarrow (1, 1, 0)_o$
A-3	$[-4, 1, -1]_t$	$(0, 1, 1)_t \Rightarrow \frac{1}{3}(-1, -1, -4)_o$	**D-2**	$[-11, 4, -5]_t$	$(-1, 1, 3)_t \Rightarrow (-1, -1, -3)_o$
B-1	$[-1, 1, 0]_t$	$(1, 1, 0)_t \Rightarrow \frac{1}{9}(-7, -7, -8)_o$	**D-3**	$[4, 11, 5]_t$	$(1, 1, -3)_t \Rightarrow (1, 1, -3)_o$

Using all the relationships in Table 3-2, a simulated RHEED pattern can be built up using Mathematica. Since [-8,7,-7] and [-7,8,7] in Table II are only 3.68° from [-1,1,-1] and [-1,1,1], and the twins' reciprocal lattice spots have large diameter because the twin crystals are small in real space (normally less than several tens of nanometers in any direction), we replace [-8,7,-7] and [-7,8,7] with [-1,1,-1] and [-1,1,1] as the corresponding directions to include as many spots as possible. The calculated RHEED patterns for lattices A to D, A-1 to A-3, C-1, D-1, and the overlap of them all are shown in Fig. 3-14. Because lattices C-2, C-3, D-2, and D-3 do not introduce new spots into the final overlapped RHEED pattern, their calculated RHEED patterns are not shown. The simulated RHEED pattern corresponding to Fig. 3-12, extracted from Fig. 3-14 (g) is shown in Fig. 3-15.

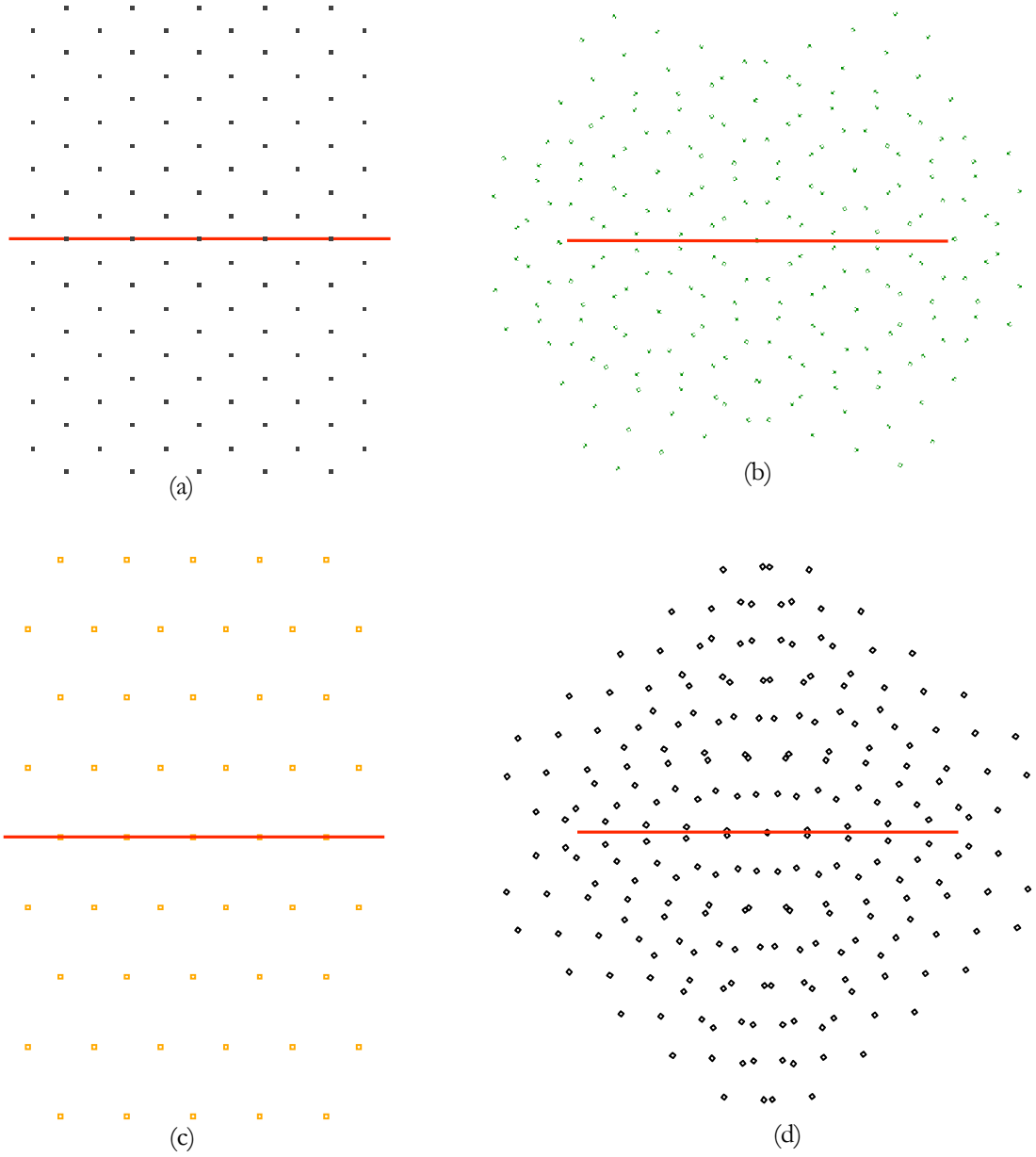


Figure 3-14. Continued on the next page.

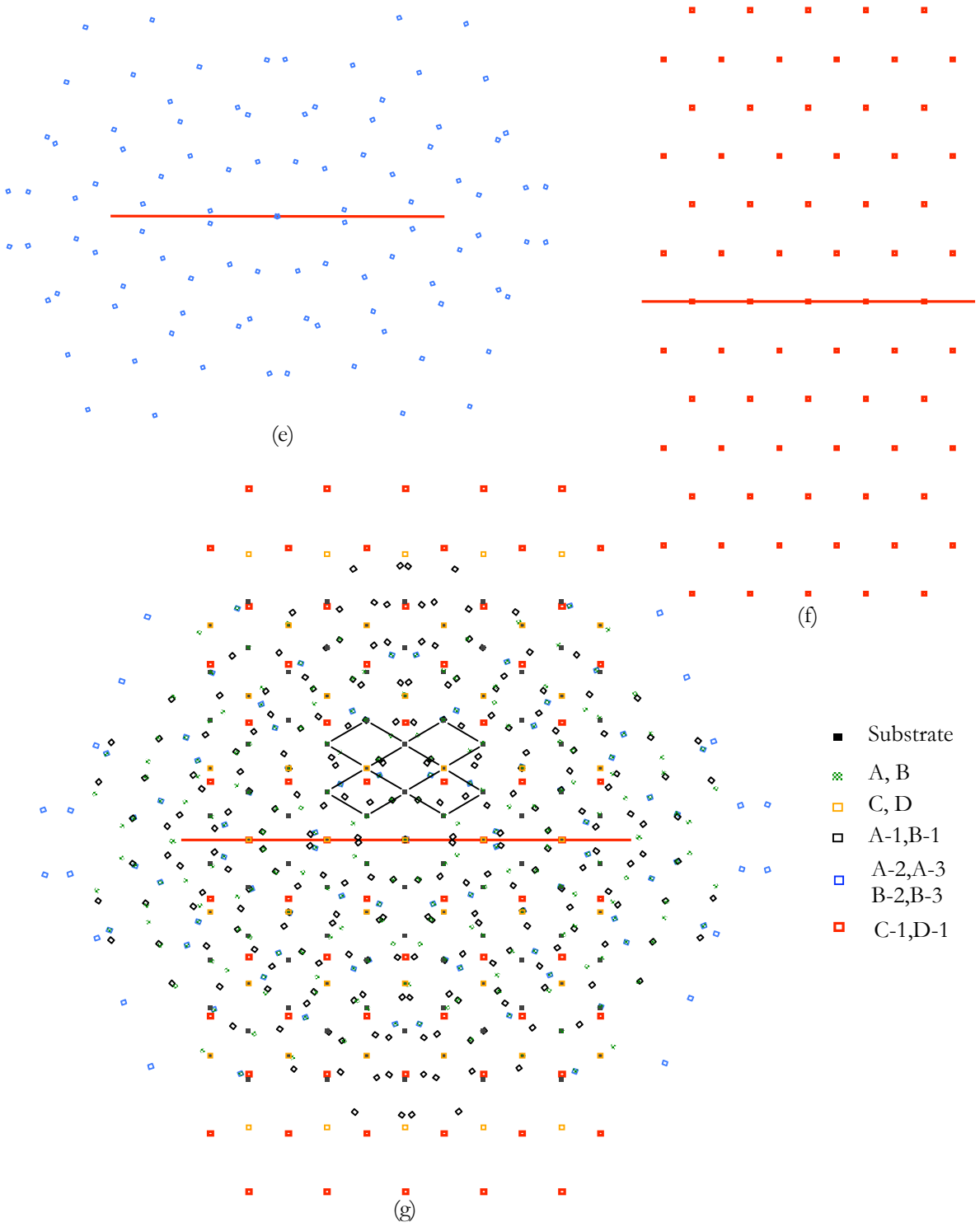
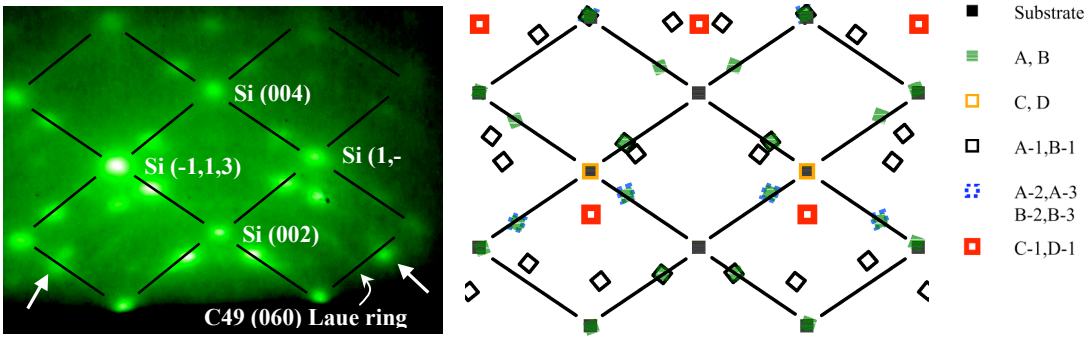


Figure 3-14. The calculated RHEED patterns of (a) (001) Si substrate, (b) lattices A and B, (c) lattices C and D, (d) lattices A-1 and B-1, (e) lattices A-2, A-3, and B-2, B-3, (f) lattices C-1 and D-1. And (g) the overlap of above 6 calculated RHEED patterns. The red lines are the center reference line. The black lines highlights the substrate Si pattern, as also in the extracted pattern in Fig. 3-15.



(a) (b)

Figure 3-15. (a) Repeat of Fig. 3-12. (b) The simulated RHEED pattern for substrate lattice O together with its first- and second- order twins.

We can see that the spot positions in Fig. 3-15 match those in Fig. 3-12 very well. The intensity of each spot is mainly determined by the amount of nanowire volume with the corresponding lattice orientation. The A-1 and B-1 spots are the weakest because statistically, their diffraction volume is less than half of that of other simulated spots. The two unmatched spots, denoted by the two straight arrows in Fig. 3-15 (a), could be from double diffraction.

The presence of twins in the silicon nanowires is confirmed by TEM observation, with a typical image shown in Fig. 3-16, which corresponds to the kink region of a Si nanowire. High-resolution images of the lattices at regions 1, 2, and 3 are shown as the insets, with {111} planes marked by white lines. From these images we can see that region 2 is a first-order twin relative to region 1, and region 3 is a first-order twin relative to region 2 and a second-order twin relative to region 1.

Si and C49-$TiSi_2$ are not lattice-matched because Si has a diamond structure with lattice parameter of 0.5431nm and C49-$TiSi_2$ has an orthorhombic structure with lattice parameters of 0.362nm, 1.376nm, and 0.360nm. Moreover, in our growth process, the $TiSi_2$ islands remain in the solid state, which is different from VLS growth situation where the catalyzing islands are in the liquid state, reducing the stress at the island-Si interface. For the orientation of Si[110]//C49-$TiSi_2$[100], Si[$\bar{1}$10]//C49-$TiSi_2$[001], and Si(001)//C49-$TiSi_2$(010), the lattice mismatch between Si[110] and C49-$TiSi_2$[100] or between Si[$\bar{1}$10] and C49-$TiSi_2$[001] is approximately 6%, which is a large mismatch in crystal growth. So

in Ti-catalyzed Si nanowire growth, the strain between C49-$TiSi_2$ islands and the Si lattice is possibly responsible for the kinking shown in Fig. 3-16.

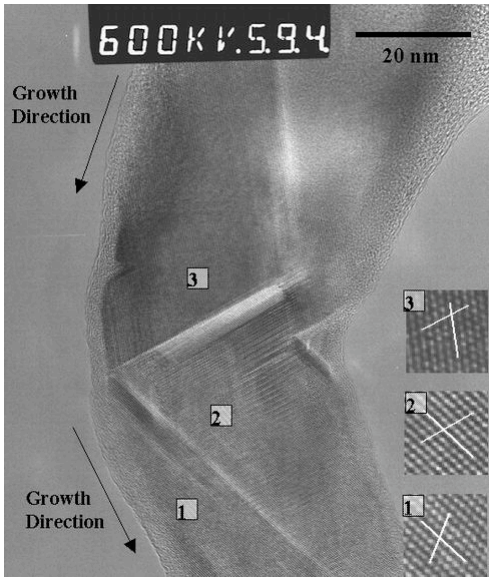
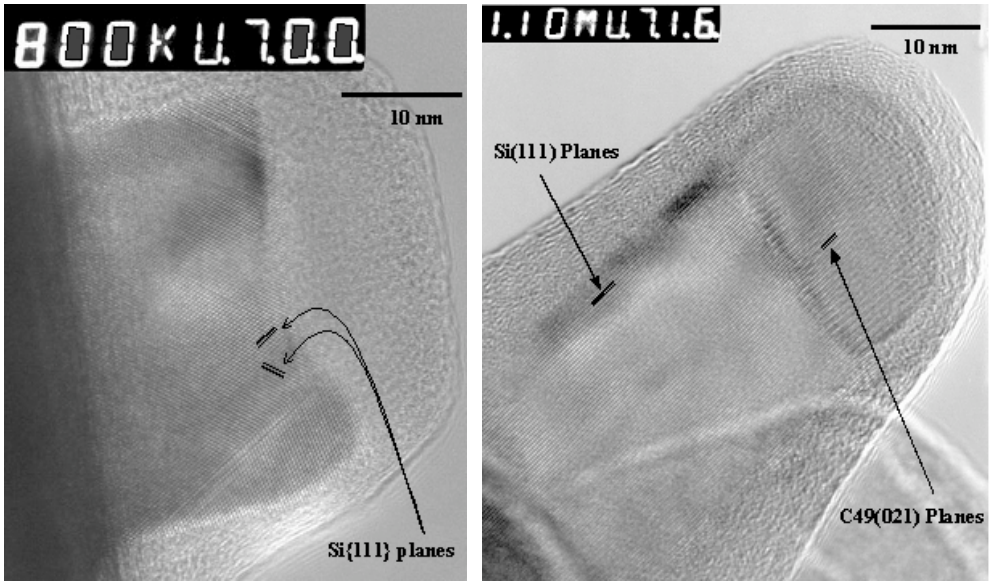


Figure 3-16. Transmission electron micrograph of a Si nanowire containing twin crystals. The insets are the enlarged Si lattice image at positions 1, 2, and 3. The white lines represent Si(111) planes orientation. Si lattice at position 1 is twin relative to that at position 2, which is twin relative to that at position 3.

Fig. 3-17 (a) shows a Si nanowire where a twin is starting to develop at its lower side in the image and a highly defected Si crystal containing stacking faults is forming at the upper side. The possible understanding for Fig. 3-17 (a) is that the stress at the interface between C49-$TiSi_2$ islands and Si causes the Shockley partial dislocation to glide through silicon crystal along {111} planes, possibly starting from the edge of $TiSi_2$ islands, where the starting of dislocation is easiest. If the Shockley partial dislocation glides through every parallel {111} plane, a twin crystal forms; otherwise, a highly defective crystal full of stacking faults forms. A schematic of the face-centered-cubic (FCC) crystal (-110) projection and the stacking fault and twin formed by Shockley partial dislocation are shown in Fig. 3-18.

After the twin is formed, it grows along with the nanowire, as shown at position 1 in Fig. 3-16. When the twin is large enough to dominate the growth, the wire changes to the new growth direction dominated by the twin crystal, resulting in a kink. The twinning process can happen several times during the nanowire growth. The nanowire can therefore change growth direction several times, leaving large twinned regions in the nanowires.

These twinned regions cause the twin diffraction spots in the RHEED pattern after growth, as shown in Fig. 3-15.



(a) (b)

Figure 3-17. Transmission electron micrographs of the grown Si nanowires. (a) A short nanowire. (b) Upper part of a nanowire. There is a thin layer of native oxide (~2nm) surrounding the nanowires and the C49 $TiSi_2$ islands, but the amorphous coating layer also comes from the wax we used for preparing the TEM samples, especially where close to the substrate. In (a), no lattice fringe is observed in the C49 $TiSi_2$ crystal because the imaging electron beam was not aligned for it. In (a), the dark region in the left part of the image is the substrate.

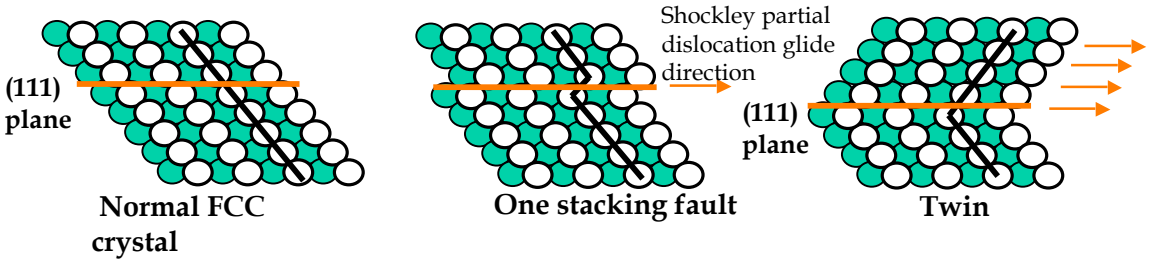


Figure 3-18. Schematic of the normal FCC crystal (-110) projection and the stacking fault and twin formed by gliding through of Shockley partial dislocations.

For $TiSi_2$ catalyzed nanowires, twinning does not occur in every nanowire, with Fig. 3-17 (b) as an example. Notice that the (021) planes in the C49-$TiSi_2$ tip are parallel to and matching the (111) planes in the Si nanowire very well. This orientation relationship between C49-$TiSi_2$ tip and Si nanowire is different from the one observed in RHEED. The calculated interplanar distance of C49 $TiSi_2$ (021) is 0.3190nm, which is 1.7% larger than the calculated Si (111) interplanar distance of 0.3136nm. Since in Fig. 3-17 (b) no twinning

is observed, the 1.7% lattice mismatch between C49-$TiSi_2$ tip and Si nanowire is probably not large enough to form a twin or highly defected crystal in the Si nanowire given the fact that the Si nanowire is only about 25 nm wide and both the tip and the nanowire are not confined laterally.

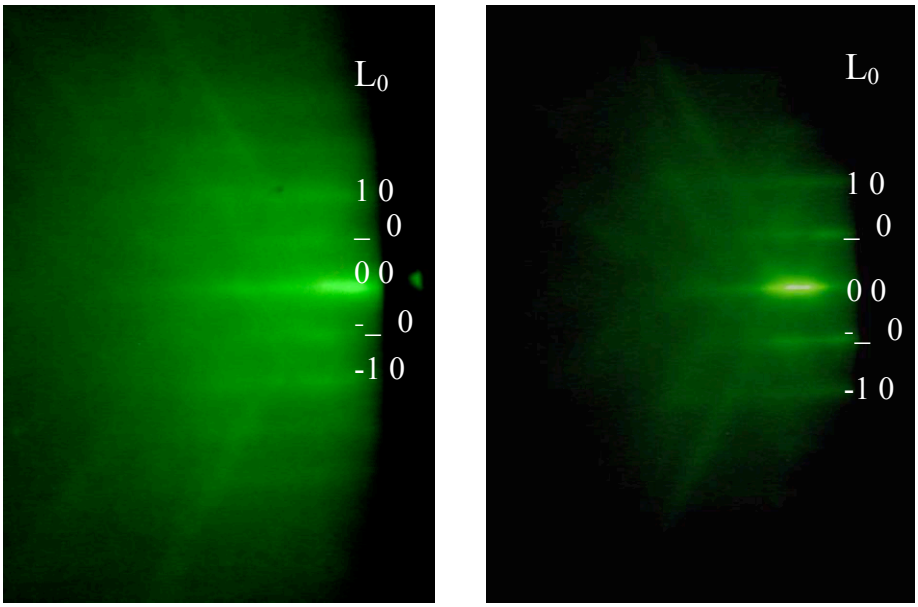
Chapter 4

Study of Titanium Silicide Islands

We have already seen that for Ti-silicide nucleated Si nanowires, the growth behavior is very much related to the catalyzing Ti-silicide islands, because those islands are where the decomposition of Si2H6 and the subsequent Si atom transport and condensation occur. Unlike VLS growth, the solid state of the Ti-silicide islands gives rise to strain and stress at the tip of the growing nanowire, resulting in kinked and non-uniform growth, especially on Si (001) substrates. This chapter presents the results of our detailed study of Ti-silicide islands.

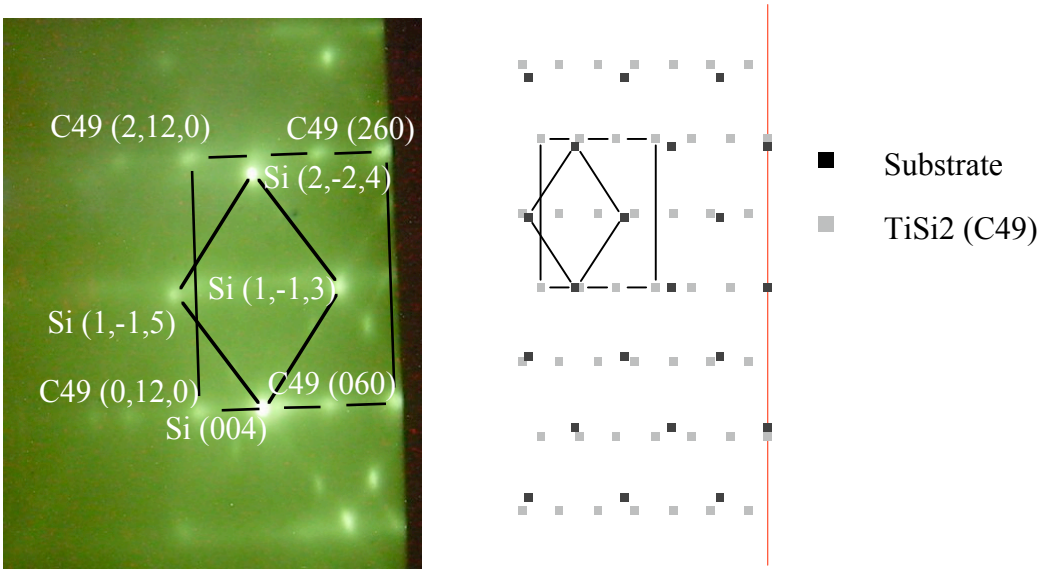
4.1 Titanium Silicide Islands on Si substrate Surface

To form the catalyzing islands, of the order of one monolayer of Ti was first deposited on Si (001) wafers at 538°C, annealed at 850°C for 10 minutes (during which islands form), then cooled to 538°C. The islands have diameters of 20 to 40 nm and cover about 20% of the wafer surface. The RHEED pattern for the sample after Ti deposition and before annealing is shown in Figs. 4-1 (a), where we see the streaks of the silicon (2□1) surface reconstruction, Kikuchi lines, and a strong diffuse background [compared with Fig. 4-1 (b)] caused by the diffraction from the surface Ti or $TiSi_x$ layer. While 500°C is high enough for Ti atoms to migrate and intermix with Si atoms, the absence of Laue rings or TiSix diffraction spots in the RHEED pattern indicates that no single crystalline phase is dominant at the surface Ti or $TiSi_x$ layer.



(a) (b)

Figure 4-1. RHEED patterns for (a) the substrate surface with approximately one monolayer of Ti deposited at 550°C, and (b) the reconstructed clean Si surface before Ti deposition, with substrate [110] as electron beam-incidence direction. L_0 is the zero order Laue zone.



(a) (b)

Figure 4-2. (a) RHEED pattern for the beginning of silicon nanowire growth (30 s), with substrate [110] as electron-beam incidence direction. (b) Simulation of the diffraction spot configuration for the orientation of Si[110]//C49-$TiSi_2$[100] and Si(001)//C49-$TiSi_2$(010), with the black lines outlining the same region as in (a).

The presence of well-orientated C49 $TiSi_2$ can be seen in the RHEED pattern in Fig. 4-2 observed near the beginning of the nanowire growth (after the first 30 seconds of the 60 minute typical nanowire growth time). In Fig. 4-2, in addition to the epitaxial Si diffraction

spots (with four spots indexed and outlined by the black-line rhombic shape), we see the C49 $TiSi_2$ (0,6,0), (2,6.0), (0,12,0), (2,12,0) diffraction spots clearly at the four corners of the rectangular outlined by black lines. The simple configuration simulation in Fig. 4-2 (b) shows the position of the spots. Comparing the measured pattern with the simulation, we see that the surface Ti has been fully alloyed with silicon, forming the final Si-rich phase C49-$TiSi_2$ after annealing at 820°C for 10 minutes. One orientation of the $TiSi_2$ islands dominates, namely

Si[110]//C49-$TiSi_2$[100] and Si(001)//C49-$TiSi_2$(010).

This is consistent with the observations of Briggs *et al.*[77] Because (1) only approximately one monolayer of Ti was deposited, and (2) the $TiSi_2$ islands cover only ~20% of the wafer surface, the clearly observable extra $TiSi_2$ diffraction spots in the RHEED pattern indicates that most of the $TiSi_2$ islands have this orientation. Another indication of the existence of C49 $TiSi_2$ is the diffuse Laue ring corresponding to C49-$TiSi_2$ {060} after Si nanowire growth, as shown in Fig. 3-12. In Fig. 4-2, we can also see Si (0, 0, 4), (1, -1, 3), (1, -1, 5), (2, -2, 4), and other diffraction spots, corresponding to the substrate, and additional diffraction spots that do not belong to the Si substrate. The additional diffraction spots come from the Si twins, which has been verified in Chapter 3, in the initial Si crystal grown underneath the $TiSi_2$ islands.

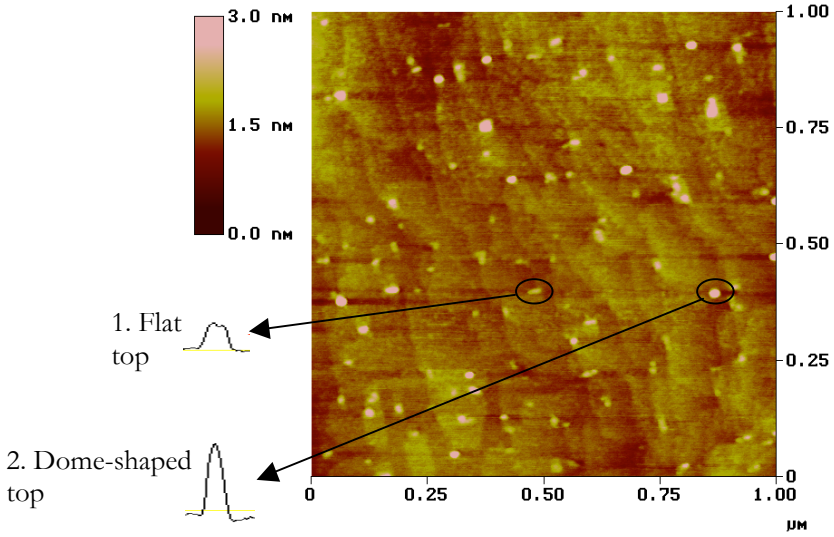


Figure 4-3. $TiSi_2$ islands after deposition at 538°C and annealing at 850°C. The inserts show cross-sections of the circled islands. Island 1 is flat-topped island and island 2 is dome top type.

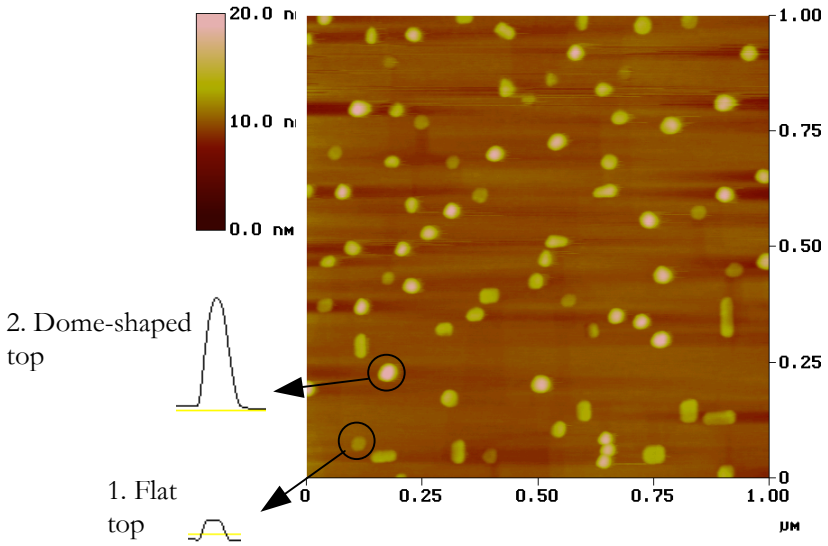


Figure 4-4. $TiSi_2$ islands after deposition at 850°C and annealing at 850°C. The inserts show cross-sections of the circled islands. Island 1 is a flat-topped island and island 2 is dome top type.

An AFM image of $TiSi_2$ islands deposited at 538°C and annealed at 850°C is shown in Fig. 4-3. Fig. 4-4 shows an AFM image of $TiSi_2$ islands both deposited and annealed at 850°C. The island cross-section profile insets are extracted from the images by using Nanoscope III 4.43r8, an AFM image analysis software from Veeco Instruments. Both profile insets in the same figure are enlarged by the same ratio. As seen in both images, there are two types of islands: one type has a flat top and tends to elongate along one of the <110> directions[78]; the other type has a dome-shaped top and is usually round. The differences arise from different deposition conditions; in Fig. 4-3, where the deposition temperature is 540°C, most of the islands have flat tops, while in Fig. 4-4, where the deposition temperature is 850°C, most of the islands are dome-like. This means that dome-like islands are easier to nucleate at higher deposition temperature, and that once the flat-topped islands have been formed, 10 minutes of annealing cannot change their type. Fig. 4-5 is a zoom-in 3D AFM image of the 850°C deposited islands, which clearly shows difference between the two types of islands. The above RHEED study showed that the flat-topped islands, which are the dominant island species in the RHEED images in Fig. 4-2, are C49-$TiSi_2$ with orientations of Si[110]//C49-$TiSi_2$[100] and Si(001)//C49-$TiSi_2$(010). Later in this chapter, TEM observations will show that the dome-like islands are also C49-

$TiSi_2$, but without a preferred orientation. Therefore, we think the difference between the two types of islands is their orientation relative to the Si substrate.

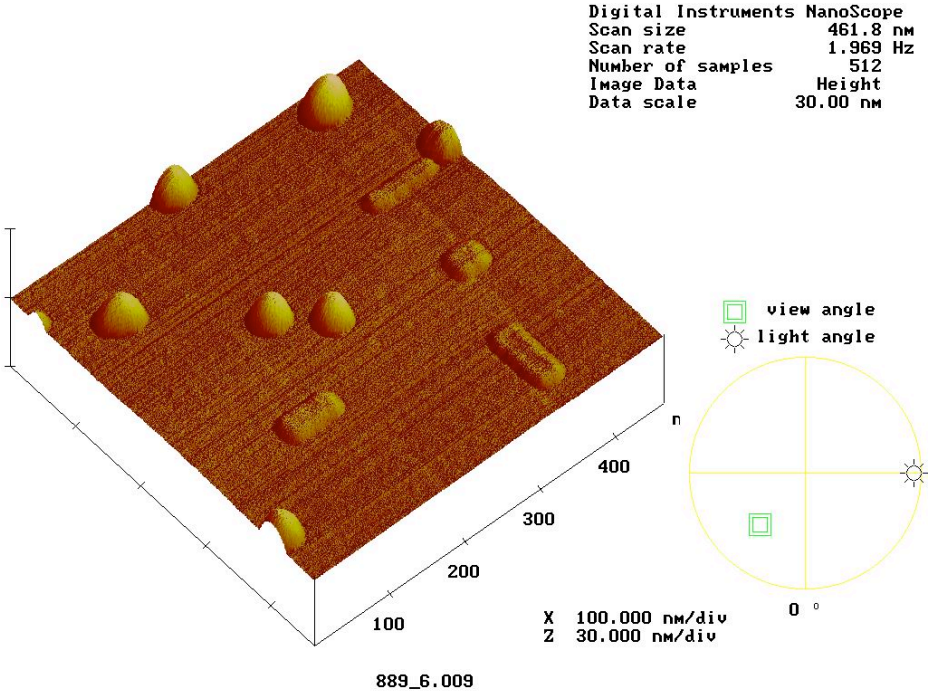


Figure 4-5. AFM 3D image of the $TiSi_2$ islands deposited and annealed at 850°C, showing four flat-topped islands, which are rectangular-shaped and tend to elongate along both <110> directions, and some dome-shaped islands, which are higher and have more round bases.

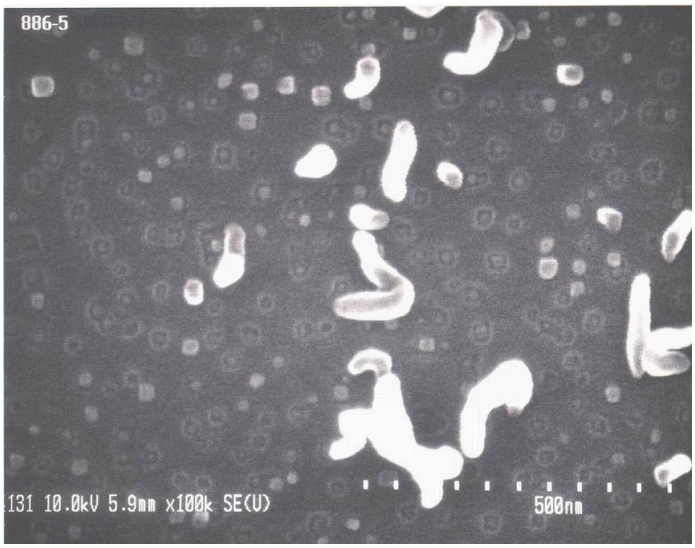


Figure 4-6. SEM image of Si nanowires grown at 540°C with 1.25 sccm of Si_2H_6. The $TiSi_2$ islands were prepared by deposition at 540°C and annealing at 850°C.

Figure 4-6 shows Si nanowires grown at 538°C for 3 hours using 1.25 sccm of Si_2H_6. The $TiSi_2$ islands were prepared by deposition at 540°C and annealing at 850°C. It shows that flat-topped $TiSi_2$ islands did not nucleate Si nanowires, but instead there is a ring of material around them. We believe that the nucleated nanowires were nucleated on the dome-like islands because a) we do not clearly see any dome-like islands in Fig. 4-6, b) the nanowire density is similar to the dome island density, and c) the normal growth on a Si substrate without catalyst is very slow (< 0.1nm/min), indicating that the islands should not be buried. Again, the difference in the ability of the two types of $TiSi_2$ islands to nucleate Si nanowires can be attributed to differences in Si condensation rate at the $TiSi_2$-Si interface.

4.2 Titanium Silicide Islands Observed by TEM

4.2.1 TEM Sample Preparation

TEM is the best way to observe the orientation of the $TiSi_2$ tips and the nanowires and to observe the $TiSi_2$-Si interface. But traditional cross-section TEM sample preparation is time-consuming and has low yield. Micro-cleaving the wafer to produce sharp tips may produce some useful TEM samples, but provides little control. Electron-beam lithography followed by anisotropic etch can produce more samples with better control, but it is still very slow in the sense of time per sample and depends on the busy and unreliable electron-beam lithography machine here at the Stanford Nanofabrication Facility. To produce cross-section TEM samples quickly (in the sense of time per sample) and with good control, I developed a method which combines 365 nm wavelength optical photolithography and deep reactive ion etch (RIE). The minimum feature dimension had to be larger than 1.5 μm for low cost photolithography mask. The steps in the sample preparation process are described below and schematically shown in Fig. 4-7.

(1) Bond the nanowire substrate onto another Si substrate.

(2) Coat the substrate with 1.6 μm positive photoresist, and expose mask 1 on it, as shown in Fig. 4-7 (a).

(3) Expose mask 2 on the substrate, as shown in Fig. 4-7 (b). Mask 1 and mask 2 define the pattern with sharp tip regions which will be less-than-100nm thick and transparent to TEM electron beam.

(4) Develop the photoresist and etch down 10 μm by deep RIE, with the photoresist as etch mask, as shown in Fig. 4-7 (c).

(5) Coat the substrate with 10 μm positive photoresist, and expose mask 3 on the substrate, as shown in Fig. 4-7 (d). Mask 3 defines the final TEM sample size, which depends on the TEM machine sample holder size and is 100 μm × 2.9 mm here.

(6) Develop the photoresist and etch through the top substrate by deep RIE, as shown in Fig. 4-7 (e).

(7) Remove the photoresist by oxygen plasma etch.

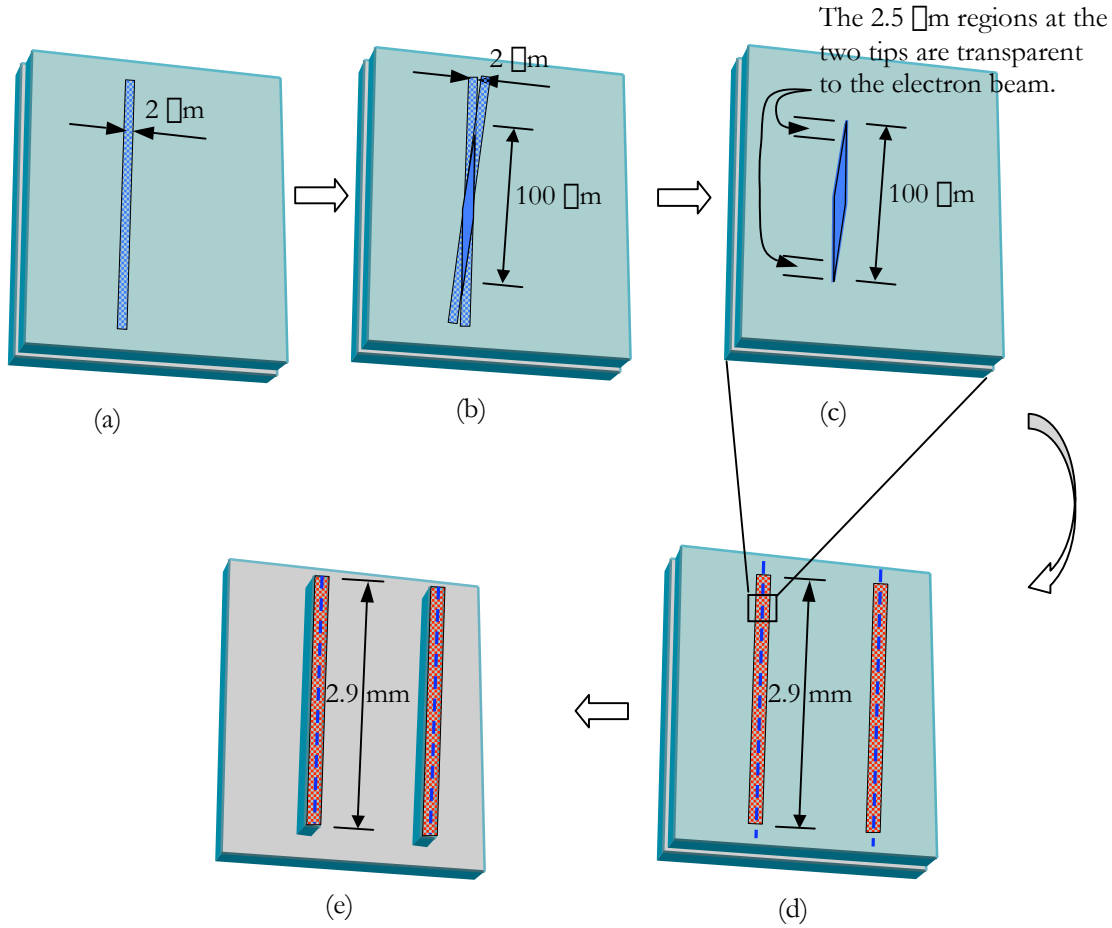


Figure 4-7. Schematics of my cross-section TEM sample preparation process.

The result of the optical lithography (step 3) is shown in Fig. 4-8. The TEM samples used in this work are produced by either the method described above or a micro-cleaving technique.

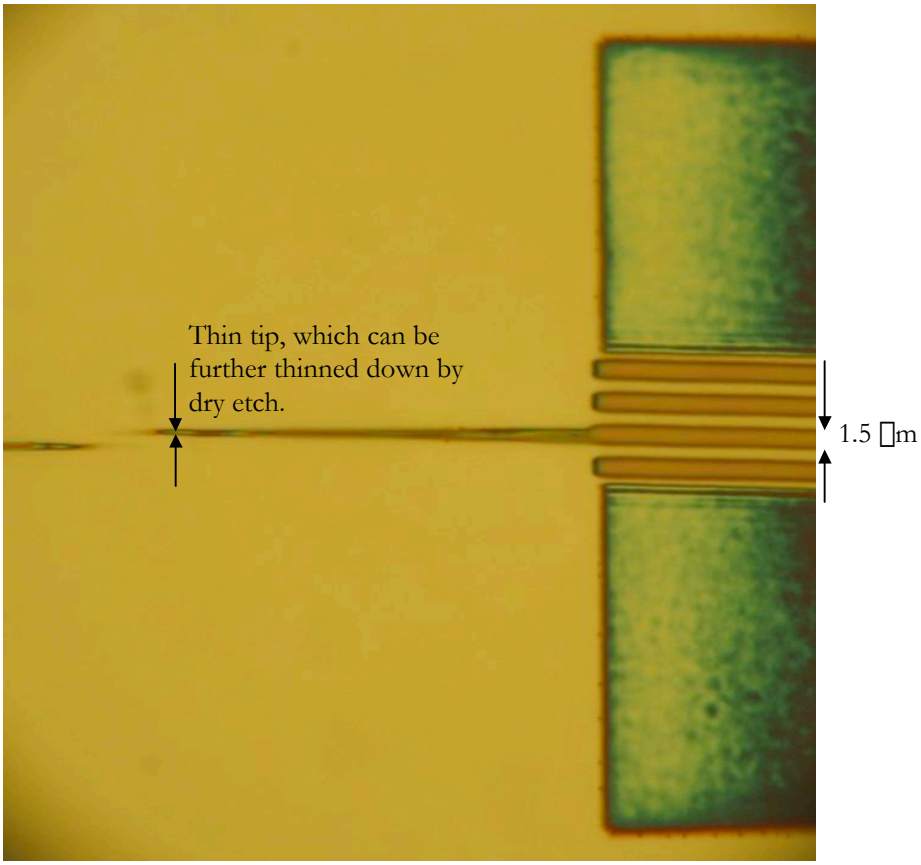


Figure 4-8. Optical microscope image showing optical lithography (365nm wavelength) result after step (3).

4.2.2 Coordinate Transformation Basics [76]

The orientation between the $TiSi_2$ islands and the underlying Si crystal can be represented by a transformation matrix. Because this approach may not be familiar to most readers, the basics of coordinate transformation from the text by Roussear [76] are provided in this section.

Consider a transformation from coordinates a, b, c, to coordinates a1, b1, c1. The relations between the basis vectors (a, b, c, and a1, b1, c1), the reciprocal vectors (A*, B*, C*, and A1*, B1*, C1*), the direct rows (i.e. the direction vectors [u v w] and [u1 v1 w1]), and the reciprocal rows [i.e. the real-space planes (h k l) and (h1 k1 l1)] are written in the following matrix forms:

$$\begin{pmatrix} a1 \\ b1 \\ c1 \end{pmatrix} = (M)\begin{pmatrix} a \\ b \\ c \end{pmatrix},\quad \begin{pmatrix} A1^* \\ B1^* \\ C1^* \end{pmatrix} = (M^*)\begin{pmatrix} A^* \\ B^* \\ C^* \end{pmatrix},\quad \begin{pmatrix} u1 \\ v1 \\ w1 \end{pmatrix} = (U)\begin{pmatrix} u \\ v \\ w \end{pmatrix},\quad \begin{pmatrix} h1 \\ k1 \\ l1 \end{pmatrix} = (H)\begin{pmatrix} h \\ k \\ l \end{pmatrix},$$

where (M) is called the transformation matrix. With (U^T) denoting the transposed matrix of (U), we also have:

$$(u1\ v1\ w1) = (u\ v\ w)\ .\ (U^T)$$

The direct row **r**, the reciprocal row **R*** and their scalar product **r.R*** are the invariants of this transformation:

$$r = (u \quad v \quad w)\begin{pmatrix} a \\ b \\ c \end{pmatrix} = (u1 \quad v1 \quad w1)\begin{pmatrix} a1 \\ b1 \\ c1 \end{pmatrix} = (u \quad v \quad w)(U^T)(M)\begin{pmatrix} a \\ b \\ c \end{pmatrix} \quad (M) = (U^T)^{-1}$$

$$R^* = (h \quad k \quad l)\begin{pmatrix} A^* \\ B^* \\ C^* \end{pmatrix} = (h1 \quad k1 \quad l1)\begin{pmatrix} A1^* \\ B1^* \\ C1^* \end{pmatrix} = (h \quad k \quad l)(H^T)(M^*)\begin{pmatrix} A^* \\ B^* \\ C^* \end{pmatrix} \quad (M^*) = (H^T)^{-1}$$

$$r.R^* = (u \quad v \quad w)\begin{pmatrix} h \\ k \\ l \end{pmatrix} = (u1 \quad v1 \quad w1)\begin{pmatrix} h1 \\ k1 \\ l1 \end{pmatrix} = (u \quad v \quad w)(U^T)(H)\begin{pmatrix} h \\ k \\ l \end{pmatrix} \quad (H) = (U^T)^{-1}$$

We also have: $(M^T)^{-1}$ = (U) and $(H^T)^{-1}$ = (U) = (M*). From this we deduce the relations:

$$(M^*) = (M^T)^{-1} = (U)$$

$$(H) = (M)$$

In the following text, a1, b1, c1, [u1 v1 w1], (h1 k1 l1) are the coordinates, directions, and planes in C49-$TiSi_2$, and a, b, c, [u v w], (h k l) are the coordinates, directions, and planes in Si.

4.2.3 TEM Observation Results and Discussion

Approximately 150 $TiSi_2$ islands were examined under TEM. Most of the islands show lattice constants consistent with C49 phase and there is absolutely no distinctive sign of a

C54 phase. Some TEM images show at least two sets of lattice planes in the $TiSi_2$ island and at least two sets of lattice planes in the Si crystals underneath the island or in the substrate. These images are used to determine the transformation matrices, which are listed in Table 4-1.

Table 4-1. Observed orientation relationships (transformation matrices) between C49-$TiSi_2$ islands and Si crystals. The substrate is Si (001).

Name of the matrix	Transformation matrix	Originally observed plane relationship		Derived plane relationship

dd	$\begin{bmatrix} 0.471 & 0.471 & 0 \\ 0 & 0 & 2.534 \\ -0.469 & 0.469 & 0 \end{bmatrix}$	Si(110)//C49(100)
		Si(1-10)//C49(001)
		(from RHEED)
				Si(110)//C49(100)
				Si(1-10)//C49(001)

dp1	$\begin{bmatrix} 0 & 0.471 & 0.471 \\ 2.534 & 0 & 0 \\ 0 & 0.469 & -0.469 \end{bmatrix}$	Si(011)//C49(100)
		Si(100)//C49(010)
				Si(011)//C49(100)
				Si(100)//C49(010)

pp3	$\begin{bmatrix} 0.365 & 0.365 & 0.422 \\ 1.134 & 1.134 & -1.962 \\ -0.469 & 0.469 & 0 \end{bmatrix}$	Si
		(111) 175.11°
		(11-1) 104.26°
			C49
			(060) 87.57°
			(110) 168.13°
				Si(1,1,-1.73)//C49(060)
				Si(1,1,0.645)//C49(110)

pp5	$\begin{bmatrix} 0.401 & 0.401 & 0.349 \\ -0.938 & -0.938 & 2.158 \\ 0.469 & -0.469 & 0 \end{bmatrix}$	Si
		(111) 175.11°
		(11-1) 65.61°
			C49
			(060) 87.57°
			(110) 168.13°
				Si(1,1,-2.3)//C49(060)
				Si(1,1,1.481)//C49(110)

pp6	$\begin{bmatrix} -0.471 & 0.471 & 0 \\ -0.835 & -0.826 & -2.245 \\ -0.415 & -0.415 & 0.307 \end{bmatrix}$	Si
		(111) 170.84°
		(11-1) 59.80°
			C49
			(021) 24.58°
			(02-1) 82.18°
				Si(110)//C49(021)
				Si(1,1,-2.038)//C49(02-1)

pp7	$\begin{bmatrix} -0.640 & -0.142 & 0.120 \\ 0.707 & -1.688 & 1.752 \\ -0.018 & 0.473 & 0.464 \end{bmatrix}$	Si
		(11-1) 109.18°
		(111) 177.34°
		(220) 142.74°
			C49
			(130) 108.45°
			(031) 39.56°
				Si(1,1,-0.982)//C49(130)
				Si(1,1,6.5)//C49(031)

pp9	$\begin{bmatrix} -0.508 & 0.084 & -0.424 \\ -0.779 & 2.049 & 1.271 \\ 0.383 & 0.383 & -0.383 \end{bmatrix}$	Si
		(2-20) 96.54°
		(202) 35.0°
		(022) 156.0°
			(130) 82.93°
			(-130) 6.39°
			(060) 136.0°
				Si(2,-1.515,0.485)//C49(130)
				Si(1,1,2)//C49(-130)

pp10	$\begin{bmatrix} -0.155 & 0.620 & -0.190 \\ 1.561 & 0.217 & 1.984 \\ -0.499 & -0.237 & -0.367 \end{bmatrix}$	Si
		(111) 74.85°
		(11-1) 8.56°
		(220) 43.99°
			C49
			(1-31) 156.58°
			(150) 66.39°
				Si(1,1,-2.899)//C49(1-31)
				Si(1,1,0.715)//C49(150)

In Table 4-1, in the column of "Originally observed plane relationship", the angles are measured relative to the horizontal direction of the TEM images, and their angular relationship relative to each other leads to the "Derived plane relationship", from which the

transformation matrices are obtained. Matrices ***pp9*** and ***pp10*** are from the $TiSi_2$ islands deposited at 850°C, and the other matrices are from the $TiSi_2$ islands deposited at 538°C. Although the sampling is very limited, the different matrices for high and low Ti deposition temperature support my claim that the preferred $TiSi_2$ island orientation changes when the Ti deposition temperature increases.

Relationship ***dd*** is first from RHEED observation, representing the orientation of dominant non-nucleating islands on the Si (001) wafer surface. It is supported by the TEM image in Fig. 4-9 (b), which shows Si (111) nearly parallel to C49-TiSi2 (130) or to (031), because we know that:

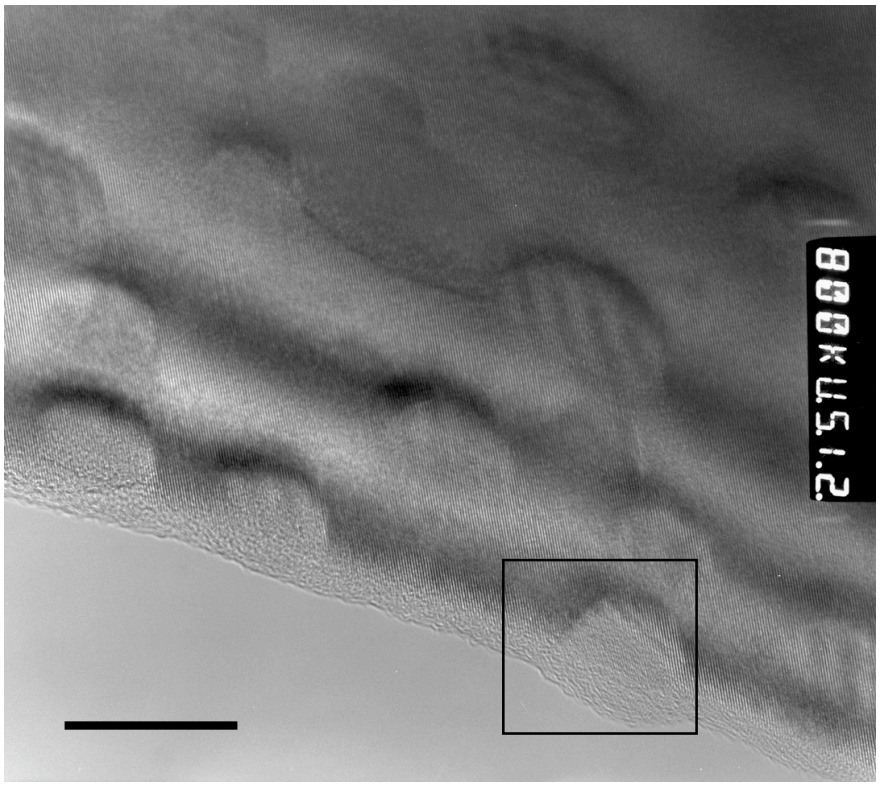
$$dd^{-1}.(0\ 3\ 1)_{C49} = (1, -1, 1.11)_{Si}$$

$$dd^{-1}.(1\ 3\ 0)_{C49} = (1,\ 1, 1.11)_{Si},$$

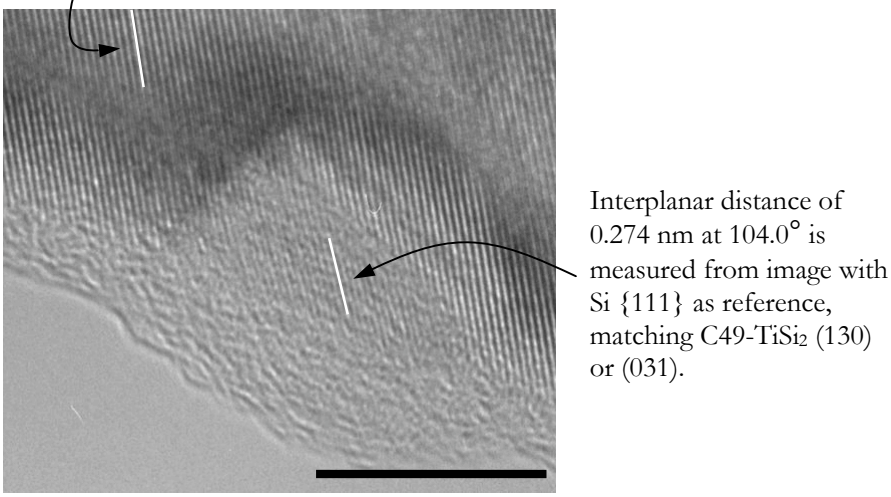
and the angle between Si (111) and Si (1,1,1.11) is (111)Si ^ (1,1,1.11)Si = 2.85°, which matches the 4° difference in Fig. 4-9 (b) reasonably. In addition, some other islands in Fig. 4-9 (a) show Moiré fringes[79] close to $1/(1/d(130)_{C49} - 1/d(111)_{Si})$ □ $1/(1/d(031)_{C49} - 1/d(111)_{Si}) = 2.92$ nm, but with a small angle distribution. This means that the orientations of the non-nucleating islands have a small distribution around relationship ***dd***, which is reasonable because the $TiSi_2$ islands for this orientation are not commensurate to the Si substrate and therefore not able to maintain a strict crystallographic relationship. Later images will show that the islands can be highly defected, and this might explain why not all of the non-nucleating islands show Moiré fringes.

Other than the above observations, one short and highly defected nanowire with a highly defective $TiSi_2$ tip matching orientation ***dd*** was also observed and is shown in Fig. 4-10. This is compatible with our previous observation that flat-topped islands, which have orientation ***dd***, can also nucleate nanowires, especially at higher Ti deposition temperature. This observation excludes the $TiSi_2$ island surface - Si_2H_6 reaction as the rate-limiting step because the non-nucleating islands shown in Fig. 4-9 (a) and the island shown in Fig. 4-10 would then have to have the same top C49 (010) surface, leading to the same surface reaction behavior. Conversely, the interfaces may have different crystalline quality and/or

slightly different orientations, leading to different interface condensation behavior and different heights, which is consistent with our observation.



(a)



(b)

Figure 4-9. (a) TEM images showing non-nucleating islands. Scale bar 20 nm. (b) Enlargement of the outlined rectangular region in (a). Scale bar 10 nm.

Orientation ***dp1*** and orientation ***dd*** are intrinsically the same, but on the Si (001) surface, orientation ***dp1*** equals orientation ***dd*** plus a 90° rotation with C49 [100] or C49 [001] as the axis. Therefore, for orientation ***dp1***, C49 (010) is perpendicular to substrate surface and its interface is different from orientation ***dd***. This further demonstrates that the $TiSi_2$ island orientation and interface are critical to nanowire nucleation.

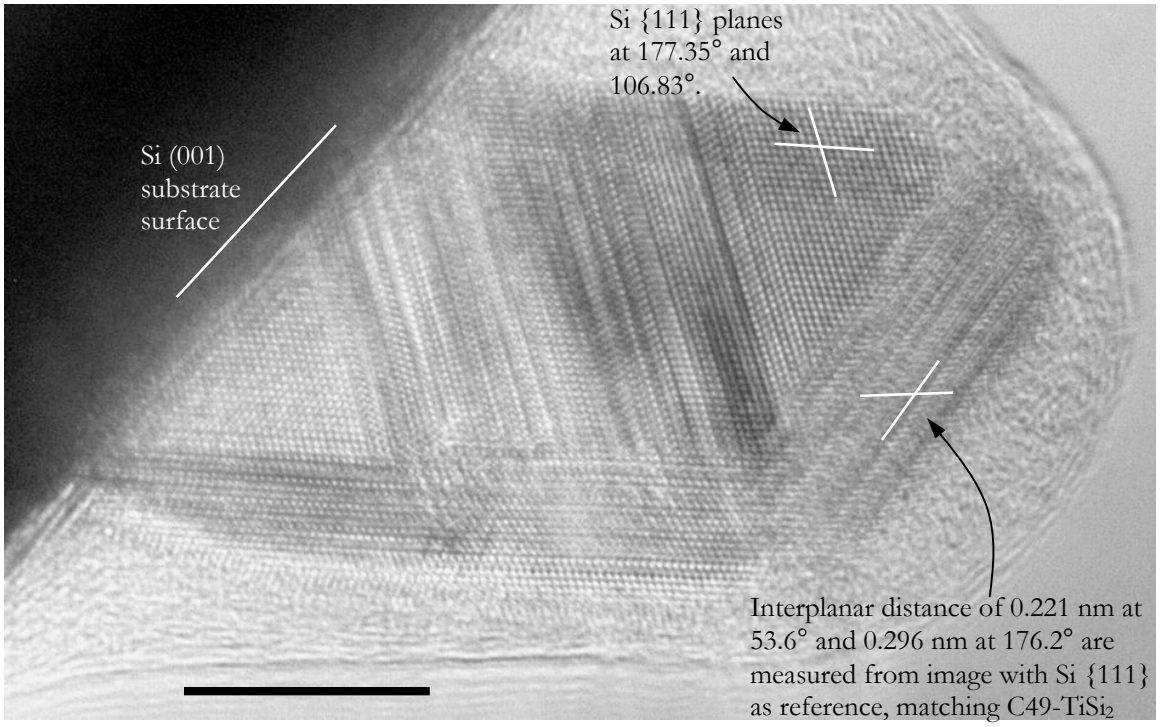


Figure 4-10. TEM Image of a short nanowire and its $TiSi_2$ tip, matching orientation dd. Scale bar 10 nm.

Orientation ***pp3*** is shown in Fig. 4-11. An important feature of this image, which also appears in many other TEM images, is that the $TiSi_2$-Si interface is faceted and stacking faults (lower junction) or strain-induced contrast (upper junction) extend from the junction between facets. The three facets are approximately Si (001) / C49 (1,4.65,0) in the middle, Si (111) / C49 (3.78,1,0) in the lower part, and Si (11-1) / C49 (1,13.73,0) in the upper part. By Si (001) / C49 (1,4.65,0), I mean that the Si (001) facet is parallel to the spacial plane C49 (1,4.65,0) determined by the C49 crystal orientation as if it is a C49 $TiSi_2$ crystal plane. Epitaxial Si crystal grows under the middle and upper facets, while a small Si twin crystal grows under the lower facet. The orientation between the Si twin crystal under the

lower facet and the $TiSi_2$ island matches orientation ***pp5***. The extra strain at the facet junctions may be the reason for the higher density of stacking faults there, which slide along {111} planes and may therefore lead to twin crystals.

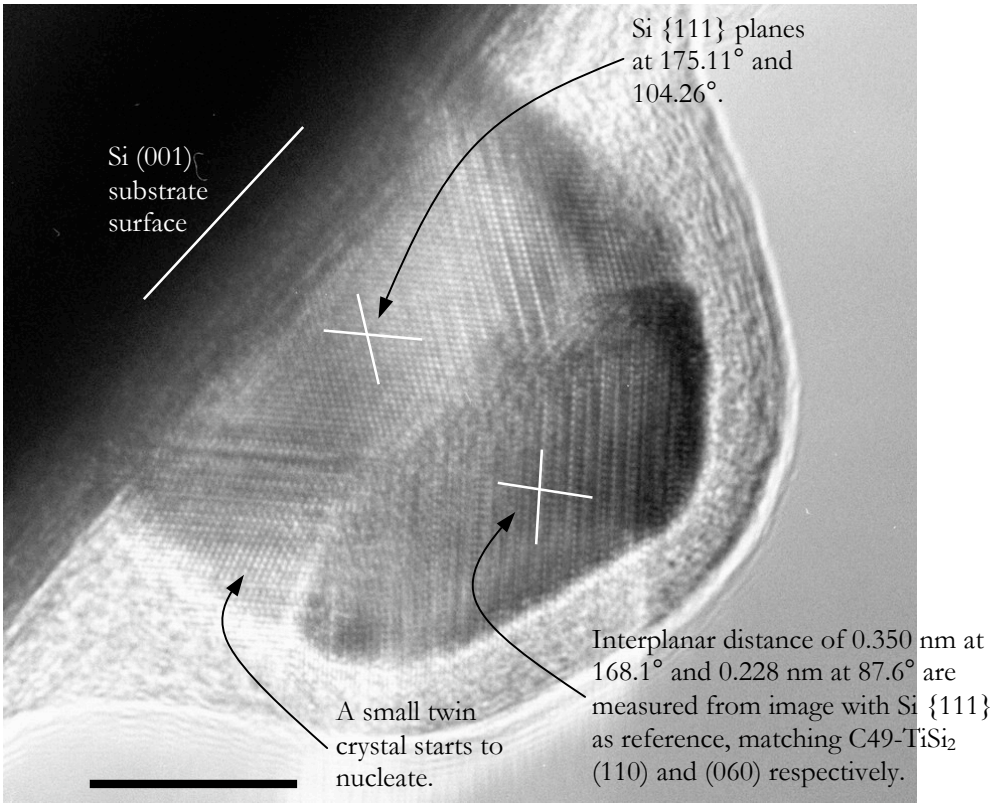


Figure 4-11. TEM Image showing orientations **pp3** and **pp5**. Scale bar 10 nm.

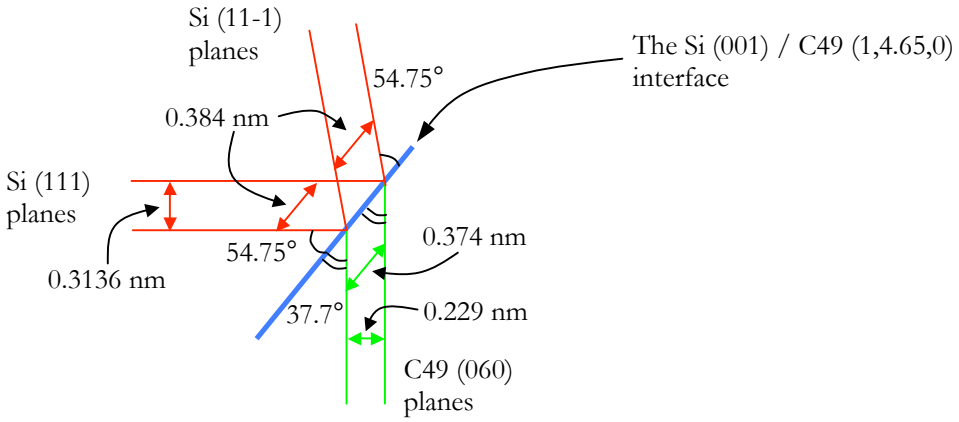


Figure 4-12. Schematics showing relatively good matching between Si {111} and C49 (060) at the Si (001) / C49 (1,4.65,0) interface, corresponding to Fig. 4-11.

For the Si (001) / C49 (1,4.65,0) interface, the Si (111) and (11-1) planes match C49 (060) relatively well at the interface (0.384 nm vs. 0.374 nm), as shown in Fig. 4-12. This

matching may lead to a lower energy interface and explain the existence of stable Si (001) / C49 (1,4.65,0) interface. Among our TEM images with clearly identifiable $TiSi_2$-Si interface, most show a similar configuration which favors interface lattice match.

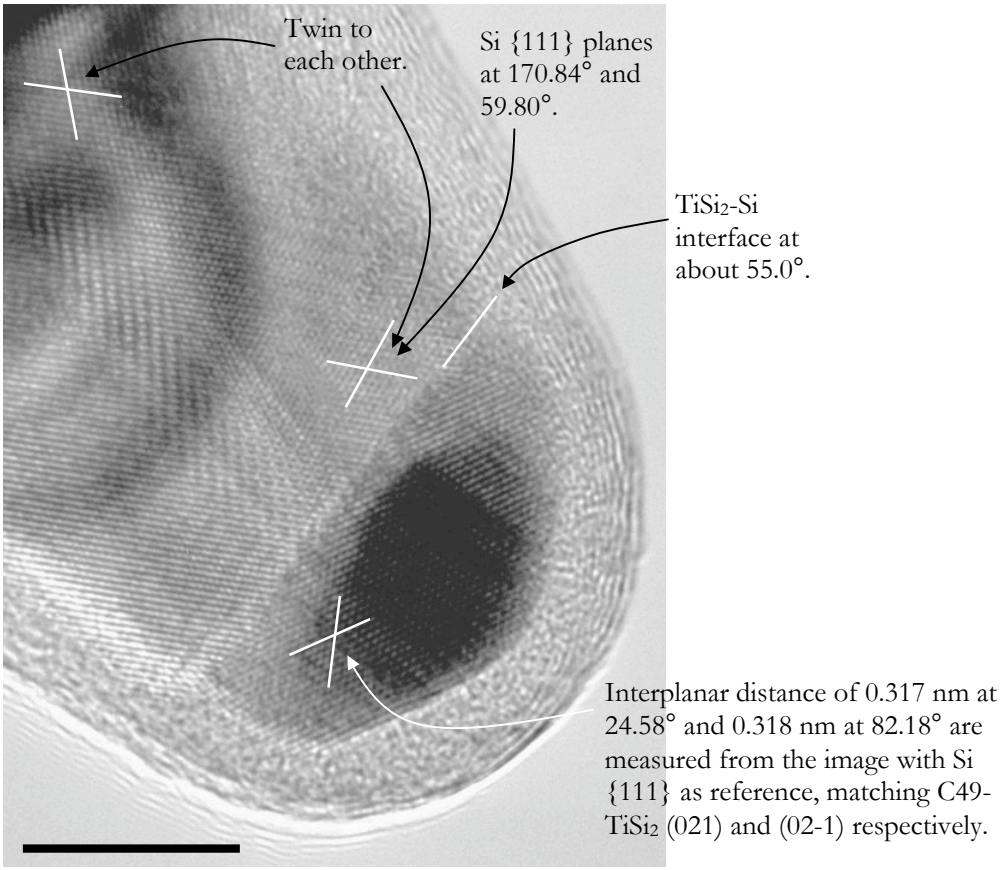


Figure 4-13. TEM Image showing orientation **pp6**. Scale bar 10 nm.

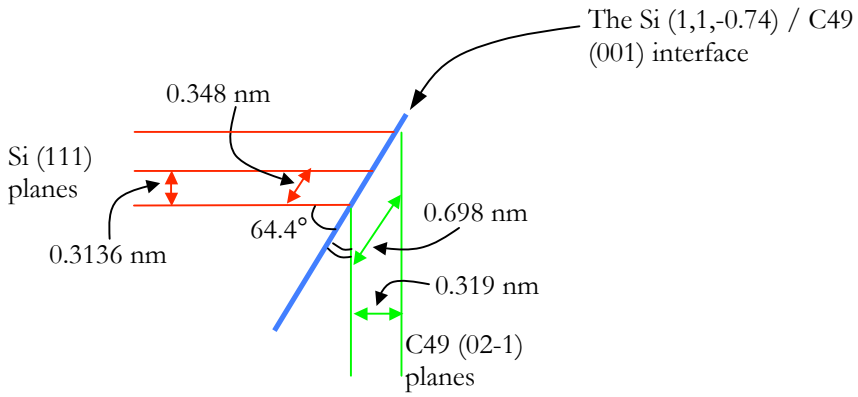


Figure 4-14. Schematics showing relatively good matching between Si {111} and C49 (02-1) at the Si (1,1,-0.74) / C49 (001) interface, corresponding to Fig. 4-13.

Fig. 4-13 shows orientation ***pp6***, where the $TiSi_2$-Si interface is a single plane, approximately Si (1,1,-0.74) / C49 (001). This interface plane also favors the matching between Si (111) and C49 (02-1), because (0.698 nm) / (0.348 nm) ≈ 2, as shown in Fig. 4-14.

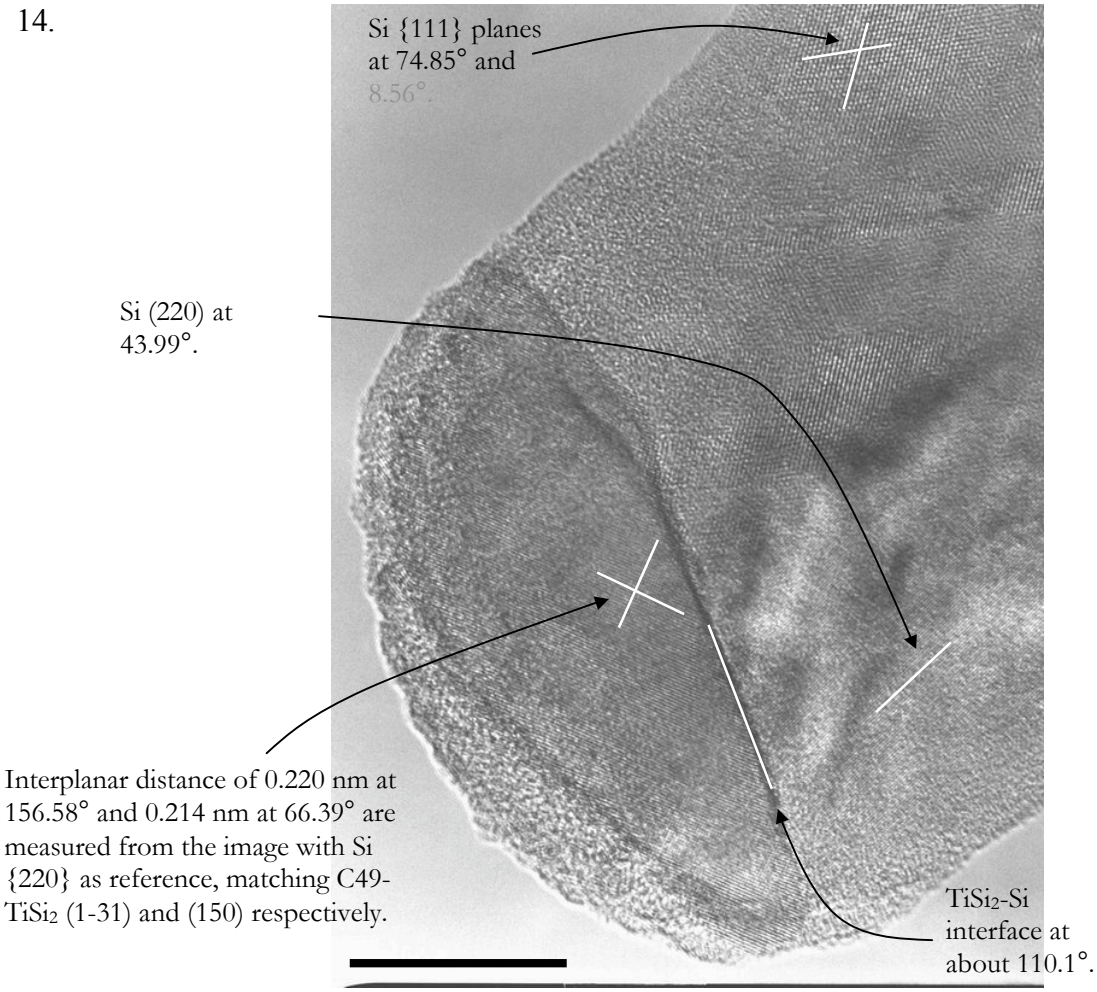


Figure 4-15. Another TEM Image showing interface lattice match. Scale bar 10 nm.

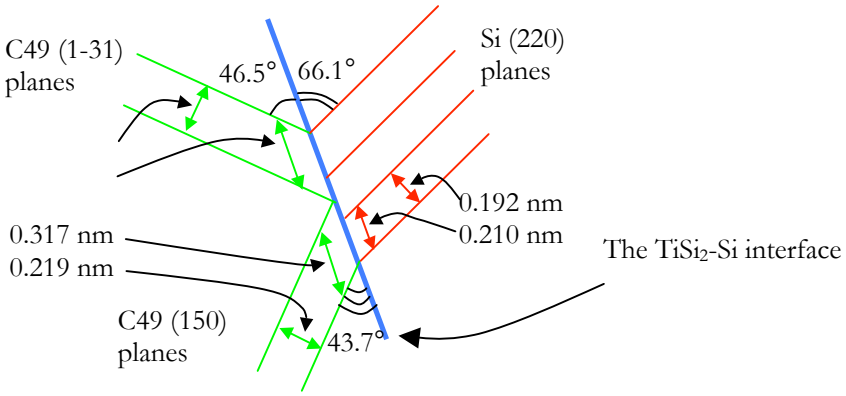


Figure 4-16. Schematics showing the lattice matching in Fig. 4-15.

Another example of the $TiSi_2$-Si interface favoring lattice match is shown in Fig. 4-15, with its schematics shown in Fig. 4-16, where (0.308 nm) / (0.210 nm) ≈ (0.317 nm) / (0.210 nm) ≈ 1.5.

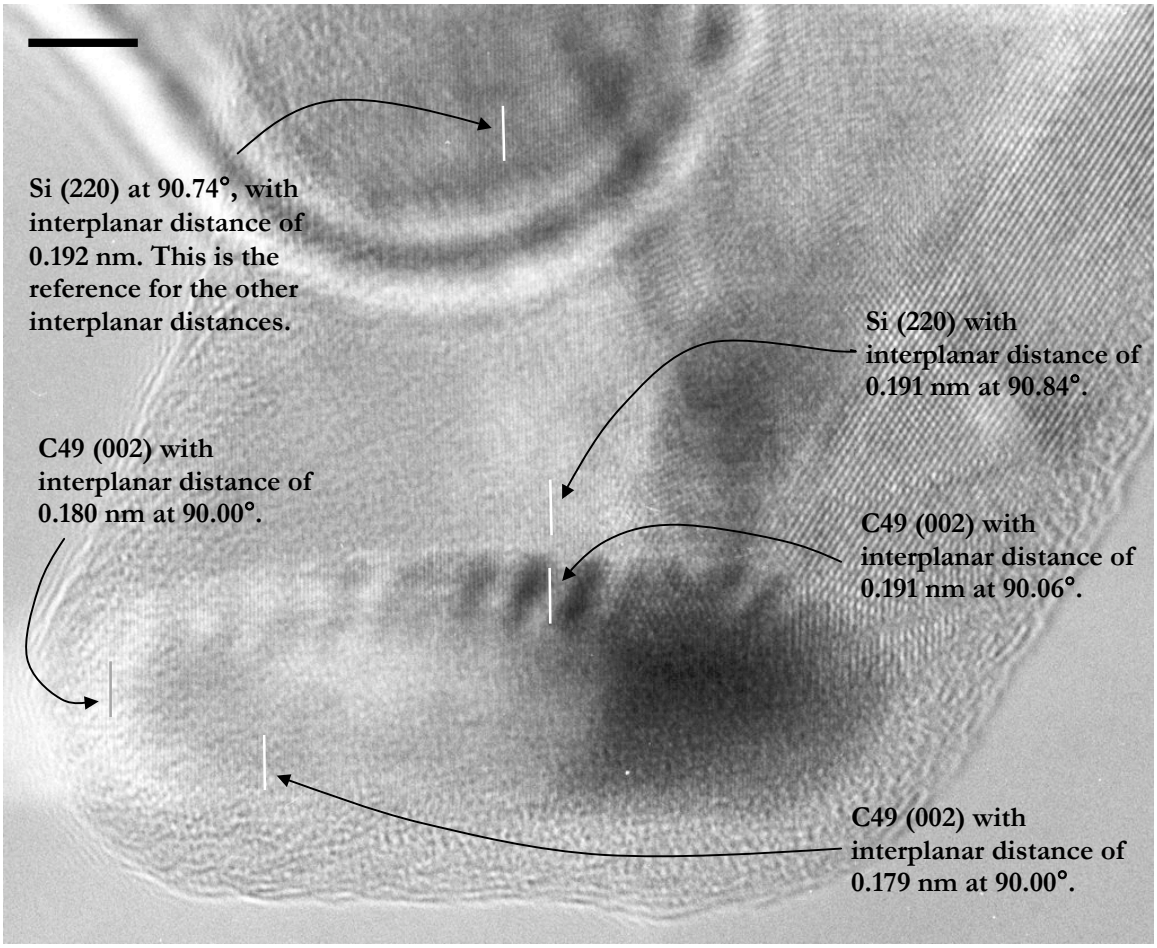


Figure 4-17. TEM image showing different lattice constants for the same set of planes at or away from the $TiSi_2$-Si interface, which is a direct evidence of interface strain.

The frequent appearance of kinking and twinning in the nanowires is attributed to strain at the $TiSi_2$-Si interface. Direct evidence of the interface strain is shown in Fig. 4-17, where the interplanar distance of Si (220) is smaller at the interface, while that of C49 (002) is larger at the interface. Thus, the Si crystal is under compressive stress at the interface and the C49-$TiSi_2$ crystal is under tensile stress. The calculated standard interplanar distance of Si (220) is 0.192 nm and of C49-$TiSi_2$ (002) is 0.180 nm. In the figure, the standard deviation of the interplanar distance measurements is about 0.006nm, which is obtained from 10 independent measurements at each site. For each measurement, the distance between over 20 lattice planes is measured and the average interplanar distance

is taken. The Moiré fringes at the $TiSi_2$-Si interface are due to strain and an angular difference of about 0.8° between the Si (220) and C49 (002) orientations.

$TiSi_2$ islands and Si nanowires on a Si (112) substrate were also studied under TEM. Interestingly, some non-nucleating islands have the orientation ***dd***, the same as the dominant, non-nucleating islands on the Si (001) substrate. But since the substrate surface is changed, the non-nucleating islands on the Si (112) substrate have a different morphology, i.e., no top flat surface, because now the C49 (060) facet is at about 35.3° to the Si (112) wafer surface, as shown in Fig. 4-18. This excludes the hypothesis that the non-nucleating islands do not nucleate nanowires because the Si atoms diffuse along a channel which is within the C49 (010) plane unless the channel is along the C49 (001) or (100) direction.

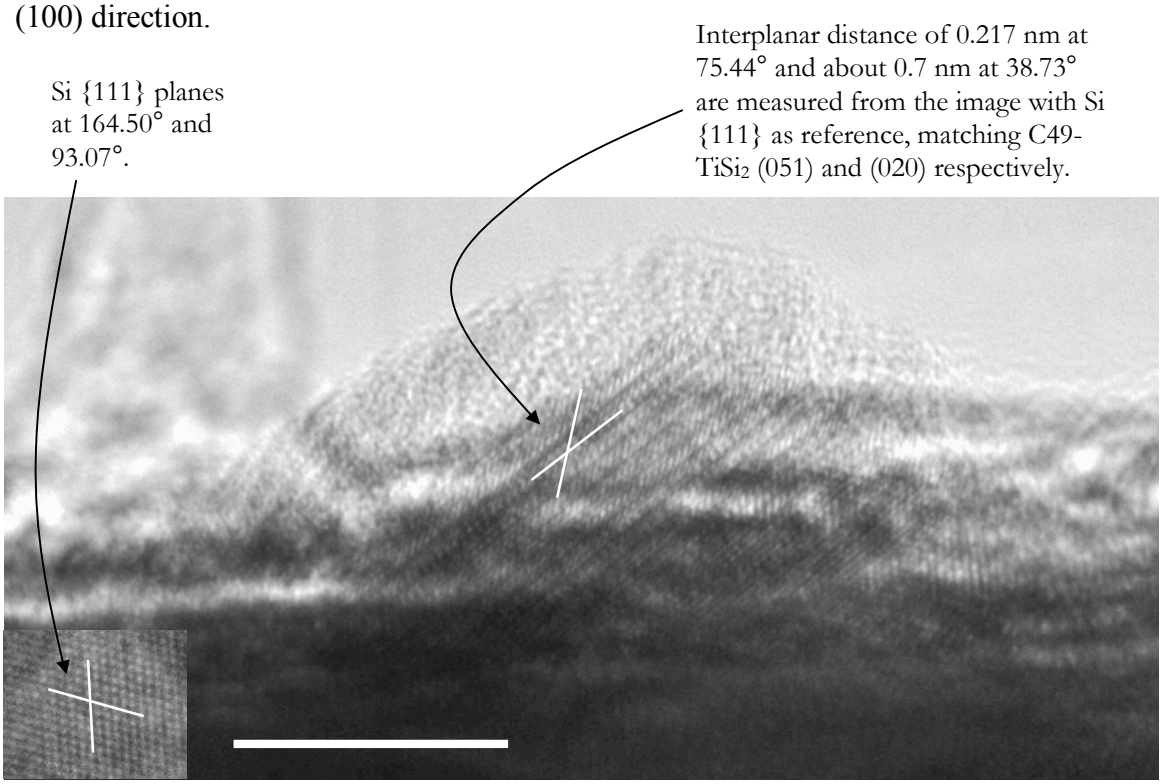


Figure 4-18. TEM image showing non-nucleating island morphology on Si (112) substrate. The inset shows the lattice image of the substrate from lower part of the same big image. Scale bar 10 nm.

Fig. 4-19 shows another non-nucleating C49-TiSi2 island, also with orientation ***dd***. But the imaging direction is slightly off the Si [-110] direction, so we can see that the island is actually elongated along the Si [-110] direction, similar to the behavior observed on Si (001) substrates.

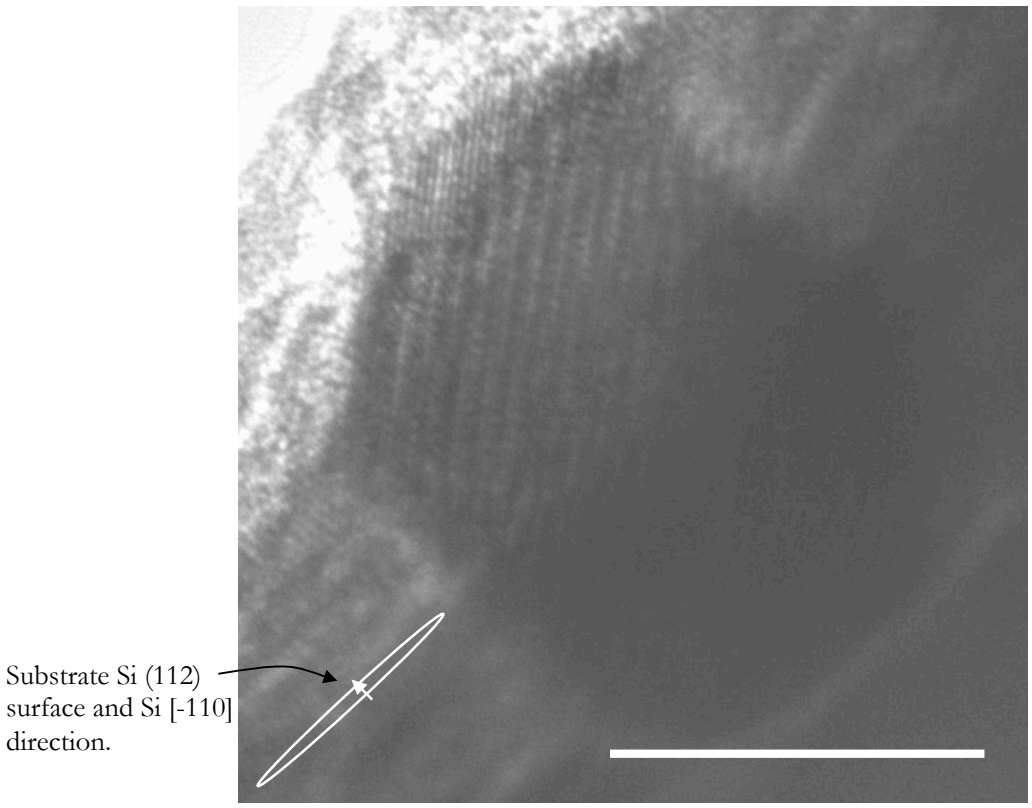


Figure 4-19. TEM image showing an non-nucleating $TiSi_2$ island with orientation **dd** and elongated along the substrate Si [-110] direction. Scale bar 10 nm.

Fig. 4-20 shows a C49-$TiSi_2$ island with an orientation very close to that of orientation ***dd***. There is about 6 nm of Si crystal grown under the island. Fig. 4-21 shows a C49-$TiSi_2$ island with an orientation also close to orientation ***dd*** and with about 40 nm of Si growth under it. The matching between the island orientation and orientation ***dd*** for the islands shown in Fig. 4-18, 4-20, and 4-21, characterized by the angle between C49 (060) and Si (001) planes, is shown in Table 4-2. The Si (001) plane orientation is calculated from Si {111} plane orientations. For the ideal orientation ***dd***, the angle between C49 (060) and Si (001) is 0°. In Fig. 4-18, 4-20, and 4-21, the angles are 0.06°, 0.40°, and 2.33° respectively, while the Si growth height under the island is almost zero, about 6 nm and about 40 nm respectively. We can see that the greater the island angular orientation deviation from orientation ***dd***, the thicker the Si growth under the island. I therefore speculate that the exact orientation ***dd*** has an interface with the Si substrate that causes little Si condensation at the interface. Any slight deviation of the C49 (060) plane from orientation ***dd*** leads to better Si growth under the island. Higher Ti deposition temperature is helpful to achieve this deviation.

Table 4-2. Comparison between the island orientations shown in Fig. 4-18, 4-20, and 4-21.

Figure number	Angle between C49 (060) and Si (001)	Si growth under the island
4-18	0.06°	No growth
4-20	0.40°	About 6 nm
4-21	2.33°	About 40 nm

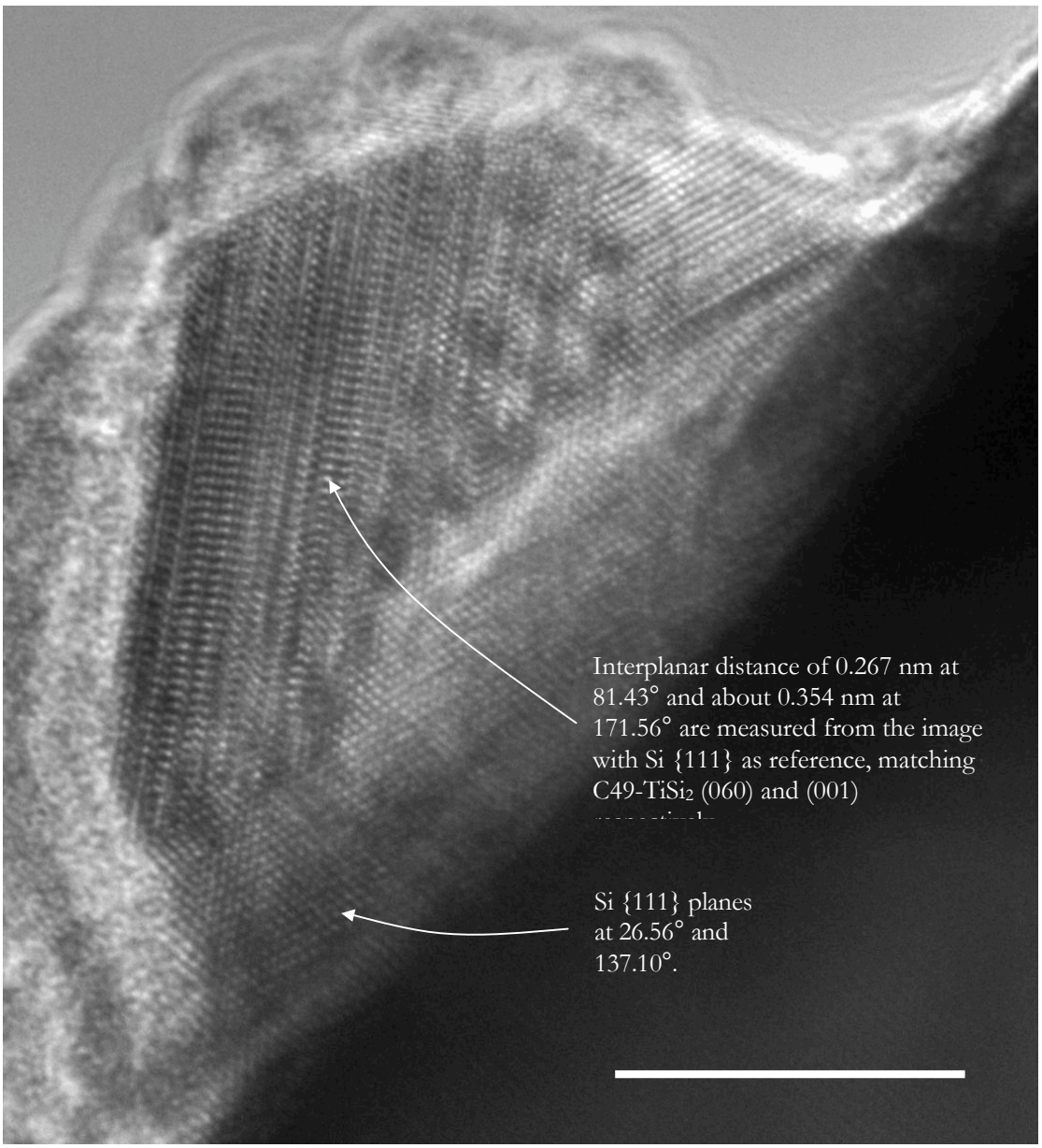


Figure 4-20. TEM image showing a $TiSi_2$ island very close to orientation **dd** and with about 6 nm Si growth under it. Scale bar 10 nm.

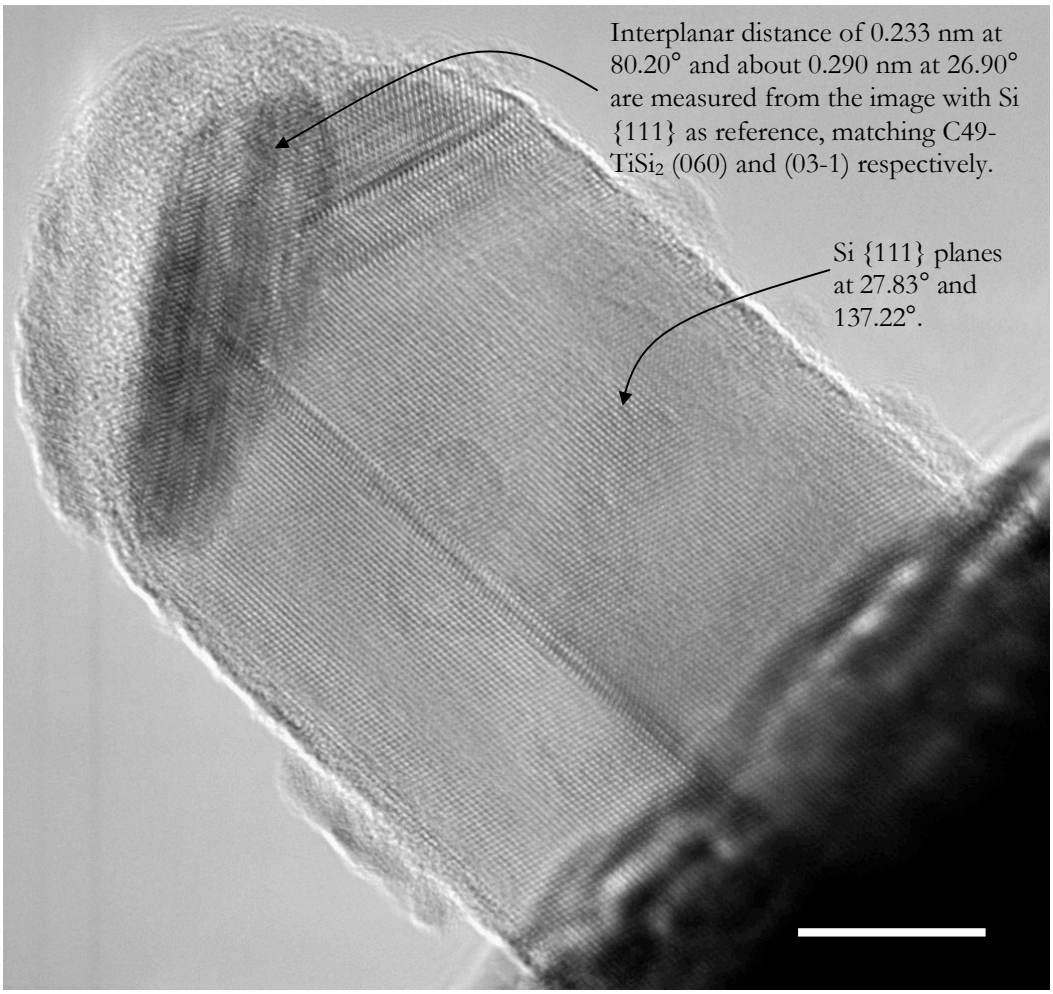


Figure 4-21. TEM image showing a $TiSi_2$ island close to orientation **dd** and with about 40 nm Si growth under it. Scale bar 10 nm.

4.3 Discussion of Growth Mechanism

Several of the previous sections have touched on the growth mechanism of titanium-silicide-nucleated Si nanowires. Combining the above TEM orientation studies with more materials science knowledge, we can establish a more complete understanding of the growth mechanism for Ti-nucleated Si nanowires.

For VLS growth, the various steps were shown in Fig. 1-8. According to Givargizov[18], the rate-limiting step is either step (2): chemical reaction on the vapor-liquid interface[80], or step (4), incorporation of the material in a crystal lattice, or possibly both. With similar arguments, the possible rate-limiting step(s) for $TiSi_2$ nucleated Si nanowire growth by MBE are also either step (2) or (4), or both. In section 3.1.3, we see that the same type of flat-topped islands, presumably with similar orientation and surface, have different growth behavior at similar growth temperatures, if the $TiSi_2$ nucleation

island are deposited at different temperatures. This fact excludes the possibility of step (2) as the rate-limiting step, because if surface reaction is limiting the growth, all the flat-topped islands should have similar growth behavior: either all or none nucleating nanowires, contrary to what is shown in Fig. 3-6. Furthermore, Table 4-2 shows that the greater the angular deviation from the orientation ***dd*,** the greater the silicon growth. In fact, larger deviation would result in less lattice mismatch at the $TiSi_2$-Si interface, as schematically shown in Fig. 4-22. The left two schematics show a flat interface and a 25° askew interface between two sets of perfect aligned crystal planes with interplanar distance of x and 1.2x, while the right two schematics show the same interface after the top crystal plane tilts about 10°. This shows that, for perfectly aligned crystal planes, similar to the case of orientation *dd*, independent of the interface orientation, the lattice mismatch at the interface is always 20%. However, for the 10° misaligned crystal planes, a perfect lattice match can be obtained at the 25° askew interface. My theory is that the increased silicon growth comes from a better $TiSi_2$-Si interface lattice match.

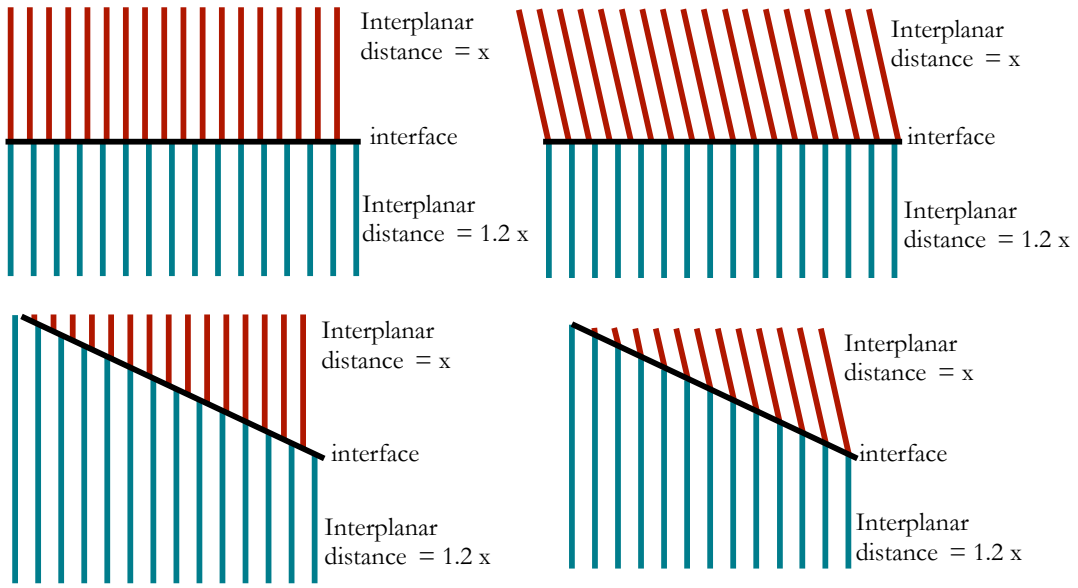


Figure 4-22. Schematic showing better mismatch for the askew interface after deviation from perfect alignment.

The above discussion leads to the question of why a smaller $TiSi_2$-Si interface lattice mismatch leads to increased Si growth. The answer lies in the basic growth kinetics. As we know, the growth rate, R_{growth}, is proportional to the attachment rate, R_{attach}, which in our

case is how fast a Si atom can attach to a growth site - most likely a dangling bond at the $TiSi_2$-Si interface. R_{attach} is governed by the energy barrier and the driving force for this attachment and is proportional to:

$$Exp(\frac{-\Delta G_A}{kT})[Exp(\frac{\Delta G_N}{2kT}) - Exp(\frac{-\Delta G_N}{2kT})] \quad ,$$

where ΔG_A is the energy barrier height and ΔG_N is the driving force, as shown in Fig. 4-22(b). Fig. 4-22(a) is a schematic of the strained $TiSi_2$-Si interface with a misfit dislocation, where the $TiSi_2$ side is under tensile strain and the Si side is under compressive strain, similar to the orientation ***dd*** situation. It also shows two interstitial Si atoms at the interface, one at the misfit dislocation core, the preferred Si interstitial site, and the other one away from the dislocation core. It is believed that Si atoms diffuse rapidly through $TiSi_2$ via the interstitial mechanism[88]. If there is no strain at the interface, then the free energy vs. position should be as illustrated in Fig. 4-22(b), where a positive driving force and a moderate energy barrier enable the Si growth. For the Si atom at the dislocation core, the increased free space around the interstitial atom decreases the free energy, hence will increase the energy barrier height and decrease the driving force or even make the driving force negative, as shown in Fig. 4-22(c), where the dotted line is the replica of the unstrained case, Fig. 4-22(b). Thus the increased free space at the dislocation core will make the attachment rate, and therefore the growth rate, slower or equal zero there. Even if the Si atom is not at the dislocation core, the misfit strain will still decrease the free energy at the $TiSi_2$ side and increase the free energy at the Si side, as shown in Fig. 4-22(d), and this will cause slower growth[89,90]. Thus Si condensation at the $TiSi_2$-Si interface as the rate-limiting step provides an explanation for almost every observed growth behavior.

For the $TiSi_2$ catalyzed Si growth, the possible silicon transport routes are shown in Fig. 4-23, where route (a) denotes diffusion through the solid silicide island, route (b) denotes catalyst island surface diffusion, route (c) denotes diffusion along the $TiSi_2$-Si interface, and route (d) denotes diffusion along the substrate surface. For the non-nucleating islands or small islands with sub-10 nm diameters where surface diffusion may have a non-negligible influence, diffusion through the solid catalyst island might not dominate the Si transport.

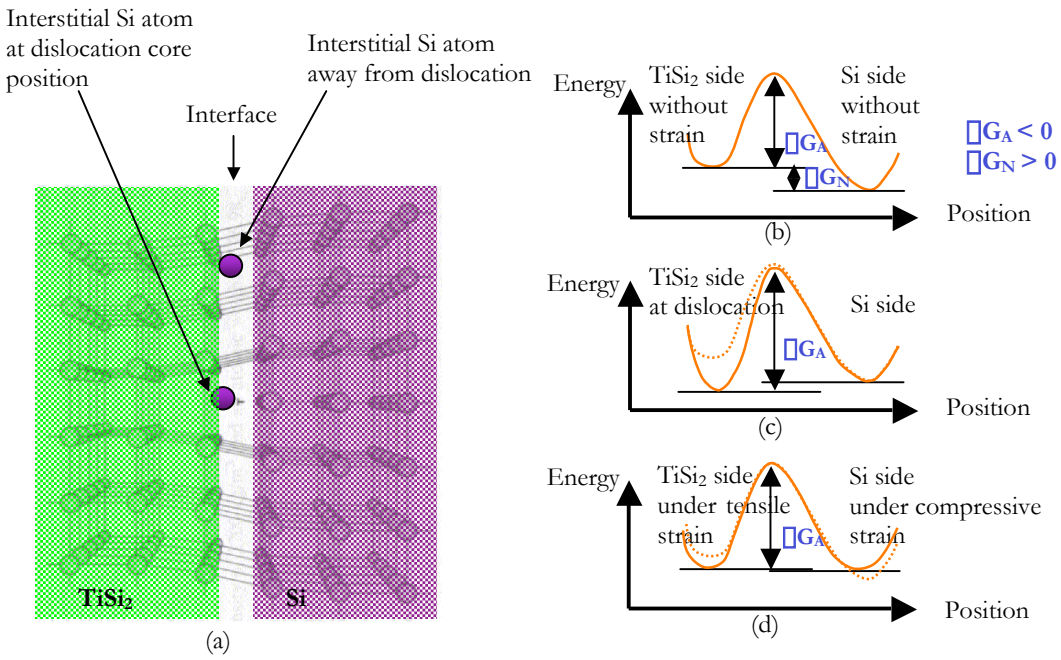


Figure 4-22. Schematic showing different energy barriers and driving forces for different interfaces or locations. In (b) and (c), the dotted curve corresponds to unstrained case.

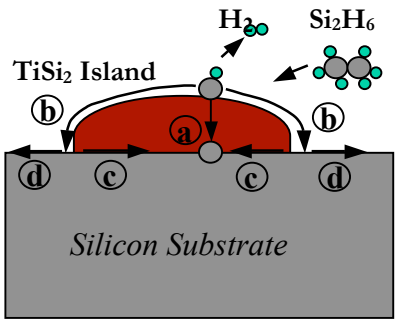


Figure 4-23. Schematic of growth mechanism and silicon transport routes.

For the non-nucleating islands, interface condensation is slow, hence the Si atom concentration in the islands builds up and Si atoms from decomposition of Si_2H_6 diffuse away along the island and substrate surfaces [route (b) and (d)]. Therefore, the $TiSi_2$ islands won't be buried by Si growth, as shown in Fig. 3-6 (a). This is further verified when solid source Si is used for growth instead of Si_2H_6. The growth result is shown in Fig. 4-24. We see a flattop island at the lower-left part of the image, which is not buried, and that the three islands at the right side even start nucleating nanowires. The extra Si atoms for the nanowire growth may come from substrate surface diffusion.

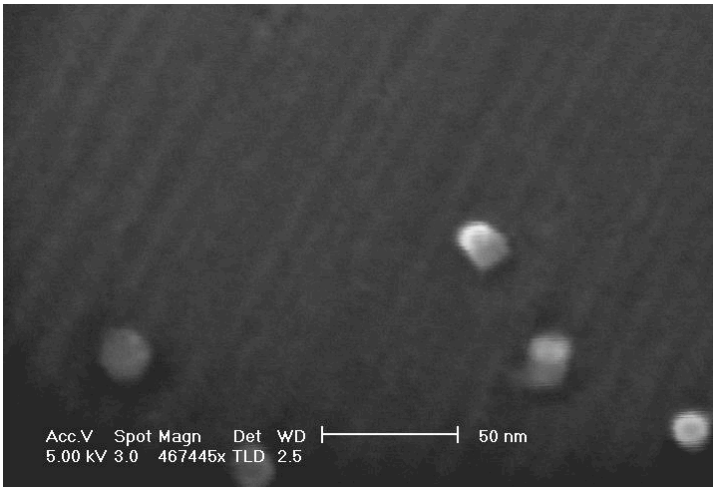


Figure 4-24. SEM image of about 20 nm solid source silicon growth on titanium silicide islands on (112) substrate at 577°C.

Titanium silicide islands smaller than 10 nm have fewer crystalline defects and interface defects per island because of their smaller volume and smaller stress at the interface, especially shear stress. Therefore, they can have a higher interface Si condensation rate and grow faster at higher temperature. Moreover, with the diameter of the islands less than about 20 lattice constants, the diffusion along the island surface and then along the island-Si interface [route (b) and (c)] could be fast enough to contribute to Si atom supersaturation at the interface and therefore contribute to a higher growth rate. At higher Ti deposition temperature, it is easier for the $TiSi_2$ nuclei to slightly tilt and achieve better interface lattice match with the underlying Si substrate, so that even the flat-topped islands grow up. However, the ineffectiveness of annealing shows that if the $TiSi_2$ islands grow larger than 20 nm, temperatures below 900°C can not make them to tilt to have better interfaces.

Chapter 5

Processing and I-V curves of *in situ* p-n Junctions and Gated Structures Made from Si Nanowires

This chapter describes the processing of *in situ* p-n junctions and an *in situ* gated structure made from Si nanowires. Here, *in situ* means the nanowires have not been moved from their original growth locations. The I-V curves of the processed structures show that while the devices are preliminary, making vertical *in situ* MOSFETs from Si nanowires is possible with further improvement.

5.1 Processing of *in situ* p-n Junctions and Gated Structures

p-n junctions, FETs, and even simple logic circuits made of silicon nanowires have been demonstrated[39,40,41]. But the common problem of these demonstrations is that the nanowires were always removed from their original growth locations, after which they were distributed in liquid and then realigned on a substrate. Further processing was then required to produce the device structures. This whole procedure, especially the removal and realignment, is very time-consuming and has very low yield. For large-scale integrated circuits or integrated sensor applications, this process can never meet the industry requirements of low cost and high throughput. Therefore, the only way to use Si nanowires in high integration is to fabricate nanowire devices or process nanowires *in situ*, i.e., without any relocation of the Si nanowires, to allow controlled interconnection of nanowire devices and substrate devices..

The fabrication of *in situ* Si nanowire devices requires good control of the Si nanowire growth. In order to be more compatible with semiconductor processing steps, such as

deposition and photo-lithography, we prefer nanowires that are perpendicular to the substrate surface. Because the preferred growth direction is Si<112>, we grow Si nanowires on Si (112) substrates to get straight nanowires perpendicular to the substrate. As Fig. 5-1 shows, however, that the majority of nanowires remain kinked. Since straight nanowires normally grow taller than kinked ones, we were able to develop a contact process that only contact the long and straight wires in our processed structures.

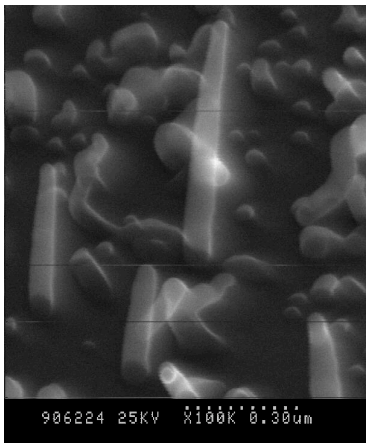


Figure 5-1. Si nanowires grown on Si(112) substrate at 570 °C for 60min with 5 sccm Si_2H_6 flow. SEM image was taken at 45° relative to the substrate surface.

We developed two processes to produce in situ nanowire p-n junctions. The first process is described below, and is illustrated schematically in Fig. 5-2.

Step 1: Grow 100 nm SiO_2 on the substrate. Use standard photolitography techniques to pattern 1.5 μm diameter openings, and etch through the SiO_2 with HF. This will act as a growth mask for the nanowires.

Step 2: Load the wafer into the growth chamber, then deposit Ti on the wafer surface. Then after annealing, Si nanowires are grown with suitable conditions. Normally the $TiSi_x$ islands on SiO_2 surface do not nucleate nanowires.

Step 3: Unload the wafer and remove the SiO_2 layer, together with the $TiSi_x$ islands on top, by dipping in 6:1 buffered oxide etch (BOE).

Step 4: Deposit a layer of 500 nm low temperature oxide (LTO) to conformally cover the nanowires.

Step 5: Polish to achieve a flat top surface and expose the Si core of long Si nanowires by using chemical mechanical polish (CMP). The remaining oxide layer thickness is expected to be 300 nm.

Step 6: Pattern and deposit top metal contact, which is made of a 300 nm Ti layer and a 30 nm Au layer which has an area of 100□m□100□m.

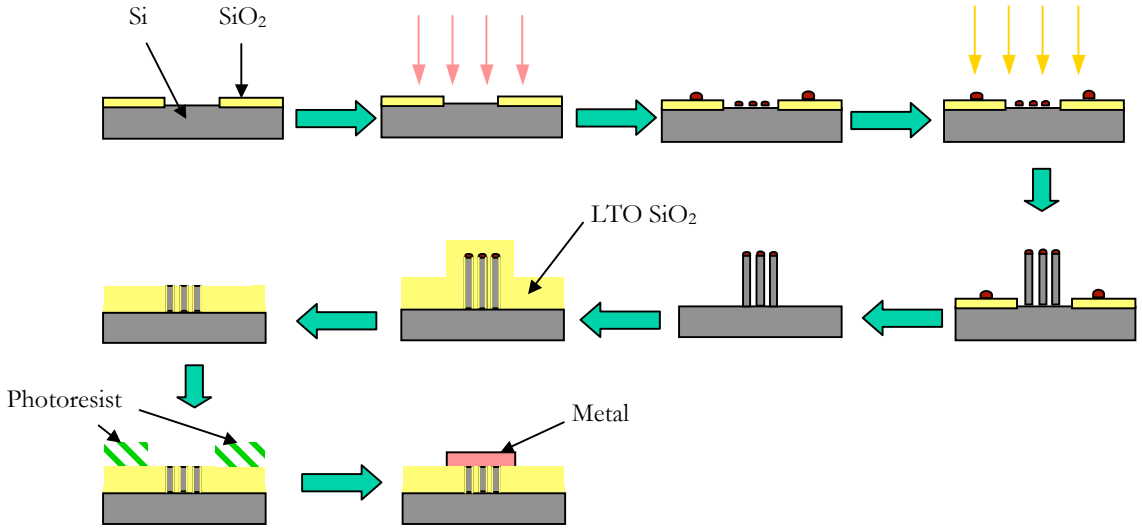


Figure 5-2. Schematic of processing steps to get in situ nanowire p-n junction structure.

We also developed a simpler, alternative process, in which the nanowires are grown without the oxide growth mask. The rest of the steps are the same, only with the oxide layer removal step omitted. But the top metal contact in the first method is only contacting the nanowires in the 1.5um diameter opening, while in the second method it is contacting the nanowires in the 100□m□100□m square opening.

The processing of the gated structures is similar to the above processing of p-n junction structures, but is slightly more complex because an additional metal layer needs to be deposited and patterned as the gate. The procedure is shown in Fig. 5-3. After the oxide growth mask is removed, a layer of gate oxide is grown at 850°C, with a thickness of 3 nm [Si (111) equivalent]. Then a gate layer, for which we use tungsten, is deposited. Tungsten is chosen because of processing considerations: we can selectively etch tungsten in H_2O_2 without etching gate SiO_2, and we can selectively etch LTO SiO_2 in HF without etching the gate tungsten layer when we need to etch through the LTO layer to contact the gate layer,

as shown in the last two steps in Fig. 5-3. Another detail that needs to be mentioned here is that for a gate tungsten layer of 150 nm thick, we first deposit 250 nm, then etch back 100nm isotropically in H_2O_2. This is to remove the sidewall coverage that may short the gate and the top drain contact. With our deposition method of electron-beam evaporation, the tungsten flux arrives at the substrate along line of sight, which results in less deposition on sidewall than on a flat substrate surface if the nanowire is not perpendicular to the substrate surface. For nanowires perpendicular to the substrate surface, there should be no sidewall deposition. This is schematically shown in Fig. 5-4.

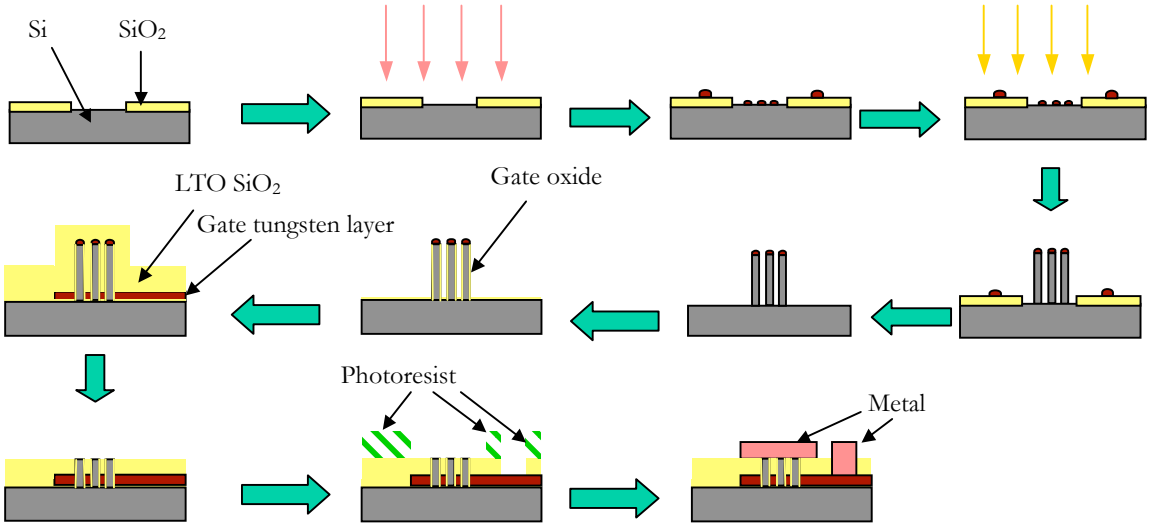


Figure 5-3. Schematic of processing steps to get in situ nanowire gated structure.

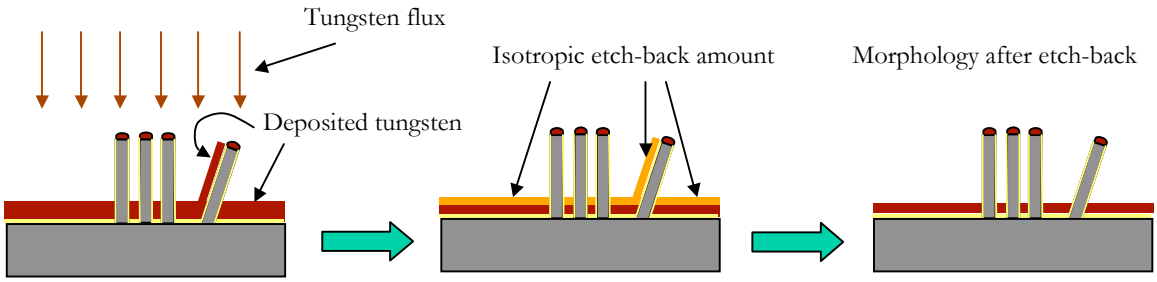


Figure 5-4. Schematic showing the combination of evaporation and etch-back to avoid sidewall coverage.

5.2 Current Measurement Results and Discussion

5.2.1 I-V Curve of *in situ* p-n Junctions

A schematic of a p-n junction made by growing n-type Si nanowires on a p-type Si substrate is shown in Fig. 5-5 and the I-V curve is shown in Fig. 5-6. From the I-V curve between –0.5 V and –0.4 V in Fig. 5-6 (b), it is clear that the slope of the I-V curve is between q/(kT), the slope of the ideal p-n junction, and q/(2kT), the slope of recombination-generation (R-G) dominated p-n junction.

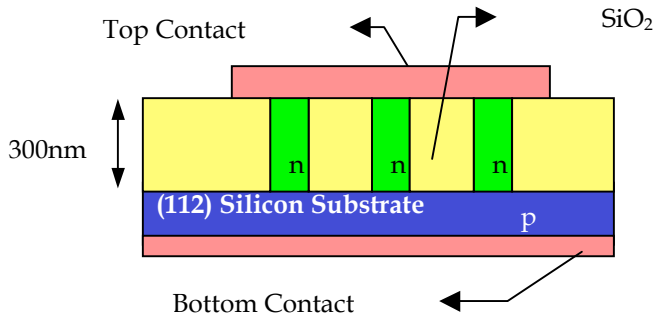
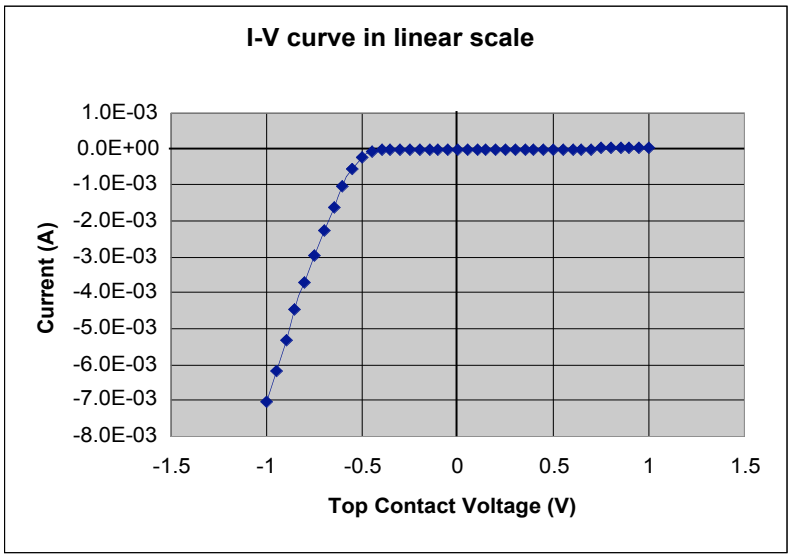
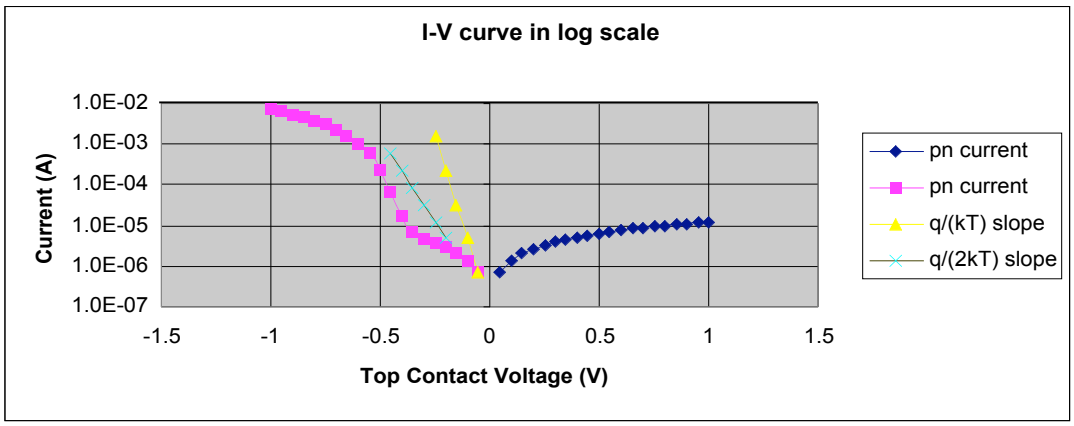


Figure 5-5. Schematic of the p-n junction structure made by n-type Si nanowire and p-type substrate.

If we can identify and extract the series resistive components in the measurement loop which cause the measured slope to deviate from q/(kT), then the p-n junction at the interface between the n-type Si nanowire and p-type Si substrate can then be modeled as a p-n junction with moderate R-G defect density. The R-G defects may be due to crystal defects left from the original $TiSi_2$-Si interface defects, and/or some remaining Ti impurity in the nanowire[81,82,83]. The series resistive components in the measurement loop include the top metal-semiconductor junction resistance, the Si nanowire resistance, and substrate resistance. In Fig. 5-6, the forward current is dominated by series resistive component in the region below –0.5V, which cause the I-V curve slope to be non-exponential with a changing slope. The I-V curve between –0.3 V and 0.3 V in Fig. 5-6 (b) is close to symmetric relative to the y-axis, which is a sign of a parallel resistive leakage path between the top and the bottom contacts. The parallel leakage path may come from the defective LTO and/or nanowire-LTO interface.



(a)



(b)

Figure 5-6. I-V curve of the p-n junction structure shown in Fig. 5-5, (a) on linear scale and (b) on log scale.

In the above measurement, it is unclear whether the top and bottom Si-metal contacts are resistive or more Schottky-contact like. If the top contact is a Schottky-contact and is limiting the current, then the I-V curve should be similar to the case of p^+ nanowire on an n substrate, similar to the I-V curve shown in Fig. 5-10 and clearly different from that shown in Fig. 5-6[84-87]. Therefore the top Si-metal contact is not limiting the current. If the bottom contact is a Schottky-contact and is limiting the current, then the current would show behavior similar to Fig. 5-6. The bottom contact covers the entire 3" wafer backside,

thus it is very unlikely that the bottom contact would limit the current because of the huge area ratio to the nanowires.

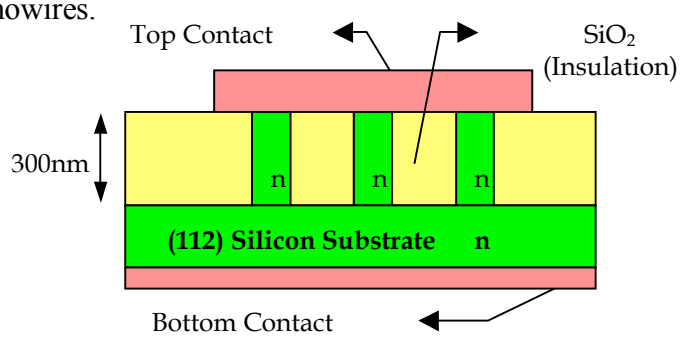


Figure 5-7. Schematic of the n-type nanowire on n-type substrate structure for measuring top metal-Si contact resistance.

To fully eliminate the possibility that the I-V curve Fig. 5-6 is limited by the bottom Si-metal contact, we deposited a small contact area (1.5 □m diameter) structure (the first method mentioned in section 5.1) as shown in Fig. 5-7. This is a n-type Si nanowire on n-type Si substrate structure. The I-V curve of the structure is shown in Fig. 5-8, and shows reasonable resistive behavior, indicating that the bottom contact is not the source of the diode behavior between the bias of -0.4V and -0.5V in Fig. 5-6. The total current in Fig. 5-8 is about 4 orders of magnitude lower than the forward-biased current in Fig. 5-6. This is due to different contact area for the two cases, which results in different number of nanowires. For the small contact area of 1.5 □m diameter, the number of contacted nanowire can be between 1 and 20.

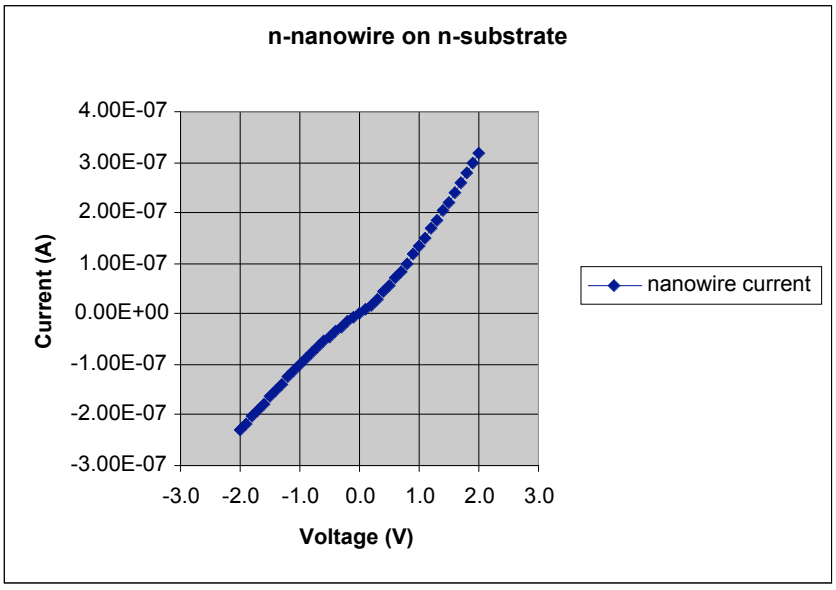


Figure 5-8. I-V curve of the contact test structure shown in Fig. 5-7.

We also fabricated a p-n junction structure made from p-type Si nanowires grown on n-type substrate whose structure is shown in Fig. 5-9. The I-V curve for this structure is shwon in Fig. 5-10. Similar to the n-nanowire on p-substrate structure, the I-V curve in Fig. 5-10 also shows three regions: (1) a R-G or parallel resistive path controlled region ($V < \sim 0.4V$), (2) a band-structure and R-G controlled mid-bias region around 0.5V, and (3) a series resistive component controlled high forward bias region ($V_{bias} > 0.7V$). The high bias region is easily explained. For an ideal p-n junction, $I = I_0 [\exp(qV_{bias}/kT)-1]$, and its resistance, dV_{bias}/dI, quickly drops as V_{bias} increases. Thus, as V_{bias} increases, most of the measurement voltage drops across the other serial resistances. Unlike the n-type nanowire/p-type substrate device, region (2) of the I-V curve of the p-type nanowire/n-type substrate device in Fig. 5-10 is not well defined and has a lower slope than that in Fig. 5-6. This is possibly due to higher top contact resistance, which makes the I-V curve more linear in region (2). Ti has a low workfunction, close to that of n^+ silicon. This results in a lower Schottky barrier height for n-Si/metal contact than for p-Si/metal contact if the Fermi level is not pinned to 1/3 of Si bandgap above valence band, as it is in typical metal contacts to bulk silicon. [84,85]

While the two previous structures featured p-n junctions located at the interface between the nanowire and the substrate, we also fabricated a device with the p-n junction located inside the Si nanowire, as illustrated in Fig. 5-11. The I-V curve for this structure is shown in Fig. 5-12.

The p-n junction inside the Si nanowires is realized by first growing n-type nanowires for 20 min, then switching to p-type doping during subsequent nanowire growth. The I-V curve in Fig. 5-12 shows a less-defined slope in region (2), again possibly also due to higher top contact resistance. The above experiments show that the interface between both n and p-type Si nanowires and Si substrates is clean enough to allow fabrication of reasonable p-n junctions, however, because of the noticeable and similar R-G current components, it appears that background incorporation of Ti in the Si nanowires and/or the strain-induced stacking-faults maybe dominating the I-V characteristics of all these structures.

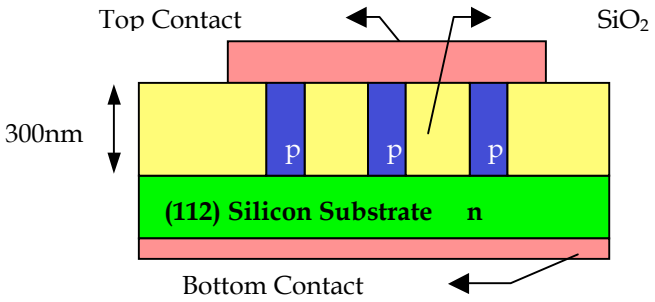
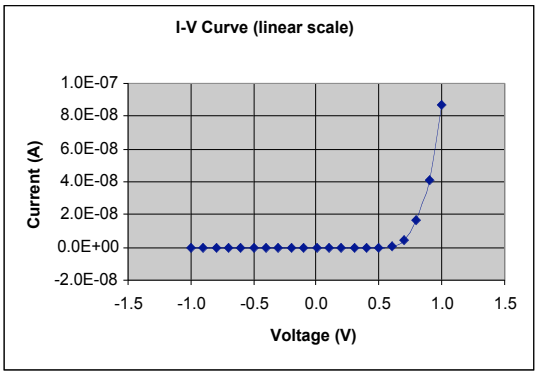
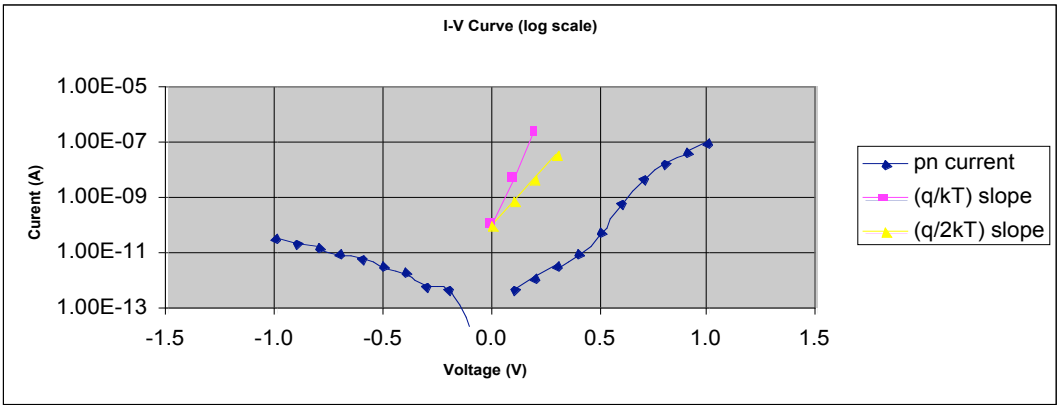


Figure 5-9. Schematic of the p-n junction structure made by p-type Si nanowire and n-type substrate.



(a)



(b)

Figure 5-10. I-V curve of the p-n junction structure shown in Fig. 5-9, (a) on linear scale and (b) on log scale.

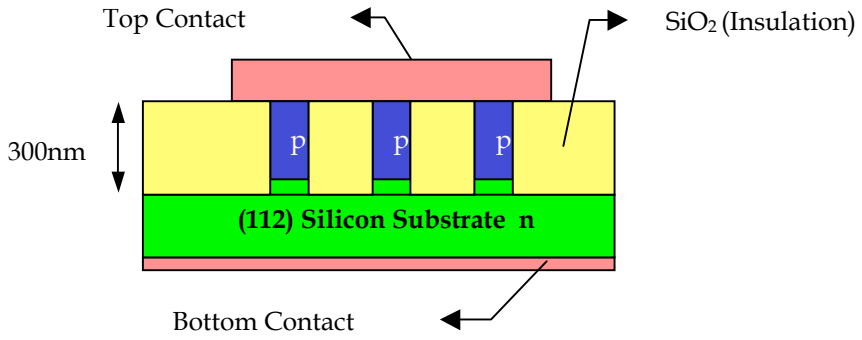
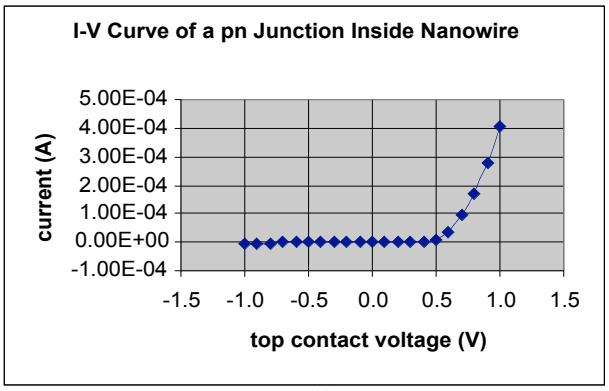
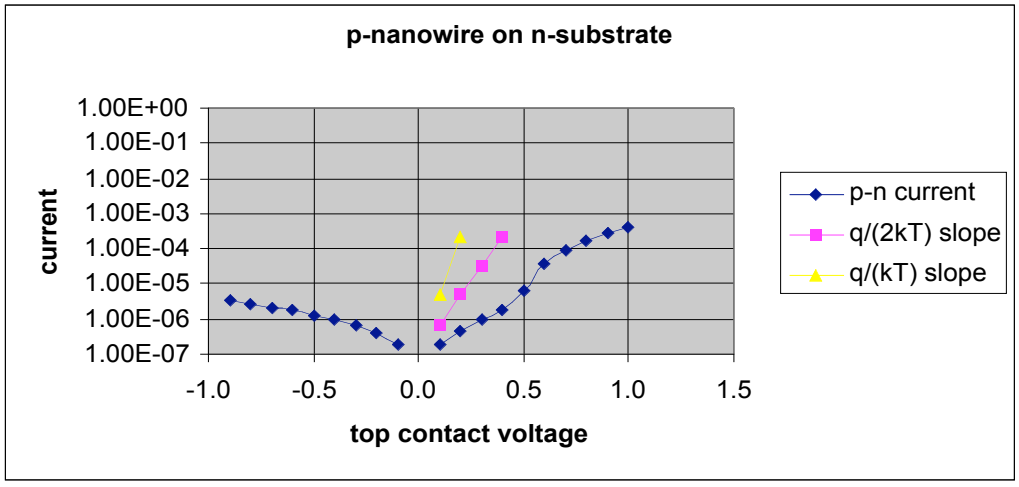


Figure 5-11. Schematic of the p-n junction structure made by growing n-type Si nanowire first and then p-type Si nanowire.



(a)



(b)

Figure 5-12. I-V curve of the p-n junction structure shown in Fig. 5-11, (a) on linear scale and (b) on log scale.

5.2.2 I-V Curve of *in situ* Gated Structures

The p-n junction results established that *in situ* doping with As and B flux during gas-source Si MBE growth can produce good p-n junctions, and that the polishing method can easily enable good contact to the Si nanowires. However, to produce a MOSFET, a controlling gate should be put around the nanowire in the form of a surrounding gate. The structure of a n-type nanowire on n-type substrate with a W controlling gate is shown in Fig. 5-13. The I-V curves for different gate voltages are shown in Fig. 5-14. The gate oxide thickness is calculated to be 3 nm from the oxidation time [calibrated for Si (111) surface].

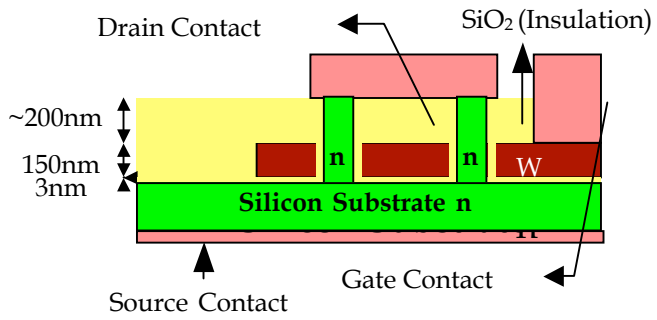


Figure 5-13. Schematic of the gated n-type nanowire on n-type substrate structure.

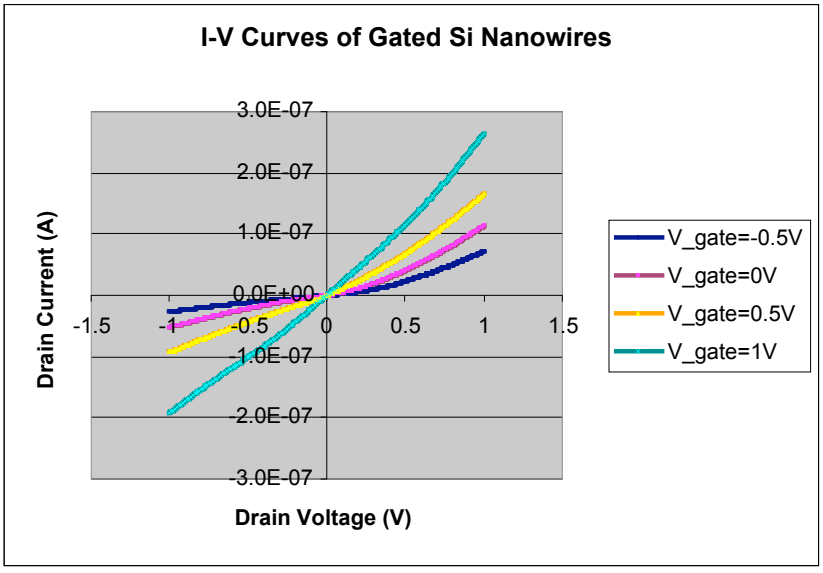


Figure 5-14. I-V curve of the gated structure shown in Fig. 5-13.

The I-V curves in Fig. 5-14 show that when the gate voltage becomes more positive, the drain current becomes larger. This is consistent with the expectation that for n-type Si nanowires, a positive gate voltage will cause surface accumulation and result in higher conductivity. Similarly, it is expected that if the gate voltage become more negative, it will cause depletion of the Si nanowires. If the entire thickness of the nanowires is depleted, then there should be no current going through the structure, except the parallel leakage current. As shown in Fig. 5-14, for V_{gate} = -0.5 V, the current is smaller, but not totally shut off. For Vgate= -1 V, the current still doesn't shut off (which is not shown for simplicity), but becomes very noisy, possibly due to tunneling or hot carrier injection through a weak region in the thin gate oxide or a high electrical field region close to the Si nanowire-substrate interface.

The finite current at negative gate voltages may be a result of incomplete depletion of the nanowire. We can estimate this from the doping and size. For a n-type Si nanowire with an estimated doping density of $5\times10^{18}/cm^3$, the nanowires might not be able to be fully depleted. Because as a close estimation, the maximum depletion depth of a planar gated structure is:

$$d_{\max} = \left(\frac{4\varepsilon_{Si}\varepsilon_0}{qN_d}\psi_P\right)^{\frac{1}{2}}$$

where $\psi_P = \frac{kT}{q}\ln\frac{N_d}{n_i}$ is the bulk potential of the doped silicon, and

ε_{Si} - relative dielectric constant of Si

ε_0 – dielectric constant of vacuum

q – electron charge

N_d – doping concentration

k – Boltzmann constant

T – absolute temperature

n_i – Si intrinsic carrier concentration.

For $N_d = 5\times10^{18}/cm^3$, the maximum depletion depth d_{max} is only 16 nm. After that depth is reached, the extra negative gate voltage will be compensated by the surface inversion charge.

For a given gate voltage, the depletion depth is:

$$d = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} tox\left[\left(1 + \frac{|Vg + Vfb|}{Vd}\right)^{\frac{1}{2}} - 1\right]$$

Where $Vd=(q N_d/2)(\varepsilon_{Si}\, tox^2/\varepsilon_{ox}^2\, \varepsilon_0)$ and

ε_{ox} - relative dielectric constant of SiO_2

tox – oxide thickness

Vfb – flatband voltage, which is about -0.5 V for W gate and n-type Si channel.

For Vg=-0.5 V, the depletion depth *d* is about 9.5 nm, while for Vg =0 V, the depletion depth is about 5.5 nm and for Vg = 0.5 V, it is 0 nm. If we assume the nanowire radius is 20 nm, then the conducting channel has a radius of 10.5 nm at Vg = -0.5 V, 14.5 nm at Vg = 0 V, and 20 nm at Vg = 0.5 V. For Vg = 1 V, the inversion charge can be considered as an extension of about 4 nm to the nanowire radius. So the channel conductance ratio between the four cases would be 1: 1.9:3.6:5.2, roughly matching Fig. 5-14.

Furthermore, any positive defect charges close to the Si surface, which may come from the donor-like deep level trap caused by Ti impurities or crystal defects, will decrease the maximum depletion depth. Therefore, it is possible that the thick Si nanowires in our gated structure could not be fully depleted, which means the gated structure would remain conductive under any gate voltage. A p-doped channel region should be helpful to resolve this problem, but introduces a new challenge in controlling the vertical alignment between the gate and the channel.

With Fig. 5-14, we can also roughly estimate the resistivity of the Si nanowires and subsequently the electron mobility in the Si nanowires. Suppose the number of the contacted Si nanowires in the structure shown in Fig. 5-13 is one. The nanowire has a radius of 20 nm and a length of 400 nm. The estimated surface depletion depth is 5 nm, so

the remaining conducting core of the Si nanowire has a radius of 15 nm. At drain voltage close to 1 V, the influence of the contacts should be very small as expected for any Schottky contact between Si and metal at room temperature. We assume that the Si nanowire is carrying all the current when drain voltage is close to 1 V, and the voltage drop across the Si nanowire equals the voltage applied to the structure. For V_gate = 0 V in Fig. 5-14, the estimated slope at drain voltage equal 1 is 2.0_10^{-7} A/V, which results in a resistance of 5.0_10^{6} Ω. Then according to R=ρL/A, where ρ is resistivity, L and A are the length and cross-section area of the nanowires respectively, the estimated nanowire resistivity ρ is 0.0088 Ω·m. For n-type Si nanowire, the formula for resistivity is ρ=1/(qμn), where q is the electron charge, 1.602_10^{-19} C, μ is the electron mobility, and n is the carrier density, roughly $5×10^{18}/cm^3$. According to the above equation, the electron mobility inside the Si nanowire is 1.4 cm^2/Vs, while the Si bulk electron mobility is about 140 cm^2/Vs, with the dopant concentration of $5×10^{18}/cm^3$. The low mobility in the Si nanowire may be due to a) surface scattering, b) voltage drop over other series resistive components, such as the nanowire-substrate junction where current crowding could happen, c) Stacking faults and dislocations in the Si nanowire resulted from Si-$TiSi_2$ interface strain, and d) Ti incorporation into the Si nanowire during growth.

Chapter 6

Summary

6.1 Conclusions

Si nanowires are grown with C49-$TiSi_2$ as the catalyzing islands in MBE with Si_2H_6 as the gas source. The preferred growth direction is Si <112>. Before the nanowire growth, approximately one monolayer of Ti is deposited and annealed to form the $TiSi_2$ islands. On Si (001) substrates, there are two types of C49-$TiSi_2$ islands, one with flat top surfaces and another with dome-shaped top surfaces. The RHEED observation shows that the flat-topped islands have the orientation of Si(110)//C49-$TiSi_2$(100), Si(1-10)//C49-$TiSi_2$(001), and Si(001)//C49-$TiSi_2$(010), which is called orientation ***dd***, relative the Si substrate. The flat-topped islands tend to elongate along Si[110]//C49-$TiSi_2$[100], which is a better lattice-matched direction than Si[1-10]//C49-$TiSi_2$[001], at high temperatures to decrease the strain energy. The dome-top islands do not have a dominant orientation relative to the substrate, but TEM observation shows that, generally, at the clearly identified interfaces, the projection of the major plane interplanar distances to the interface indicates good lattice-matches between the C49-$TiSi_2$ crystal and the Si crystal at the interface.

Normally only dome-top islands nucleate Si nanowires. A detailed TEM study of the non-nucleating islands on Si(112) substrate shows that more deviation from the orientation ***dd*** leads to more Si crystal growth under the $TiSi_2$ island. This is consistent with the speculation that the lattice mismatch strain and stress for orientation ***dd*** (6% mismatch) prohibits the Si growth. The deviation from orientation ***dd*** leads to less lattice mismatch at the $TiSi_2$–Si interface and therefore leads to more Si growth. The good interface lattice

match between the dome-top $TiSi_2$ islands and Si nanowire crystal underneath them is consistent with this hypothesis.

The lattice strain between C49-$TiSi_2$ crystal and the Si crystal also causes Si twin crystals to form during the nanowire growth. The twin crystals grow larger together with the nanowires, and can change the nanowire growth direction to twinned Si <112>, resulting in kinks in the nanowires. The concurrency of twinning and kinking is observed by TEM.

In situ p-n junctions at the nanowire-substrate interface and inside the Si nanowires were fabricated. The I-V curves of the p-n junctions indicate that the p-n junctions are reasonably good, although a parallel resistive leakage path and R-G current are observable. The gated n-type nanowire on n-type substrate structures show an obvious current modulation effect, which is an indication that a surrounding-gate vertical *in situ* MOSFET made by Si nanowires is possible.

6.2 Future Work

6.2.1 Higher Ti Deposition Temperature

We have observed that higher Ti deposition temperature leads to more Si nanowire nucleation, possibly due to better formation of dome-top $TiSi_2$ islands with good interface lattice match. Unfortunately, our MBE substrate heater can not go above 900°C. So a good way to achieve higher Ti deposition temperature might be to deposit the Ti in an external deposition chamber which is able to handle temperatures above 1000°C. The substrate could then be loaded into the MBE chamber or CVD tube to an0neal in a H_2 atmosphere to reactivate the $TiSi_2$ island surface, which is necessary for catalyzing Si_2H_6 decomposition. Then the normal Si nanowire growth procedure can be followed. High temperature Ti deposition should give straighter nanowires. One thing which needs particular attention is the quantity of Ti deposited, because a high deposition temperature causes more surface diffusion and therefore results in larger, but fewer $TiSi_2$ islands. As described before, because C49-$TiSi_2$ has slightly different a and c lattice constants, larger $TiSi_2$ islands can be elongated and cause an undesired growth shape.

6.2.2 Alloy to Decrease Lattice Mismatch

Since lattice mismatch is the main reason for kinked Si nanowire growth, decreasing the lattice mismatch should lead to better nanowire growth. We prefer using Ti as the catalyzing metal because it has low diffusivity and solubility in Si, but we can add another metal or element to alloy into the $TiSi_2$ island, hoping to give better lattice match. The alloying should be done only after the $TiSi_2$ islands are formed, because with an alloy lattice-matched to Si, small islands can not be obtained by *in situ* annealing since the nucleation driving forces of lattice strain energy and interface energy no longer exist. I have tried alloying Ge, Al, and Ga, but none of these approaches worked.

6.2.3 Improve the Processing of the Gated Structure

A gated p-n-p or n-p-n nanowire would behave more like a MOSFET than the structure shown in Ch. 5, but aligning the gate and the channel doping is a huge processing challenge. Using the nanowire-substrate interface as a junction for n-p-n or p-n-p structures should be helpful for achieving better control of the alignment because it is well-defined and the substrate surface can be used as a reference for processing. Having an extra thick gate layer to guarantee the overlap between the gate and source/drain is feasible but less elegant. A higher fraction of straight Si nanowires and better controlled *in situ* doping will be necessary to achieve better device fabrication and performance.

Bibliography

Bibliography

[1] A. P. Alivisatos, "Semiconductor clusters, nanocrystals, and quantum dots," Science, vol. 271, pp. 933-937, Feb., 1996.

[2] U. Banin and O. Millo, "Tunneling and optical spectroscopy of semiconductor nanocyrstals," Annu. Rev. Phys. Chem., vol. 54, pp. 465-492, Feb., 2003.

[3] L. Pavesi, L. D. Negro, C. Mazzoleni, G. Franzo, and F. Priolo, "Optical gain in silicon nanocrystals," Nature, vol. 408, pp. 440-444, Nov., 2000.

[4] L. Patrone, D. Nelson, V. I. Safarov, M. Sentis, and W. Marine, "Photoluminescence of silicon nanoclusters with reduced size dispersion produced by laser ablation," J. Appl. Phys., vol. 87, no. 8, pp. 3829-3837, Apr., 2000.

[5] R. Wang, G. Zhou, Y. Liu, S. Pan, H. Zhang, D. P. Yu, and Z. Zhang, "Raman spectral study of silicon nanowires: high-order scattering and phonon confinement effects," Phys. Rev. B, vol. 61, no. 24, pp. 16827-16832, June, 2000.

[6] Z. Ding, B. M. Quinn, S. K. Haram, L. E. Pell, B. A. Korgel, and A. J. Bard, "Electrochemistry and electrogenerated chemiluminescence from silicon

nanocrystal quantum dots," Science, vol. 296, no. 5571, pp. 1293-1297, May, 2002.

[7] D. P. Yu, Q. L. Hang, Y. Ding, H. Z. Zhang, Z. G. Bai, J. J. Wang, Y. H. Zou, W. Qian, G. C. Xiong, and S. Q. Feng, "Amorphous silica nanowires: intensive blue light emitters," Appl. Phys. Lett., vol. 73, no. 21, pp. 3076-3078, Nov., 1998.

[8] D. P. Yu, Z. G. Bai, J. J. Wang, Y. H. Zou, W. Qian, J. S. Fu, H. Z. Zhang, Y. Ding, G. C. Xiong, L. P. You, J. Xu, and S. Q. Feng, "Direct evidence of quantum confinement from the size dependence of the photoluminescence of silicon quantum wires," Phys. Rev. B, vol. 59, no. 4, pp. 2498-2501, Jan., 1999.

[9] J. Zi, K. Zhang, and X. Xie, "Microscopic calculations of Raman scattering from acoustic phonons confined in Si nanocrystals," Phys. Rev. B, vol. 58, no. 11, pp. 6712-6715, Sept., 1998.

[10] T. Takagahara and S. Takeda, "Theory of the quantum confinement effect on excitons in quantum dots of indirect-gap materials," Phys. Rev. B, vol. 46, no. 23, pp. 15578-15581, Dec., 1992.

[11] R. S. Wagner and W. C. Ellis, "Vapor-liquid-solid mechanism of single crystal growth," Appl. Phys. Lett., vol. 4, no. 5, pp. 89-90, Mar., 1964.

[12] R. S. Wagner and C. J. Doherty, "Controlled vapor-liquid-solid growth of silicon crystals," J. Electrochem. Soc., vol. 113, no. 12, pp. 1300-1305, Dec., 1966.

[13] R. S. Wagner, "Defects in silicon crystals growth by the VLS technique," J. Appl. Phys., vol. 38, no. 4, pp. 1554-1560, Mar., 1967.

[14] R. S. Wagner and C. J. Doherty, "Mechanism of branching and kinking during VLS crystal growth," J. Electrochem. Soc., vol. 115, no. 1, pp. 93-99, Jan., 1968.

[15] R. S. Wagner, in "Whisker technology," edited by A. P. Levitt, New York: Wiley-interscience, pp. 47-119, 1970.

[16] R. S. Wagner, W. C. Ellis, K. A. Jackson, and S. M. Arnold, "Study of the filamentary growth of silicon crystal from the vapor," J. Appl. Phys., vol. 35, no. 10, pp. 2993-3000, Oct., 1964.

[17] E. I. Givargizov, "Periodic instability in whisker growth," J. Cryst. Growth, vol. 20, pp. 217-226, 1973.

[18] E. I. Givargizov, "Fundamental aspects of VLS growth," J. Cryst. Growth, vol. 31, pp. 20-30, 1975.

[19] D. W. F. James and C. Lewis, "Silicon whisker growth and epitaxy by the vapour-liquid-solid mechanism," Brit. J. Appl. Phys., vol. 8, no. 16, pp. 1089-1094, Aug., 1965.

[20] "Bulletin of alloy phase diagrams," Metals Park, OH: American Society for Metals, 1992.

[21] D. J. Eaglesham, A. E. White, L. C. Feldman, N. Moriya, and D. C. Jacobson, "Equilibrium shape of Si," Phys. Rev. Lett., vol. 70, no. 11, pp. 1643-1646, Mar., 1993.

[22] G. A. Bootsma and H. J. Gassen, "A quantitive study on the growth of silicon whiskers from silane and germanium whiskers from germane," J. Cryst. Growth, vol. 10, pp. 223-**234**, 1971.

[23] J. Westwater, D. P. Gosain, S. Tomiya, and S. Usui, "Growth of silicon nanowires via gold/silane vapor-liquid-solid reaction," J. Vac. Sci. Technol. B, vol. 15, no. 3, pp. 554-557, June, 1997.

[24] M. Yazawa, M. Koguchi, A. Muto, M. Ozawa, and K. Hiruma, "Effect of one monolayer of surface gold atoms on the epitaxial growth of InAs nanowhiskers," Appl. Phys. Lett., vol. 61, no. 17, pp. 2051-2053, Oct., 1992.

[25] H. P. Tang, L. Vescan, and H. Luth, "Equilibrium thermodynamic analysis of the Si-Ge-Cl-H system for atomospheric and low pressure CVD of Si_{1-xGex}," J. Cryst. Growth, vol. 116, pp. 1-14, 1992.

[26] "Handbook of chemistry and physics," edited by R. Weast, Cleveland: Chemical Rubber, 1983.

[27] Alfredo M. Morales and Charles M. Lieber, "A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires," Science, vol. 279, no. January, pp. 208-211, Jan., 1998.

[28] N. Wang, Y. F. Zhang, Y. H. Tang, C. S. Lee, and S. T. Lee, "SiO2-enhanced synthesis of Si nanowires by laser ablation," Appl. Phys. Lett., vol. 73, no. 26, pp. 3902-3904, Dec., 1998.

[29] Y. F. Zhang, Y. H. Tang, N. Wang, D. P. Yu, C. S. Lee, I. Bello, and S. T. Lee, "Silicon nanowires prepared by laser ablation at high temperature," Appl. Phys. Lett., vol. 72, no. 15, pp. 1835-1837, Apr., 1998.

[30] N. Wang, Y. H. Tang, Y. P. Zhang, D. P. Yu, C. S. Lee, I. Bello, and S. T. Lee, "Transmission electron microscopy evidence of the defect structure in Si nanowires synthesized by laser ablation," Chem. Phys. Lett., vol. 283, no. 5-6, pp. 386-372, Feb., 1998.

[31] T. I. Kamins, R. Stanley Williams, Y. Chen, Y.-L. Chang, and Y. A. Chang, "Chemical vapor deposition of Si nanowires nucleated by $TiSi_2$ islands on Si," Appl. Phys. Lett., vol. 76, no. 5, pp. 562-564, Jan., 2000.

[32] T. I. Kamins, R. Stanley Williams, D. P. Basile, T. Hesjedal, and J. S. Harris, "Ti-catalyzed Si nanowires by chemical vapor deposition: Microscopy and growth mechanisms," J. Appl. Phys., vol. 89, no. 2, pp. 1008-1016, Jan., 2001.

[33] T. I. Kamins, R. S. Wagner, T. Hesjedal, and J. S. Harris, "Chemically vapor deposited Si nanowires nucleated by self-assembled Ti islands on patterned and unpatterned Si substrates," Physica E, vol. 13, no. 2-4, pp. 995-998, Mar., 2002.

[34] T. I. Kamins, X. Li, and R. Stanley Williams, "Thermal stability of Ti-catalyzed Si nanowires," Appl. Phys. Lett., vol. 82, no. 2, pp. 263-265, Jan., 2003.

[35] Y Cui, Q. Wei, H. Park, and Charles M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," Science, vol. 293, no. 5533, pp. 1289-1292, Aug., 2001.

[36] N. A. Melosh, A. Boukai, F. Diana, B. Gerardot, A. Badolato, P. M. Petroff, and J. R. Heath, "Ultrihigh-density nanowire lattices and circuits," Science, vol. 300, pp. 112-115, Apr., 2003.

[37] Z. He, J. Xu, M. S. Xu, Z. Xie, I. H. Wilson, X. L. Ma, Q. Li, N. Hung L. S. Wang, C. S. Lee, and S. T. Lee, "Dispersion, refinement, and manipulation of single silicon nanowires," Appl. Phys. Lett., vol. 80, no. 10, pp. 1812-1814, Mar., 2002.

[38] C. Li, D. Zhang, X. Liu, S. Han, T. Tang, J. Han, and C. Zhou, "In2O3 nanowires as chemical sensors," Appl. Phys. Lett., vol. 82, no. 10, pp. 1613-1615, Mar., 2003.

[39] Jae-Young Yu, Sung-Wook Chung, and James R. Heath, "Silicon Nanowires: Preparation, Device Fabrication, and Transport Properties," J. Phys. Chem. B, vol. 2000, no. 104, pp. 11864-11870, Nov., 2000.

[40] Sung-Wook Chung, Jae-Young Yu, and James R. Heath, "Silicon nanowire devices," Appl. Phys. Lett., vol. 76, no. 15, pp. 2068-2070, Apr., 2000.

[41] Y. Huang, X. Duan, Y Cui, L. J. Lauhon, K. Kim, and Charles M. Lieber, "Logic gates and computation from assembled nanowire building blocks," Science, vol. 294, pp. 1313-1317, Nov., 2001.

[42] K. Sawada and M. Futagawa, "Field electron emission device using silicon nano-wires," IEDM Proceedings, Dec., 2002.

[43] Y. Huang, X. Duan, Y Cui, and Charles M. Lieber, "Gallium Nitride Nanowire Nanodevices," Nano Lett., vol. 2, no. 2, pp. 101-104, Jan., 2002.

[44] M. S. Gudiksen, L. J. Lauhon, J. Wang, D. C. Smith, and Charles M. Lieber, "Growth of nanowire superlettice structures for nanoscale photonics and electronics," Nature, vol. 415, pp. 617-620, Feb., 2002.

[45] X. Duan, Y. Huang, Y Cui, J. Wang, and Charles M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," Nature, vol. 409, pp. 66-69, Jan., 2001.

[46] J. C. Johnson, H. Yan, R. D. Schaller, L. H. Haber, R. J. Saykally, and P. Yang, "Single Nanowire Lasers," J. Phys. Chem. B, vol. 105, no. 46, pp. 11387-11390, Nov., 2001.

[47] J. C. Johnson, H. Choi, K. P. Knutsen, R. D. Schaller, P. Yang, and R. J. Saykally, "Single gallium nitride nanowire lasers," Natura Materials, vol. 1, pp. 106-110, Oct., 2002.

[48] X. Duan, Y. Huang, R. Agarwal, and Charles M. Lieber, "Single-nanowire electrically driven lasers," Nature, vol. 421, pp. 241-245, Jan., 2003.

[49] B. Xiang, H. Z. Zhang, G. H. Li, F. H. Yang, F. H. Su, R. M. Wang, J. Xu, G. W. Lu, X. C. Sun, Q. Zhao, and D. P. Yu, "Green-light-emitting ZnSe nanowires fabricated via vapor phase growth," Appl. Phys. Lett., vol. 82, no. 19, pp. 3330-3332, May, 2003.

[50] Klaus Graff, "Metal Impurities in Silicon-Device Fabrication," edited by H. K. V. Lotsch, Herdelberg: Springer, Aug., 1999.

[51] C. P. Parry, S. M. Newstead, R. D. Barlow, P. Augustus, R. A. A. Kubiak, M. G. Dowsett, T. E. Whall, and E. H. C. Parker, "Elemental boron doping behavior in silicon molecular beam epitaxy," Appl. Phys. Lett., vol. 58, no. 5, pp. 481-483, Feb., 1991.

[52] A. Cho, "Film deposition by molecular beam techniques," J. Vac. Sci. Tech., vol. 8, pp. S31-S38, 1971.

[53] A. Cho and J. Arthur, "Molecular beam epitaxy," Prog. Solid-State Chem., vol. 10, pp. 157-192, 1975.

[54] H. Hirayama, M. Hiroi, K. Koyama, T. Tatusmi, and M. Sato, "Gas source silicon molecular beam epitaxy," Mat. Res. Soc. Symp. Proc., vol. 220, pp. 545-556, 1991.

[55] H. Jorke, H. Kibbel, F. Schaffler, and H. J. Herzog, "Low temperature kinetics of Si(100) MBE growth," Thin Solid Films, vol. 183, pp. 307-313, 1989.

[56] Y. Shiraki, "Silicon molecular beam epitaxy," Prog. Crystal Growth Charact., vol. 12, pp. 45-66, 1986.

[57] S. L. Delage, in "Silicon molecular beam epitaxy: capabilities and trends," Academic Press, Inc., pp. 207-254, 1989.

[58] E. C. Larkins and J. S. Harris, in "Molecular beam epitaxy of high-quality GaAs and AlGaAs," edited by R. F. C. Farrow, Park Ridge: Noyes Publications, pp. 115-274, 1995.

[59] J. E. Green, "Atomic-level control during film growth under highly kinetically constrained conditions: H mediation and ultrahigh doping during Si1-xGex gas-source epitaxy," MRS Bulletin, pp. 777 Oct., 2001.

[60] J. E. Johannes and J. G. Ekerdt, "Gas-phase reaction study of disilane pyrolysis: applications to low pressure chemical vapor deposition," J. Electrochem. Soc., vol. 141, no. 8, pp. 2135-2140, Aug., 1994.

[61] H. Wado, T. Shimizu, S. Ogura, M. Ishida, and T. Nakamura, "Selective epitaxial growth of Ge and SiGe using $Si_{2H6\ gas}$ and Ge solid source molecular beam epitaxy," J. Cryst. Growth, vol. **150**, pp. **969-973**, 1995.

[62] "Handbook of semiconductor wafer cleaning technology," edited by W. Kern, New Jersey: Noyes Publications, 1993.

[63] "Handbook of semiconductor silicon technology," edited by W. C. O'Mara, R. B. Herring, and L. P. Hunt, New Jersey: Noyes Publications, pp. 283-284, 1990.

[64] W. R. Flavell, in "Surface structures determination by interference techniques," edited by J. C. Vickerman, West Sussex: John Wiley & Sons Ltd., pp. 313-393, 1997.

[65] W. Braun, "Applied RHEED - reflection high-energy electron diffraction during crystal growth," Berlin Heidelberg: Springer-Verlag, 1999.

[66] J. S. Byun, S. J. Choi, J. J. Kim, J. Choi, J. Swenberg, and R. Achutharaman, "Selective titanium silicide deposition using SiH4-TiCl4-H2 in low pressure

chemical vapor deposition and film characterization," J. Electrochem. Soc., vol. 145, no. 11, pp. 3941-3950, Nov., 1998.

[67] J. Wollschlager, "Substrate-step-induced effects on the growth of CaF2 on Si (111)," Appl. Phys. A, Mater. Sci. Process. (Germany), vol. A75, no. 1, pp. 155-166, July, 2002.

[68] U. Hessinger, M. Leskovar, and M. A. Olmstead, "Role of step and terrace nucleation in heteroepitaxial growth morphology: growth kinetics of CaF2/Si(111)," Phys. Rev. Lett., vol. 75, no. 12, pp. 2380-2383, Sept., 1995.

[69] "Phase transformations in materials," edited by G. Kostorz, Bebunden: Wiley-Vch, 2001.

[70] T. H. McDaniels, J. A. Venables, and P. A. Bennett, "Island nucleation in a reactive two-component system," Phys. Rev. Lett., vol. 87, no. 17, pp. 1761051-1761054, Oct., 2001.

[71] S. M. Lee, E. T. Ada, H. Lee, J. Kulik, and J. W. Rabalais, "Growth of Ti and $TiSi_2$ films on Si(111) by low energy Ti+ beam deposition," Surf. Sci., vol. 453, no. 1-3, pp. 159-170, May, 2000.

[72] Y. Chen, D. A. A. Ohlberg, and R. Stanley Williams, "Nanowires of four epitaxial hexagonal silicides grown on Si(001)," J. Appl. Phys., vol. 91, no. 5, pp. 3213-3218, Mar., 2002.

[73] M. Stevens, Z. He, D. J. Smith, and P. A. Bennett, "Structure and orientation of epitaxial titanium silicide nanowires determined by electron microdiffraction," J. Appl. Phys., vol. 93, no. 9, pp. 5670-5674, May, 2003.

[74] T. Y. Tan, S. T. Lee, and U. Gosele, "A model for growth directional features in silicon nanowires," Appl. Phys. A, vol. 74, pp. 423-432, 2002.

[75] E. I. Givargizov, "Ultrasharp tips for field emission applications prepared by the vapor-liquid-solid growth technique," J. Vac. Sci. Technol. B, vol. 11, pp. 449 1993.

[76] J. J. Rousseau, "Basic crystallography," West Sussex, England: John Wiley & Sons Ltd., pp. 19-21, 1998.

[77] G. A. D. Briggs, D. P. Basile, G. Medeiros-Ribeiro, T. I. Kamins, D. A. A. Ohlberg, and R. Stanley Williams, "The incommensurate nature of epitaxial titanium disilicide islands on Si(001)," Surf. Sci., vol. 2000, no. 457, pp. 147-156, 2000.

[78] P. A. Bennett, B. Ashcroft, Z. He, and R. M. Tromp, "Growth dynamics of titanium silicide nanowires observed with low-energy electron microscopy," J. Vac. Sci. Technol. B, vol. 20, no. 6, pp. 2500-2504, Dec., 2002.

[79] J. M. Cowley, N. Ooi, and R. E. Dunin-Borkowski, "Moire patterns in electron microscopy with atomic focuser crystals," Acta Cryst., vol. A55, pp. 533-542, 1999.

[80] S. M. Gates and S. K. Kulkarni, "Kinetics of surface reactions in very low-pressure chemical vapor deposition of Si from SiH_4," Appl. Phys. Lett., vol. **58**, no. **25**, pp. **2963-2965**, June, 1991.

[81] F. Gaiseanu, M. Schelarie D. Sachelarie, and J. Esteve, "Analytical modeling of the gold diffusion induced modification of the forward current through p-n silicon junctions," Diffusion and Defect Data Part B, vol. 57-58, pp. 525-529, 1997.

[82] G. Zavodinsky and I. A. Kuyanov, "Local-density approximation study of p-Si/n-Si nanoscale junctions," Superlattices and Microstructures, vol. 20, no. 2, pp. 187-192, 1996.

[83] F. M. Ross, R. Hull, D. Bahnck, J. C. Bean, L. J. Peticolas, and C. A. King, "Changes in electrical device characteristics during the in situ formation of dislocations," Appl. Phys. Lett., vol. 62, no. 12, pp. 1426-1428, Mar., 1993.

[84] W. Cabanski and M. Schulz, "Tunneling anamoly in disordered metal silicide-silicon junctions," Appl. Phys. A, vol. A50, no. 6, pp. 541-544, June, 1990.

[85] A. Poyai, E. Simoen, C. Claeys, A. Czerwinski, and E. Gaubas, "Improved extraction of the activation energy of the leakage current in silicon p-n junction diodes," Appl. Phys. Lett., vol. 78, no. 14, pp. 1997-1999, Apr., 2001.

[86] R. F. Pierret, "Semiconductor device fundamentals," Addison-Wesley Pub Co., Mar., 1996.

[87] S. M. Sze, "Physics of semiconductor devices," John Wiley & Sons, Inc., 2003.

[88] M. A. Nicolet and S. S. Lau, in “Materials and Process Characterization,” edited by N. G. Einspruch and G. B. Larrabee, New York: Academic, 1983.

[89] P. G. Shewmon, “Diffusion in Solid,” 2nd ed., Warrendale, PA: The Metallurgical Society, 1989.

[90] H. F. Hsu, L. J. Chen, and J. J. Chu, “Epitaxial growth of $CoSi_2$ on (111)Si inside miniature-size oxide openings by rapid thermal annealing,” J. Appl. Phys., vol. 69, no.8, pp.4282-5, Apr. 1991.