COMPLEMENTARY MODULATION-DOPED FIELD-EFFECT TRANSISTOR

A DISSERTATION

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DOCTOR OF PHILOSOPHY

By

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Abstract

A Modulation-Doped Field-Effect Transistor(MODFET) has demonstrated ultra-high speed digital circuit performance. However, in enhancement/depletion (E/D) circuit configuration, their low noise margin, together with low operational voltage which is limited by leakage current through the Schottky gate, place constraints on the practical design of E/D digital MODFET circuits.

Complementary MODFETs (C-MODFETs), the GaAs analogue of CMOS, have advantages of high noise margin, and low power dissipation while maintaining the high speed characteristics of the MODFET structure. SPICE simulation confirmed these features of C-MODFETs. We have developed a fabrication process for C-MODFETs by Selective Molecular Beam Epitaxy. The initial experimental results demonstrated the predicted high noise margin and low power dissipation, however, the relatively slow switching speed suggested a need for improvements. These improvements include: (i) enhancement of the p-channel drain current capability, (ii) elimination of the current collapse due to deep donors ("DX" center) in n-channel MODFETs at cryogenic temperatures and (iii) scaling down the gate length to 1μm, which would substantially enhance the p-channel MODFETs in which the velocity of holes was still in the non-saturated regime.

Various new p-MODFET structures, such as; double heterojunction p-MODFET, strained single quantum well p-MODFET, delta-doped channel p-MODFET and double heterojunction p-MODFET were all investigated. The double heterojunction p-MODFET showed the highest potential drain current and transconductance at cryogenic temperatures, while the delta-doped channel p-MODFET showed the best transconductance at room temperature. Improved complementary MODFET circuits consisting of pseudomorphic (AlGaAs/InGaAs/GaAs) n-MODFETs and double heterojunction p-MODFETs for low temperature application, and complementary MODFET circuits consisting of pseudomorphic n-MODFETs and delta-doped channel p-MODFET for room temperature application were both developed and investigated. A 17 stage ring oscillator operated at 77°K demonstrated the smallest propagation delay among all complementary FET circuits and the smallest power-delay product among all semiconductor integrated circuits.

Acknowledgment

I wish to thank my advisor Professor James S. Harris, and express my gratitude for his support, interest, guidance, and above all patience during the course of this work. I particularly appreciate his willingness to allow me to pursue my research directions in my own way, while providing many opportunities to meet people whose suggestions were sometimes crucial in completing my work. I would also like to express my thanks to Professors James Plummer, Butrus Khuri-Yakub, Robert Dutton, and Richard Swanson for their useful discussions. Profesors Harris, Plummer and Khuri-Yakub's careful reading of this manuscript is gratefully acknowledged.

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Finally, I would like to thank my friends, my parents and my wife Mihoko. Their love and support have been invaluable.

Dedication

To Mihoko, Kentaro and Mariko.

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GLOSSARY

C-MODFET	Complementary Modulation-Doped Field-Effect Transistor
DLTS	Deep-Level Transient Spectroscopy
ECL	Emitter-Coupled Logic
FET	Field-Effect Transistor
HEMT	High Electron Mobility Transistor
LEC	Liquid-Encapsulated Czochralski
LPE	Liquid-Phase Epitaxy
MBE	Molecular Beam Epitaxy
MESFET	Metal-Semiconductor FET
MISFET	Metal-Insulator Semiconductor FET
MOCVD	Metal-Organic Chemical Vapor Deposition
MODFET	Modulation-Doped Field-Effect Transistor
MOS	Metal-Oxide Semiconductor
n-MODFET	n-channel Modulation-Doped Field-Effect Transistor
PECVD	Plasma-Enhanced Chemical Vapor Deposition
p-MODFET	p-channel Modulation-Doped Field-Effect Transistor
RHEED	Reflection High Energy Electron Diffraction
SEM	Scanning Electron Microscope
SIMS	Secondary Ion Mass Spectroscopy
SSQW	Strained Single Quantum Well

Chapter 1

INTRODUCTION

1.1 BACKGROUND

Just as the study of surface leakage current in bipolar devices opened up the way to the MOS structure[MOLL 59], a Modulation-Doped Field-Effect Transistor (MODFET) was invented through the study of an AlGaAs/GaAs superlattice[DINGLE 78] in 1978. Dingle observed an extremely high electron mobility in the lateral direction in his modulation-doped superlattice structure shown in Figure 1.1. It did not take long until this structure was applied to field-effect transistors and extremely high switching speeds were reported [HIYAMIZU 80], [DELAGEBEAUDEUF 80]. Intensive work on MODFET(HEMT) circuits began at that time and this has led toward a successively higher integration, e.g., a 4-Kbit Static RAM [KURODA 86]. However, it is still not clear if MODFETs will dominate in high speed digital logic applications for several reasons: first, GaAs MESFETs are almost as fast as MODFETs in logic speed and they have a simpler

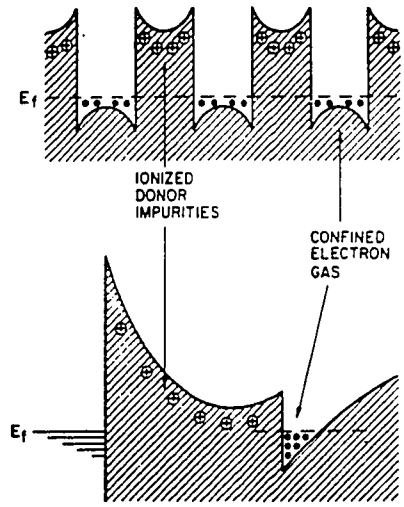


Figure 1.1 Modulation doping for a super lattice (top) and a heterostructure with an attached Schottky junction (bottom). After L.Esaki [ESAKI 83].

fabrication processes; second, the operation of compound semiconductor field-effect transistors (including MODFETs and MESFETs) are limited to low voltage by the Schottky gate leakage current, which results in low noise margins and a lack of design flexibility as long as enhancement / depletion (E/D) type circuits(or DCFL) are used.

1.2 MOTIVATION

The advantages of complementary circuits seem to solve these problems of E/D type GaAs circuits. Although low power dissipation is the basic advantage of complementary FETs for Si MOS applications, the advantages of larger noise margin and full-swing logic levels become the major advantages in the case of compound semiconductor FETs which must operate at low voltages. These advantages further increase process tolerance and design flexibility as well. There is, of course, an anticipated disadvantage for complementary semiconductor circuits. Gallium arsenide and related semiconductors have a large ratio of electron to hole mobility. This low hole mobility leads to a propagation speed disadvantage by a certain factor compared with E/D type circuits. This will be described in chapter 2. However, as we have seen in the history of silicon IC's where CMOS has replaced NMOS, overcoming greater process complexity and larger unit cell size, the disadvantages of new technologies may be overcome without serious problems as long as the advantages play a critical role in the new technological generation. In that regard, we are convinced that we have enough motivations to develop complementary MODFETs to demonstrate their advantages and to suggest approaches to overcome their current disadvantages.

1.3 OBJECTIVES

The first objective of this thesis was to evaluate the advantages and disadvantages of complementary MODFETs by computer simulation. This may appear to be analogous to the (silicon)MOS case, but the outcomes are certainly not obvious because of the peculiarities of (GaAs)MODFETs: (i) large mobility ratio ($\approx$15) between electrons and holes, (ii) low voltage operation, near one volt, necessitated by the maximum forward voltage on Schottky gates. The second and major objective was to demonstrate a circuit technology with high speed, low power dissipation and high noise margins by fabricating complementary MODFET circuits. Since our project started in 1984, several attempts have been reported to make complementary circuits in different versions of the heterojunction FET family, e.g. MISFET, however, they fail to show the highest potential of

complementary heterojunction FETs because the structures do not provide full advantage of their potential as will be explained in detail in chapter 3. In order to accomplish the second objective,which was the major objective of this thesis, fabrication processes needed to be established, starting from scratch. The final objective was to investigate the potential performance of complementary MODFETs in comparison with existing technologies using comparable lithographical dimensions.

1.4 MATERIALS CHOICES

Molecular beam epitaxy (MBE) technology with GaAs based materials provides a number of potential materials choices to accomplish our target structures. Figure 1.2 [TIEN 82] shows the energy gap versus lattice constant for most III-V compounds. The boundaries joining the binary compounds give the ternary alloy energy gap and lattice constant. In order to attain the high quality layers required for FET device fabrication, the heterostructure needs to be reasonably well lattice-matched, within the limit of the critical thickness[MATHEWS 76] of the layers which accomodate the strain without generating dislocations. The GaAs-$Al_xGa_{1-x}As$ system is the most familier combination based upon GaAs substrates. This system has only 0.04% maximum lattice mismatch which occurs when x equals unity(AlAs).

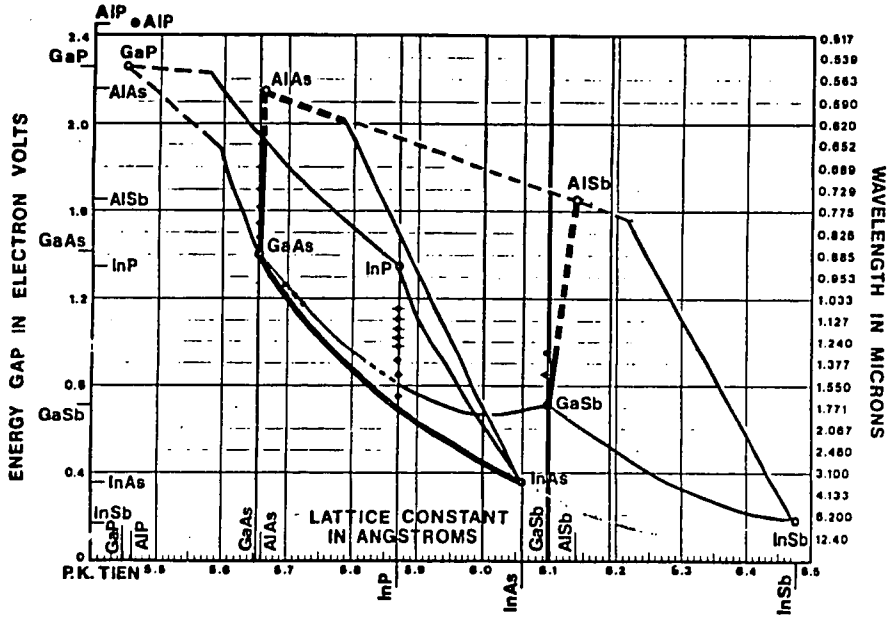


Figure 1.2 Energy-gap and lattice constant of various compound semiconductores. After P.K.Tien [TIEN 82].

In addition to the freedom of aluminum mole fraction choice, this system is compatible with InGaAs. The InGaAs alloy gives additional freedom to the materials combinations in the heterostructures, although the mole fraction of indium must be limited to be 10-20% , depending on the thickness of the strained layer. Germanium, lattice-matched to GaAs, adds one more variety to the AlGaAs-GaAs(InGaAs) system[ARAI 85]. Thus, the AlGaAs-GaAs based system has the largest variety of materials choice, which is advantageous for the challenge of making novel structures. This system was our choice for this complementary MODFET study. Another well-studied and promising heterostructure system, is the AlInGaAs-InGaAs system which is lattice-matched to InP substrate. This system is useful for n-channel MODFETs[HIYAMIZU 86] and resonant tunneling devices[INATA 86] because it gives a much higher conduction-band discontinuity and a larger energy separation between Γ valley and L valley than the GaAs based alloys.

1.5 OUTLINE OF THE PRESENT THESIS

Chapter 2 describes the computer simulations of complementary MODFETs in comparison with E/D type MODFETs using SPICE[NAGEL 75]. The main tasks in this chapter are (i) to clarify the potential advantages of complementary MODFETs, especially high noise margins, (ii) to evaluate the speed degradation that complementary MODFETs suffer from using the low mobility p-channel MODFET, and (iii) to evaluate the range of propagation speed versus power consumption for complementary MODFET technology and compare this with other technologies. Chapter 3 describes the fabrication process that was developed to demonstrate the performance potential of complementary MODFETs. First, we describe the choice of the conventional MODFET structure over other versions of heterostructure FETs to experimentally evaluate the potential of complementary heterostructure FETs. Then, the overall fabrication process is described, including detailed explanations of the MBE and selective epitaxial regrowth. Chapter 4 describes initial experimental results of p-channel, n-channel and complementary MODFETs using 2μm gate length devices. Chapter 5 describes various improvements suggested by the initial results. Major areas for improvements include: p-channel MODFET drain current capability, reduction of the DX center problem in n-channel MODFETs and the lateral scaledown of the gate lengths to 1μm. Three approaches for p-channel improvements were pursued: double heterostructure p-MODFET, strained layer quantum well p-MODFET and doped-channel p-MODFET. Chapter 6 is devoted to experimental results and discussions on the improved structure for complementary MODFETs. Dynamic circuit

results are compared with existing technologies and projections are made comparing complementary MODFETs with other semiconductor devices. Chapter 7 summarizes the main contributions of the present thesis and suggests several topics for future work.

Chapter 2

SPICE SIMULATIONS

2.1. INTRODUCTION

In this chapter, performance comparisons are made between complementary logic and enhancement / depletion (E/D) type logic based upon SPICE [NAGEL 75] simulations. Since there were no existing SPICE MODFET models, appropriate adaptation of existing models was required. The key assumptions in adapting MOSFET SPICE models for MODFETs are described in section 2.2. The calculational method for determining propagation delay is described in section 2.3. The major results of the simulation and discussion are given in section 2.4, where the first part concerns noise margins, the second part deals with propagation delay and the third part describes power consumption and power delay products.

2.2. DEVICE PARAMETERS

The principle of the MODFET device operation is nearly identical to that of the MOSFET and the physical correspondence between these two types of FETs has been discussed [PIERRET 84]. Thus, for the initial simulation of MODFET circuits, the SPICE[NAGEL 75] parameters for MOSFETs are modified to fit the experimental MODFET data. The device structure shown in Fig.2.1 was used for the typical MODFET structure [MIMURA 84]. The key experimental device parameter which must be modeled is the gain parameter, K, which is modeled as follows:

$$K = \mu \left(\frac{W}{L} \right) C_0 , \tag{2.1}$$

where μ is the electron(hole) mobility, W is the gate width, L is the gate length, and

$$C_0 = \frac{\varepsilon(\text{AlGaAs})}{t\,(\text{AlGaAs})} \tag{2.2}$$

where ε is the dielectric constant and t the thickness, respectively of the AlGaAs layer. This fitting is done as a function of different gate lengths as shown in Fig.2.2[ABE 84].

The key assumptions for this fitting are as follows:

(i) For the static current-voltage characteristics of enhancement MODFETs, the measured device gain parameter , K, in Fig.2.2 is used for n-channel MODFETs of various channel lengths.
(ii) For the static current-voltage characteristics of depletion type MODFETs, the corresponding K-values in Fig.2.2 are decreased by the ratio of the AlGaAs thickness between enhancement and depletion type devices.
(iii) For the static current-voltage characteristics of p-channel MODFET one fifteenth of the K-values given in Fig.2.2 for n-channel devices are used. This corresponds to the ratio of mobilities for electrons and holes in GaAs.

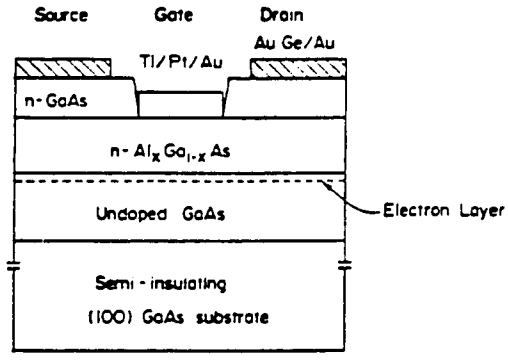


Fig.2.1 Device structure of a HEMT. GaAs cap layer thickness and $Al_{.3}Ga_{.7}As$ thickness are 500Å and 600Å respectively.

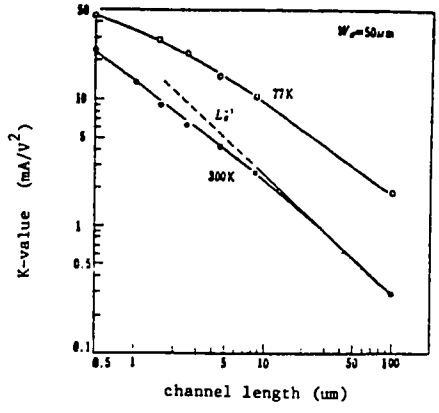


Fig.2.2. Device gain parameter (K-value) dependence on channel lengths of a HEMT(n-channel MODFET).[ABE 84]

(iv) For dynamic analysis, MOS gate capacitance-voltage relations were assumed to be valid in MODFET analysis*.

* The small signal gate capacitance-voltage relations derived for MODFETs [LEE 83], for example, can be shown to be identical to the first order calculation derived for MOSFET[MEYER 71],[LIU 82].

(v) The gate-to-bulk capacitance is set to zero, since it is almost negligible for the MODFET structure because of the semi-insulating substrate and only gate-to-source and gate-to-drain capacitances are important in the analysis.
(vi) Gate overlap capacitances were set to be zero since there is no overlap, as shown in the MODFET structure in Fig.2.1.
(vii) In order to take account of the operation voltage limitation due to leakage current through the Schottky gate, the simulation voltage range was restricted to 0v to 1.0v.

In Table 2-1 below, K-values derived from Fujitsu data [ABE 84] and calculated transconductances based on these K-values are tabulated. These transconductance numbers turn out to represent quite well the experimental values reported later and lend greater credence to the predictions of these initial SPICE simulations.

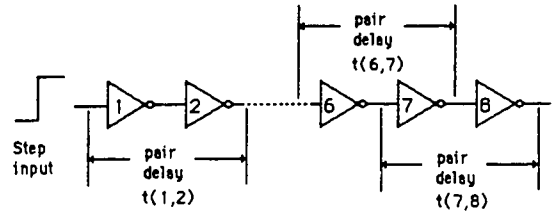
gate length		0.5μm		1μm	
temperature		300°K	77°K	300°K	77°K
K-value (mA/V^2 mm)	p-channel	490	930	274	710
	n-channel	32.6	62	18.3	47.3
g_m (mS/mm) at Vdd=0.6	p-channel	245	465	137	355
	n-channel	16.3	31	9.1	23.7
g_m (mS/mm) at Vdd=1v	p-channel	441	837	247	639
	n-channel	29.4	55.8	16.4	42.6
Gate Capacitance (pF/cm^2)		2.63×10^{-7} (Enhancement)		1.75×10^{-7} (Depletion)	

Table 2.1 Device parameters calculated from K-value data.

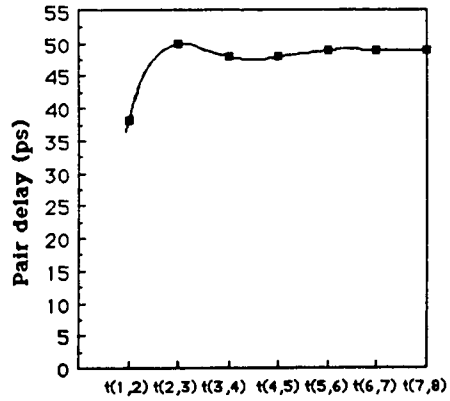
2.3. CALCULATIONAL METHOD OF INVERTER PROPAGATION DELAY

In order to save computation time as well as to avoid the uncertainty of ring oscillators, a chain of 8 identical inverters (Fig.2.3) are used to measure pair delays. The pair delay of the last two inverters of the chain has been chosen to represent the delay of inverters in realistic circumstances in an integrated circuit, where input wave forms are dumped through the preceding stages.

Generally, a stage delay depends upon input wave form as well as on the intrinsic delay and the capacitive load. So, it is necessary to have a configuration of enough stages to be able to measure the saturated delay time where the input wave form has the saturated slope that represents the real situation implemented in real circuits. An example of delay time convergence is shown in Fig 2.3. The constant delay after 5 stages assures the validity of the above method for the determination of pair delays.



A chain of 8 inverters used for delay simulation.



Figire 2.3 A chane of inverters and the pair delay convergence.

2.4. RESULTS AND DISCUSSION

The main purpose of this circuit simulation was to examine the values of noise margin of complementary MODFET circuits expected to be superior to E/D type MODFET circuits, which were and to examine the speed penalty complementary MODFETs pay by employing p-channel devices in the circuit. These results may seem to be analogous to a CMOS and NMOS comparison to some extent, but it is not obvious because of the much lower voltage operation (≈ 1 volt) of MODFETs and the high mobility difference between n-channel and p-channel FETs ($\mu(N)/\mu(P)\approx 15$) in GaAs.

2.4.1. Noise Margin

The worst case static series-voltage noise margin can be found graphically with the well-known "mirror-and-maximum-square method" [HILL 68]. However, since this condition is too severe to evaluate circuit performance[APPENDIX A], noise immunity will be used as a practical and less severe noise margin definition. Noise Immunity is defined as:

$$\text{Noise Immunity} = \frac{NM_0 + NM_1}{V_{DD}}, \tag{2.3}$$

where NM_0 and NM_1 represent noise margin of logic 0 and noise margin of logic 1, respectively, as defined in Figure 2.4. V_{DD} denotes the supply voltage. Simulated data for static characteristics of complementary and E/D type inverters are shown in Figure 2.5. The noise immunities of complementary and E/D type inverters are shown in Figure 2.6. Noise Immunities are plotted as a function of W/L ratio with supply voltage as a parameter.

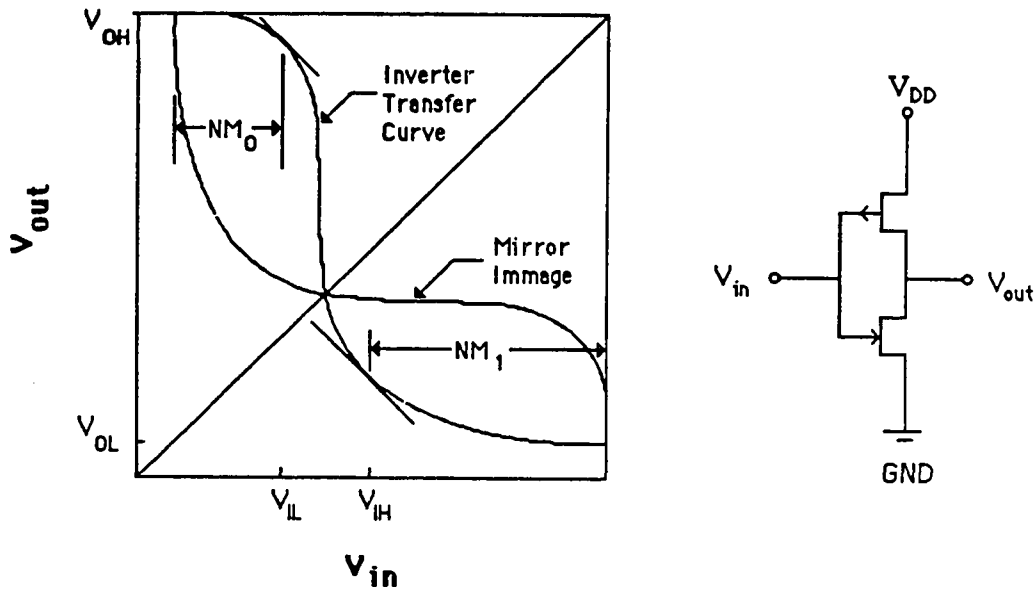
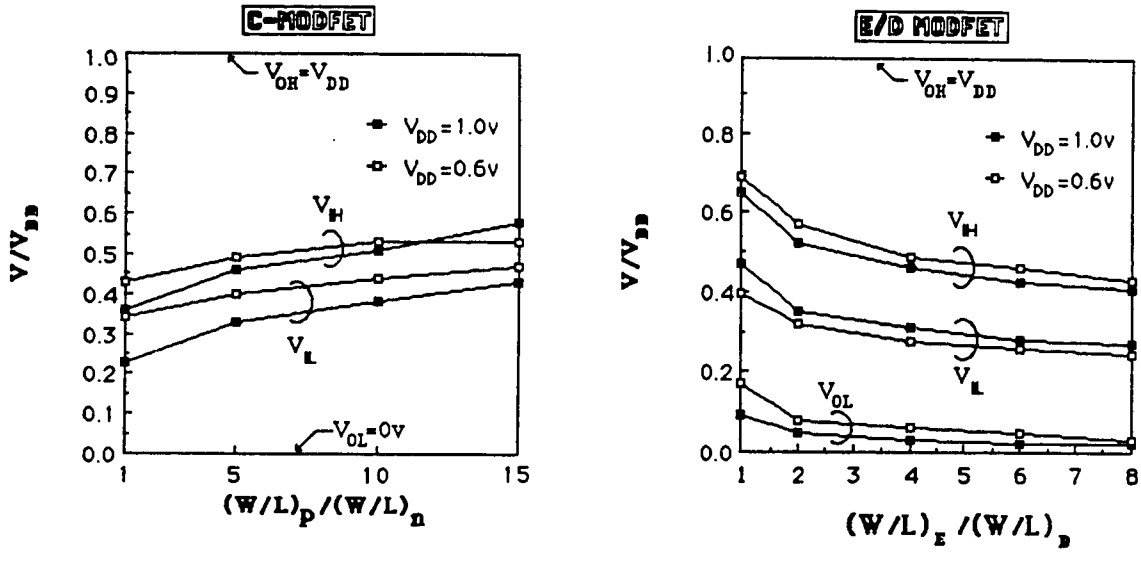
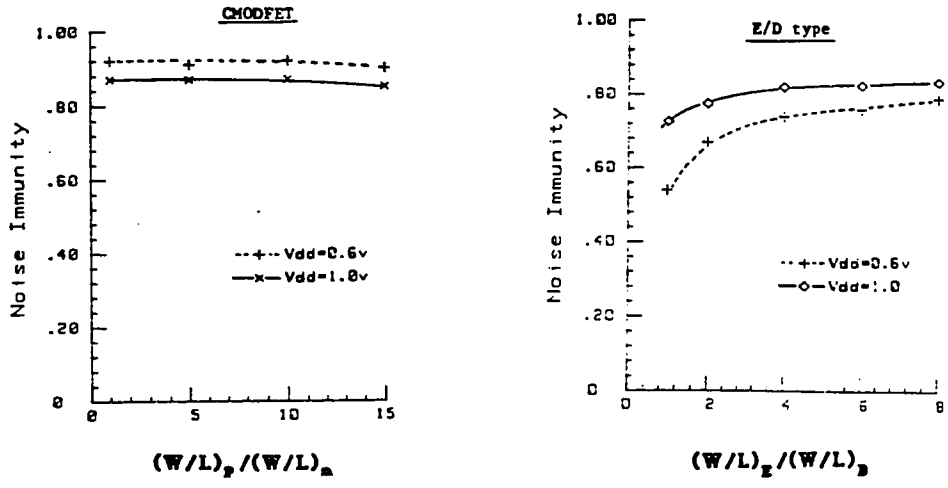


Figure 2.4 Voltage transfer characteristics of an inverter circuit.



(a) (b)

Figure 2.5 Static characteristics of a complementary MODFET inverter (a) and E/D type MODFET inverter (b).



(a) (b)

Figure 2.6 Noise immunity of complementary (a) and E/D type inverter circuits (b).

The results show that the noise immunity for the complementary type is superior to the E/D type over a wide range of W/L ratio in keeping high noise margin. In other words, (i) one can choose any reasonable W/L ratio to optimize speed, power etc. for complementary circuits while still achieving a high noise margin and (ii) for E/D type circuits, there arise constraints on geometric ratio in order to maintain sufficient noise margin, e.g., assuming a conservative value of 0.8 for the minimum noise immunity, a condition of $(W/L)_E$ / $(W/L)_D \geq 4$ should be satisfied in the case of 0.6 volt supply voltage and a condition of $(W/L)_E$ / $(W/L)_D \geq 8$ should be satisfied in the case where 1 volt power-supply is used. Note also the secondary effect that the lower power-supply voltage improves the noise immunity for complementary type, whereas a higher supply voltage is better for the E/D type.

2.4.2. Propagation Delay

Propagation delays for 1 μm and 0.5 μm gate length devices are shown in Figures 2.7(a) and 2.7(b) respectively. In both figures, propagation delays are plotted versus capacitive load, which is connected to each output node in addition to the gate capacitance of the next stage inverter. For complementary type circuit simulations, V_{DD} = 0.6v was chosen because complementary circuit operation without significant static current is limited

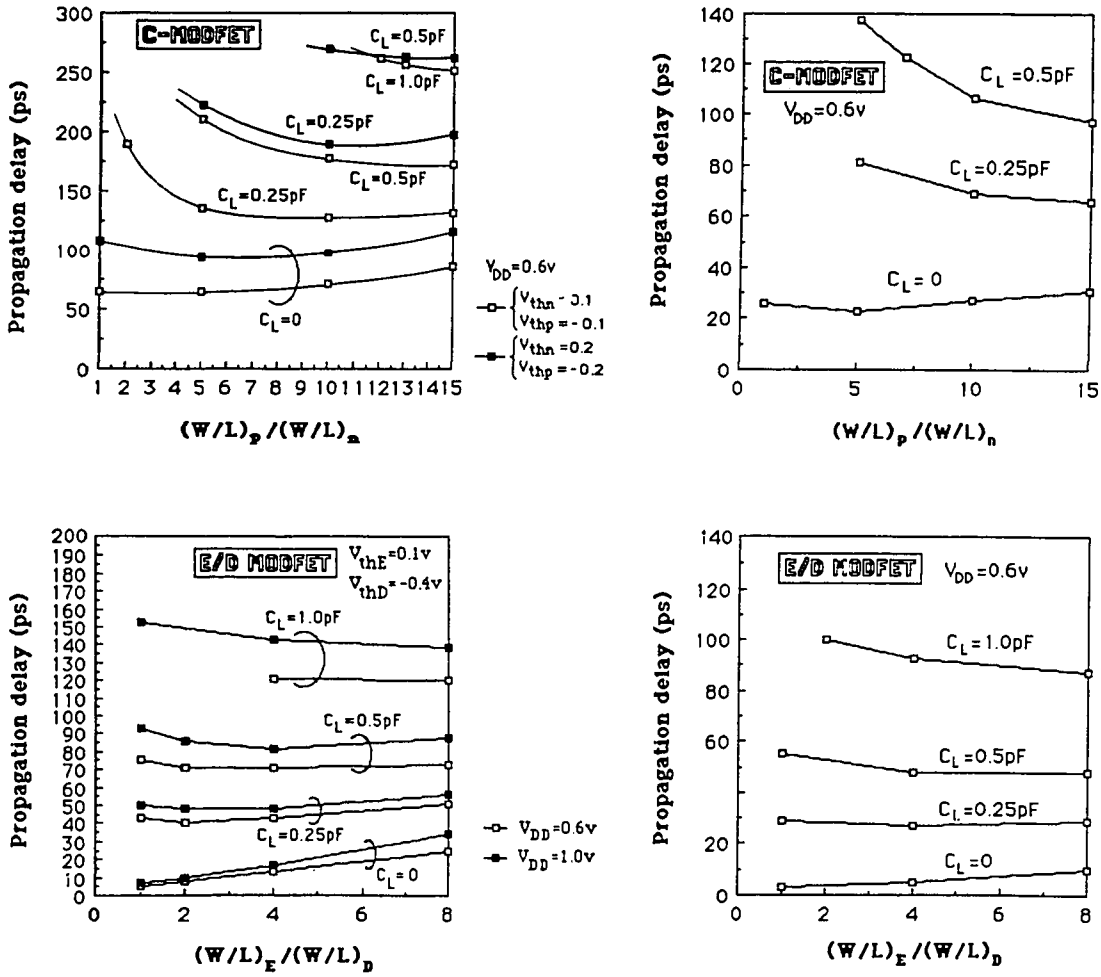


Figure 2.7 Propagation delay of complementary and E/D MODFET circuits as a function of W/L ratio of an inverter for (a) 1μm gate length device and (b) 0.5 μm gate length devices.

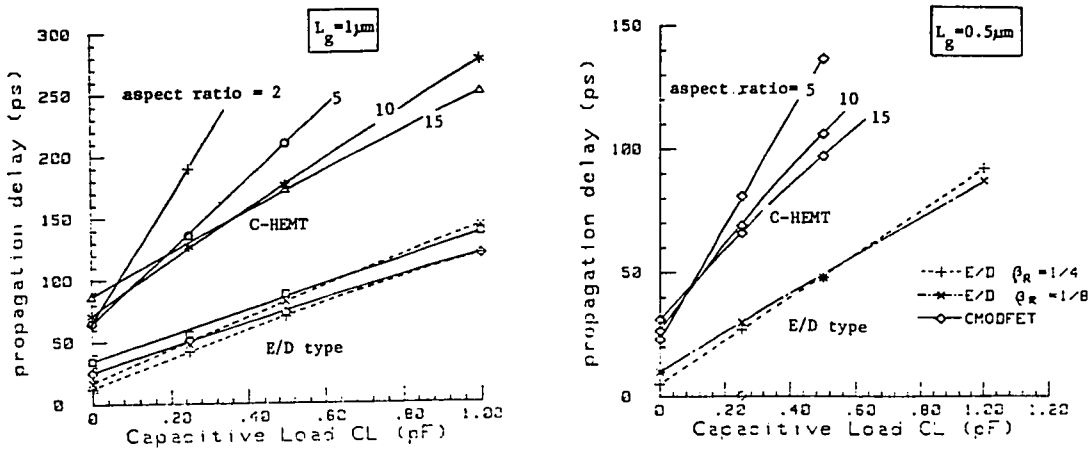


Figure 2.8 Propagation delay of complementary and E/D MODFET circuits as a function of capacitive load for (a) 1μm and (b) 0.5μm gate length devices.

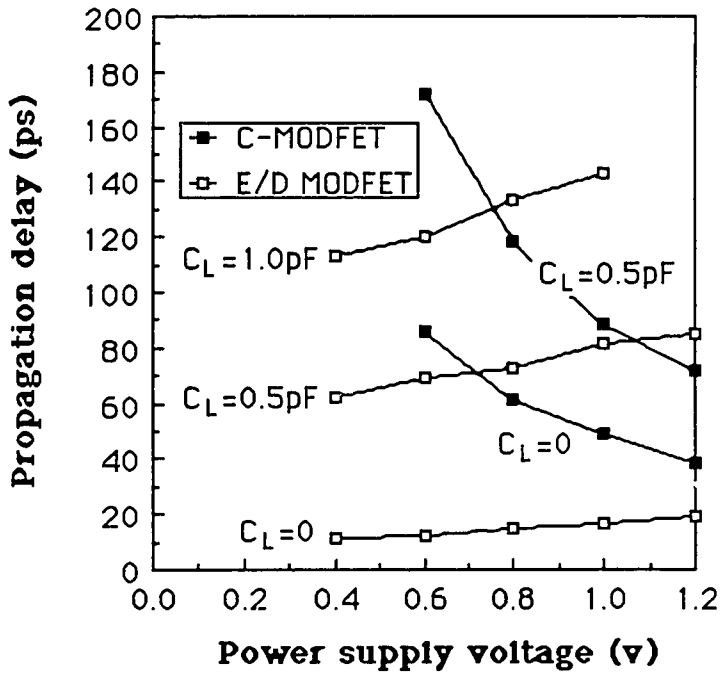


Figure 2.9 Propagation delay of complementary and E/D MODFET circuits as a function of supply voltage.

by the gate leakage current due to the low Schottky barrier height of p-channel gates. Figures 2.7(a) and (b) clearly show that the complementary type is slower than E/D type for any W/L ratio when compared with the same capacitive load. It should also be noted that the complementary type is quite sensitive to threshold voltage, which results in a significant supply voltage dependance,as shown in Fig.2.7. This indicates that the limited gate-to-source voltage is degrading the speed of the complementary type MODFET inverter. It should also to be noted that the minimum speed occurs at smaller gate widths of the p-channel device with low input capacitance and the minimum point moves to the ratio of W_P / W_N = 15, which gives $\beta_P / \beta_N = 1$. This indicates that in the range of C_L = 0 - 0.5 pF, the propagation speed is limited both by the large gate capacitance and by the high resistivity of p-channel MODFETs.

Speed performance of E/D type circuits shown in Fig.2.7(a) indicate little dependence on W/L ratio except C_L = 0 case, where the speed is strongly affected by the gate capacitance. Another point to note for E/D type circuits is that their higher speed at lower voltage which is the result of their constant load current having to charge the capacitance to smaller values of supply voltage. However, for fixed W/L ratio, the low supply voltage does not provide adequate noise immunity as shown in Figure 2.6. A similar result for the shorter gate length case of L = 0.5μm is shown in Fig.2.7(b), where V_{DD} = 0.6v is used for both complementary and E/D type circuits. This figure shows greater improvements in speed for the complementary case compared to the E/D circuit at shorter gate lengths. It is however, still clear that the E/D type is far superior to complementary type in terms of raw speed.

Using Figures 2.7(a) and (b), the propagation delay dependence on capacitive load are plotted for both complementary and E/D circuits in Figures 2.8(a) and (b) respectively. This figure shows that an overall speed ratio of about 2 is expected for both channel lengths, L = 1μm and L = 0.5μm, i.e E/D type is faster than complementary type by a factor of about 2 with any capacitive load. Extrapolated points represent input gate capacitance and these values (absolute values of the extrapolation) are proportional to the gate area, as expected. These parasitic gate capacitances decrease in short channel devices, and this can be seen in Figures 2.8(a) and (b). The reduction of geometry may appear to help the complementary type MODFET performance compared to the E/D type, however not significantly if we compare speeds at the same capacitive load points. This occurs because the parasitic capacitance is expected to be much smaller than the gate capacitance in MODFET structures with an undoped substrate and the total capacitive load should be dominated by the input gate capacitance. Consequently, it is not a fair comparison of speeds when we look at the delays for the same capacitive load point when we compare

the propagation delay of different gate length devices. In order to do this comparison correctly, we need to evaluate average fanout number and the parasitic capacitance of the interconnect lines. An easy way to do this task without evaluating average fanout and interconnect line length, is just to assume ring oscillator circuits where capacitive load simply equals the input capacitance of the next stage inverter(zero parasitic capacitance). This is done in the next section and the results are compared with various semiconductor technologies. An alternative way of increasing the C-MODFET speed is to increase the supply voltage in some way. In Fig.2.9, propagation delays are simulated for various supply voltages, neglecting the voltage limit set by the gate leakage current through the low Schottky barrier height for holes at a metal /AlGaAs interface. A barrier height of 0.7 volts for 40% of Aluminum in the AlGaAs layer was used. It is noteworthy that, with a supply voltage of greater than 1.2 volt, C-MODFET catches up E/D MODFET in speed. Thus structures with greater barrier heights could dramatically effect this result.

2.4.3 Power-Delay Product

The power consumption of a complementary FET circuit is low because there is virtually no static current. Thus, the total power of a complementary circuit stage is dominated by the dynamic power which is expressed as:

$$P = C_L V_{DD}^2 f \tag{2.4}$$

where C_L is load capacitance,V_{DD} denotes power-supply voltage, and f represents the input clock frequency.

In integrated circuits, the power dissipation per stage is expressed as:

$$P = C_L V_{DD}^2 \frac{1}{N\tau} p \tag{2.5}$$

where N, τ, p are the average number of delays per clock cycle, the delay per stage, and the switching probability, respectively. System designs require N to be 10~15 and the average switching probability, p, is typically 20% [APPENDIX B] yielding a factor of 50 % smaller power dissipation compared with the simple evaluation of CV^2f, where f is substituted for $1/\tau$. Taking account of the above argument on power dissipation and using the simulation results for single stage propagation delay , the power-delay product of complementary MODFET circuits is evaluated and compared with other existing technologies in Figure 2.10. The data of other technologies are taken from standard conditions: Si MOS families use single 5v as V_{dd}, with 2μm nominal gate lengths,

submicron CMOS has 0.7-0.8μm effective channel length, Silicon ECL uses standard voltage supply of 5.2v with 1.25-1.5 μm feature size, GaAs MESFET and MODFET use 1-1.5v voltage supply with gate feature size of 1.5μm. The measured temperature is room temperature unless explicitly stated. Most state-of-the-art standard technologies are compared and some of the new bipolar approaches, such as Super-Self-align Process Technology (SST) [MIYANAGA 84] are neglected for simplicity, but competing technologies such as low temperature CMOS and MODFETs are shown in the figure although they are not established and standard yet. Complementary MODFET circuits exhibit the smallest power-delay product among all existing semiconductor technologies and thus represent an attractive candidate for very high speed VLSI technology.

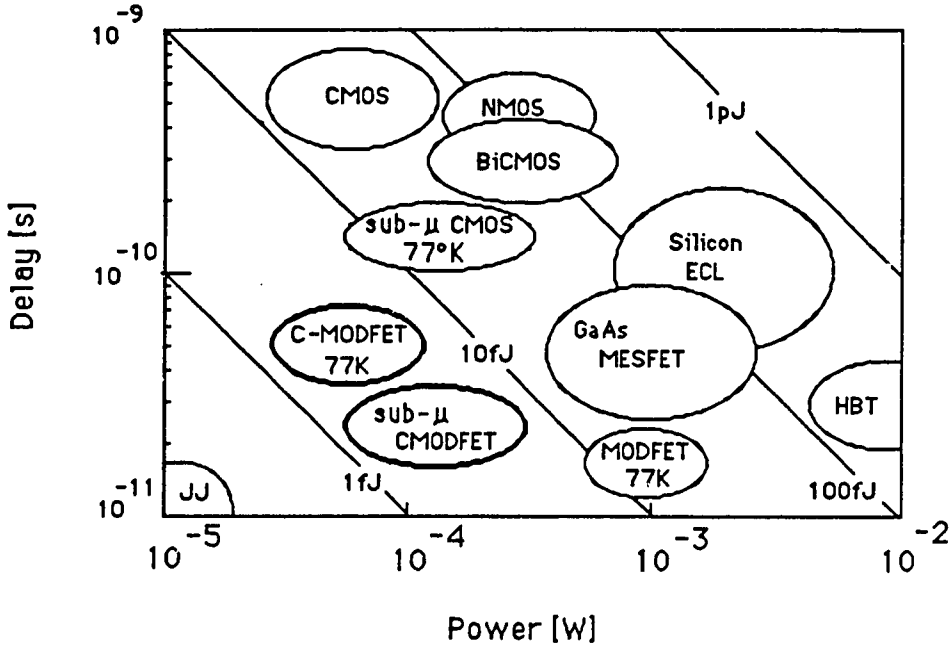


Figure 2.10 Projected propagation delay vs power dissipation for complementary MODFET circuit and other competing IC technologies.

2.5. CONCLUSION

A comparison of predicted circuit performance between C-MODFET and E/D MODFET has been done using SPICE simulation. While complementary type inverters show slower speed than E/D type inverters by a factor of 2, their noise immunity is superior to E/D MODFET circuits over a wide range of W/L ratio, yielding much greater flexibility in circuit design. Small power consumption allows C-MODFETs to yield the smallest power-delay product among all semiconductor devices.

The simulation, disregarding the gate leakage current, also shows that C-MODFETs could exceed E/D-MODFETs in switching speed at higher supply voltage (V_{DD} >1.2v). This suggests development of p-channel MODFETs with higher Schottky barrier height. While the structure is beyond the scope of this thesis, it provides significant incentive to begin development of conventional p-channel MODFETs and evaluate C-MODFET circuit concepts.

Chapter 3

DEVICE STRUCTURE AND FABRICATION PROCESS

3.1 INTRODUCTION

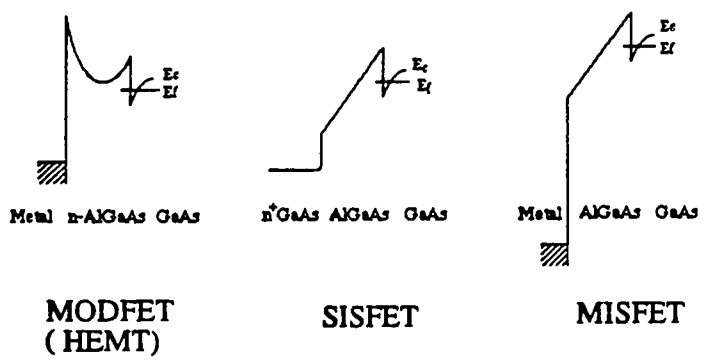
In this chapter, a target device structures for complementary MODFETs are described and the fabrication process is explained in detail. In the second section, several kinds of heterojunction field-effect transistors are compared and the choice of MODFET structure is rationalized for the purpose of checking the potential of complementary heterojunction FETs experimentally. In the third section, the overall fabrication process is described, followed by detailed explanations of the molecular beam epitaxy (MBE) technology and selective regrowth which were developed for this investigation.

3.2 TARGET STRUCTURE

After the first MODFETs were demonstrated [MIMURA 80] [DELAGEBEAUDEUF 80], several alternative structures were proposed and demonstrated, such as: SISFET [SOLOMON 84] [MATSUMOTO 84], MISFET[ARAI 85] or HIGFET[DANIELS 86], and Inverted-HEMT [KINOSHITA 84]. Each structure has advantages and disadvantages. Thus the device structural choice becomes a strong function of the specific circuit objectives, (i.e. raw speed, low power, minimum speed-power product, sensitivity to threshold voltage, etc.). Since our ultimate goal is to investigate the potential of complementary heterojunction FETs in digital applications through experimental demonstration, we had to carefully choose a structure which maximized its performance and was at least feasible to implement. A comparison of various heterojunction FETs are listed in Figure 3.1. MODFETs (or HEMTs) have inherent advantages because of their adjustable threshold voltages by either doping or gate recess. This situation is easily understood when we recall that the threshold voltage of a MODFET depends on the thickness and impurity doping level of the AlGaAs layer. However, a rather complex processing approach, such as two MBE growths, is needed to implement a complementary circuit based upon these devices. A SISFET, in which a heavily doped GaAs layer is

substituted for a metal gate, has a uniform and constant threshold voltage, since the barrier height in this case is nearly equal to the conduction-band discontinuity near the channel, as shown in the band-diagram in Fig.3.1. However, the near zero thresholds allow large static current to flow during the switching cycle when this device is applied to a comlementary circuits. SISFET also have a structural disadvantage of high sheet resistivity of the gate semiconductor and increasing the thickness of the gate semiconductor conflicts with processing goals of surface planarity. A complex process approach is also inevitable to realize a complementary circuit using SISFETs. A MISFET structure, being the simplest, is advantageous for processing, especially when the complex complementary structure is involved. However, it has serious disadvantages with threshold voltage mismatch between p-channel and n-channel FETs and large threshold voltages (≈ half of the operational voltages). These large threshold voltages greatly degrade the drain current and hence speed capabilities. It is clear at this stage that the MODFET approach is most suited to demonstrate the highest performance potential in heterojunction complementary circuits, despite its difficulties in fabrication and controlability.

	Advantages	Disadvantages
MODFET (HEMT)	Adjustable threshold voltage	Larger variation of threshold voltages
SISFET	Good uniformity of threshold voltage ($V_{th} \approx 0v$)	High static current
MISFET	Simple structure	Too large V_{th} ($V_{thn} \approx 0.8v, V_{thp} \approx -0.6v$)



MODFET (HEMT) SISFET MISFET

Figure 3.1 A comparison of various GaAs Heterojunction FETs

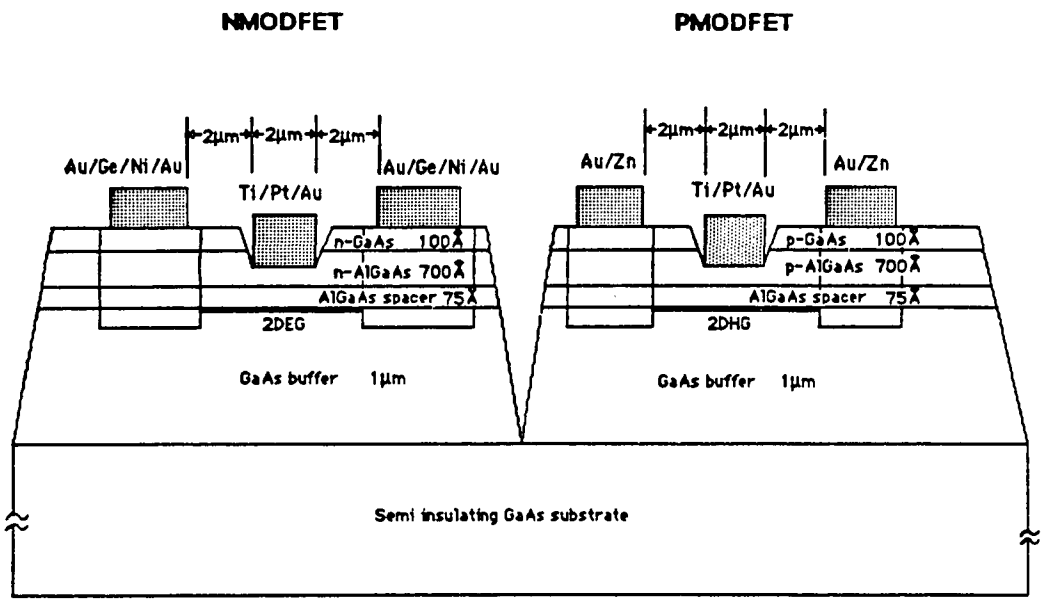


Figure 3.2 A target structure for complementary MODFET circuits

Fig. 3.2 shows a target structure for a complementary circuit, consisting of both n-channel and p-channel single heterojunction MODFETs, integrated on a wafer in a planar fashion. This structure requires separate n and p-channel MBE growth, but provides maximum flexibility in circuit design. The development of this double MBE growth and fabrication technology are described in the following sections.

3.3 FABRICATION PROCESS

In this section, a general description of our process flow for complementary MODFETs is given. This is followed by descriptions of molecular beam epitaxy (MBE) and selective regrowth technologies.

In this section, a general description of our process flow for complementary MODFETs is given. This is followed by descriptions of molecular beam epitaxy (MBE) and selective regrowth technologies.

3.3.1 Process Flow

Figure 3.3 shows our process flow for a complementary MODFET circuit. First, a MODFET structure is grown by molecular beam epitaxy. This could be either n-channel or p-channel MODFET. We chose to grow the n-channel MODFET structure first to minimize Be diffusion in the p-type modulation-doped layers by setting the Be doping growth at the final stage of the two MBE growths. After growth of the n-channel layers, a 3000Å silicon dioxide layer is deposited by PECVD (Plasma Enhanced Chemical Vapor Deposition). A regrowth pattern is formed using the 1st mask layer and the silicon dioxide film is etched by dipping the wafer in a buffered HF (6:1). Subsequently, the initial n-MODFET layers are etched by a phosphoric based etchant ($H_3PO_4 : H_2O_2 : H_2O$ = 1:1:30) down to the original GaAs substrate surface. The wafer is then taken to the MBE chamber again to do the regrowth for p-channel MODFETs, using the silicon dioxide film as a mask. Subsequently, the poly-crystalline GaAs grown on the silicon dioxide layer is removed by the H_3PO_4-H_2O_2-H_2O (=1:1:30) solution using a second level mask. Residual polycrystalline GaAs at the periphery of the regrown region is lifted off by etching all the silicon dioxide on the surface of the wafer by buffered HF(6:1). The wafer now consists of n-channel regions and p-channel regions. Using a third level mask, the device isolation is done by mesa etching using the H_3PO_4-H_2O_2-H_2O (=1:1:30) solution. A second 3000Å PECVD silicon dioxide film is then deposited. This film serves as surface passivation as well as a spacer layer to help lifting off metal layers by forming an overhang structure together with the photoresist layer. By following this process, the wafer surface will be covered either by a passivation film (silicon dioxide) or metals (ohmic metal and gate metal) leaving no GaAs surface exposed to the atmosphere. Using a fourth level mask, an n-type ohmic contact pattern is defined and the silicon dioxide is etched to form an overhang structure. Then, n-type ohmic metal (Au/Ge/Ni/Au) is evaporated by e-beam evaporation and lifted off. Similarly, using a fifth level mask, the p-type ohmic pattern is defined and the ohmic metal (AuZn/Au) is evaporated by thermal evaporation. Both types of ohmic metals are alloyed simultaneously in a rapid thermal annealer at 450°C for 30 seconds. Using a sixth level mask, gate patterns are defined and after silicon dioxide is etched by a buffered HF(6:1) etch, a gate recess etch is performed using a H_3PO_4-H_2O_2-H_2O (=1:1:30) solution at 15°C. Gate metal (Ti/Pt/Au) is then

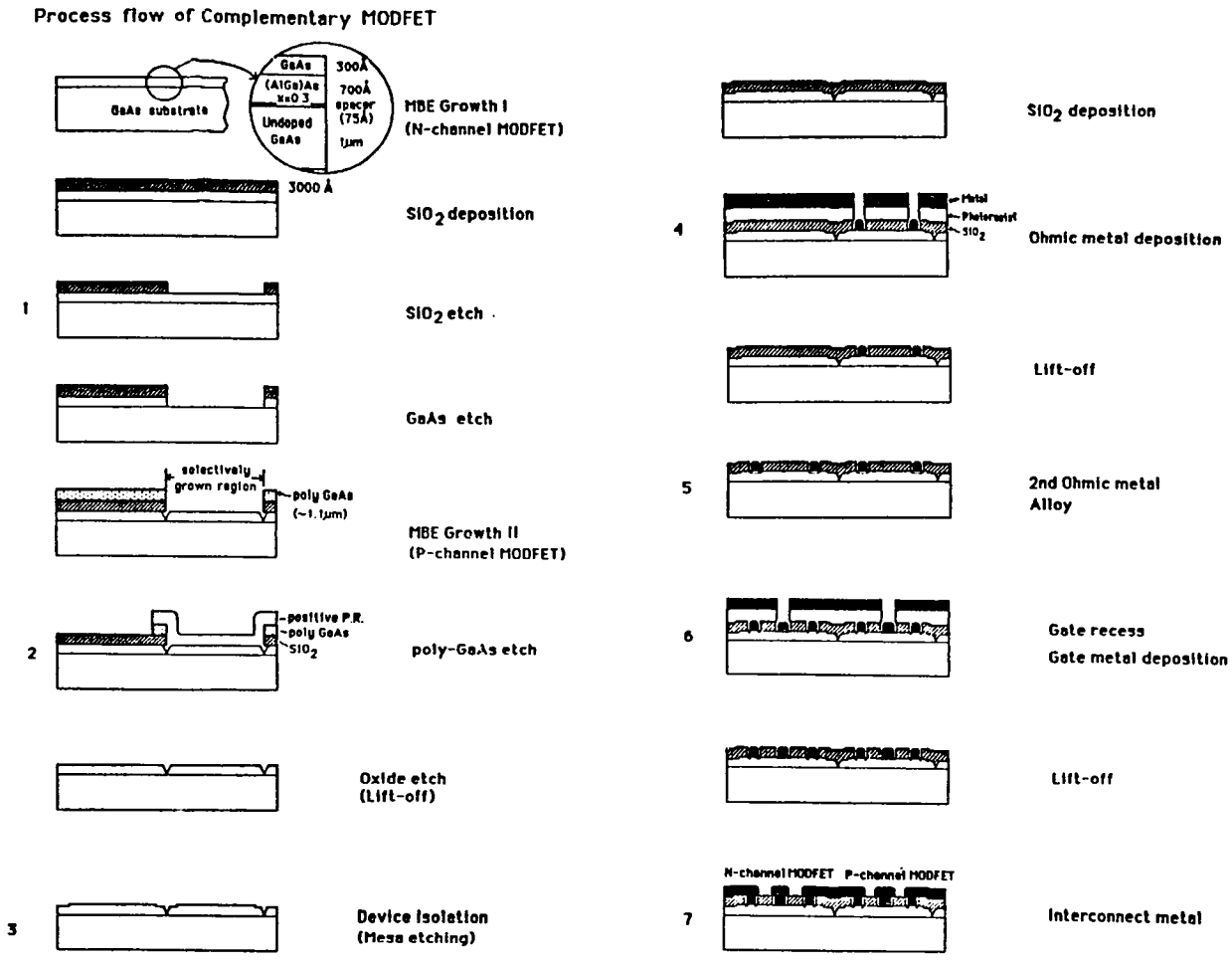


Figure 3.3 The process flow of a complementary MODFET circuit.

evaporated by an e-beam evaporator and the metal is lifted off by an acetone dip. Finally, using a seventh level mask, the interconnect pattern is defined and a 5000Å metal (Ti/Au) layer is evaporated by e-bean evaporation and lifted off using a chlorobenzene technique [MIMURA 86].

3.3.2 Molecular Beam Epitaxy and Selective Regrowth

3.3.2.1 Molecular Beam Epitaxy

The Stanford MBE machine is based on the standard GEN-II system commercially available from Varian Associates, but it has several additional features such as (i) an expandable system which can be connected to metalization and Auger/e-beam/focussed ion beam systems for in-situ patterning through a transition tube connecting the two isolated growth chambers, (ii) an Indium free wafer mounting system[HELLMAN 86], and (iii) a recirculating refrigeration system which provides the continuous cooling of the radial vane source shroud using an isopropyl alcohol/water mixture maintained at minus 10°C.

Our system has Gallium, Arsenic, Aluminum, Silicon, Beryllium and Indium elemental sources. All source/substrate temperatures and furnace shutters are computer controlled by a HP9000 Model 540.

Our system was the first system which was especially suitable for the fabrication of complementary MODFETs requiring two separate growths. Because the substrate is free from troubles of indium bonding, it eliminates the necessity for backside polishing, particularly for pattern definition between the two growths.

Similar wafer preparation recipes are used in many laboratories. However, when examined in detail, they are all different, even from individual to individual in the same lab. Basically a wafer preparation consists of three steps : (i) solvent clean, (ii) GaAs surface etch to remove defects and microscopic scratches caused by wafer slicing and polishing, and (iii) final etching of oxides formed in the second step. We use boiling acetone, trichloroethylene(TCE), acetone, isopropyl alcohol in this order to clean wafers followed by deionized(DI) water rinse. The first acetone rinse removes water from the surface. TCE removes any organic contamination, and the second acetone rinse desolves the remaining TCE. Isopropyl alcohol desolves any remaining acetone. Solvent cleaning steps can be skipped for wafers prepared by reliable wafer suppliers. We use H_2SO_4-H_2O_2-H_2O (=4:1:1) etchant with its temperature set to 40°C±2° for one minute to remove about 5μm of the GaAs surface. The temperature is set so as to be low enough to avoid

wavy surfaces but high enough to etch the wafer surface within a reasonablly short time. The DI rinse should be long enough (typically 4 minutes minimum) to completely dilute and remove the sulfuric acid since it is nonvolatile. The NH_4OH-H_2O_2-H_2O (1:1:10) etchant removes all oxides on the wafer surface formed in the long DI rinse. The wafer is then spin-dried and immediately loaded into the MBE load chamber.

After the wafer is prebaked in the load chamber (10^{-8} Torr range) at up to 400°C for an hour to remove water, it is brought into the transition tube (low 10^{-9} Torr range) and then brought into a growth chamber (typically 10^{-10} Torr range with idling source temperatures). The oxide is removed by heating the substrate to ~680°C for typically 20 minutes. The surface is examined by Reflection High-Energy Electron Diffraction (RHEED) prior to the growth. During the growth, the substrate is rotated at typically 5 to 10 rpm in order to produce good uniformity in thickness and doping. Uniformity over a 2-inch wafer is within 2%. The growth rate is typically 0.5 μm to 1μm/hr. There is a trade-off between growth time and oval-defect density because both growth rate and galliun oxide evaporation rate (causing defects) are proportional to the gallium source temperature. Depending on the device structure, growth design should take into account the trade-off of substrate temperature unless multi gallium sources are available. This is because the best growth temperatures are different for different materials, e.g., ~470°C for InAs(or InGaAs), 600-660°C for GaAs, and 700-750°C for AlAs(or AlGaAs)*. For our initial target structures for complementary MODFETs, consisting of AlGaAs/GaAs layers, a substrate temperature of 660°C was used with a growth rate of 1μm/hr. For more complex structures, such as pseudomorphic MODFETs, optimization discussions will be given in the later chapters.

3.3.2.2 Selective Epitaxial Growth by MBE

In this sub-section, selective MBE, as a means to integrate p-channel and n-channel MODFETs, is described.

Patterned silicon dioxide (deposited by PECVD) is used as a masking layer for the etch-and-regrow technique by molecular beam epitaxy. Unlike MOCVD growth, poly-GaAs growth over the silicon dioxide surface commonly occurs under normal MBE growth conditions** (growth rate, As/Ga flux ratio, substrate temperature,...etc). Thus, a crucial part of the process sequence is the removal of the polycrystalline GaAs without

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* These (temperature) numbers change from system to system, depending on each measurement set up.

** In certain extreme growth conditions(at high substrate temperatures as high as 775°C), virtually no poly-GaAs growth has been observed, even in MBE [OKAMOTO 87].

etching the single crystal AlGaAs/GaAs layers. For this purpose, it becomes important to develop a structure in which a natural breakage occurs between single crystal and polycrystalline GaAs after the regrowth. It is ideal to etch the GaAs substrate p-region all the way down to the initial surface of the first MBE growth prior to the regrowth. The relatively thick etch (≈1μm) through the layer in the [100] direction produces a preferential etch toward the [111] directions at the edge of the silicon dioxide mask pattern. Figure 3.4 shows cross sectional SEM micophotographs of selective regrowth observed from two directions. They clearly show the breakage between the poly- and single crystal GaAs regions. It is also desirable to have a buffer layer of about 1μm in depth for the purpose of minimizing the effect of interface states on MODFET I-V characteristics. Patterned etching is done using H_3PO_4-H_2O_2-H_2O (=1:1:30) solution at 15°C, followed by DI rinsing for at least four minutes.

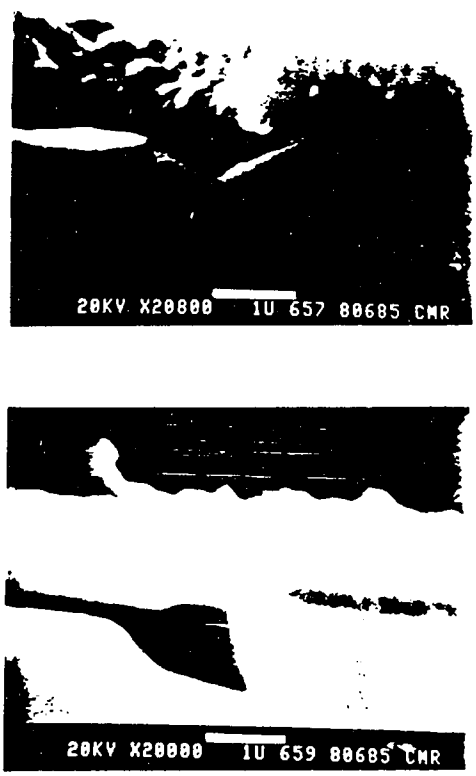


Figure 3.4 Cross sectional SEM mirophotographs of selective regrowths (a) along [011] direction and (b) along [110] direction.

Before bringing the pattern-etched wafer into the load-lock of the MBE machine, final etching is done using NH_4OH-H_2O_2-H_2O (1:1:10) etchant for ten seconds to remove any residual oxide from the surface. This is followed by a DI rinse and spin dry. This final DI rinse should be long enough to rinse off residual etchants but short enough to prevent thick oxide formation. If this DI rinse is insufficient, GaAs dendrite formations are observed on the silicon dioxide region as shown in Figure 3.5. Dendrites create a serious problem for the subsequent circuit processing by forming holes in the silicon dioxide when a photo-lithography mask is pushed against the wafer in the next exposure step by the contact aligner.

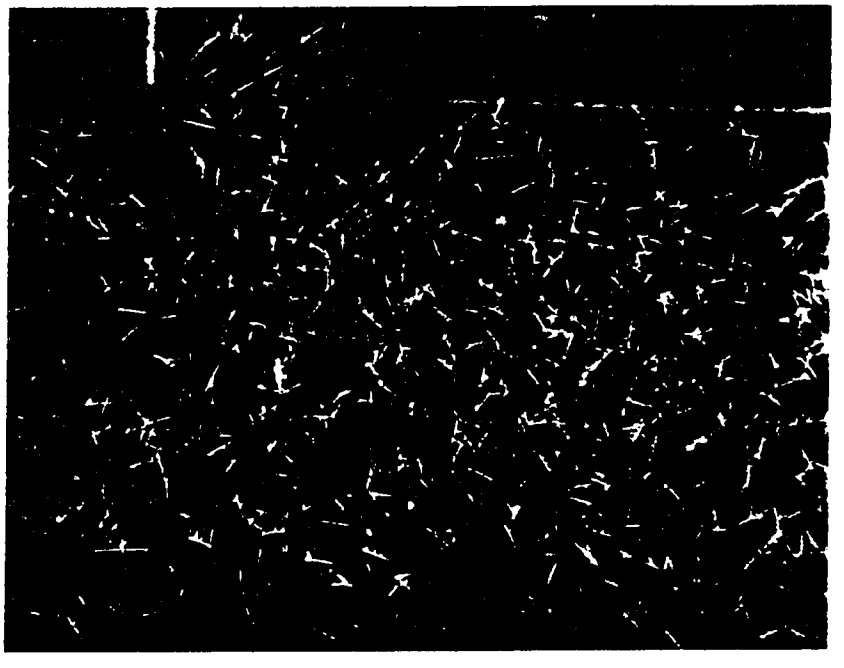


Figure 3.5 GaAs dendrite formation on the surface of polycrystalline GaAs grown on silicon dioxide by MBE as a result of inadequate surface cleaning.

Before introduction into the growth chamber, the substrate is baked in the load-lock. The same substrate temperature (400°C) is used as the normal growth, but for a longer time (≈ 1.5 hour) to minimize possible contamination into the growth chamber. The final heat-clean of the surface oxide prior to regrowth consists of a 30-40 minute bake at 680°C ($T_{sub.}$). We use the same growth conditions for the regrowth as for the normal growth (Section 3.3.2.1).

The surface morphology of the regrowth film pattern observed under an optical microscope looks identical to the normal films grown without patterning. Observed defect densities of both oval defects and the defects from other origins were comparable to the normal films. The defect densities appeared to be independent of pattern size. The two dimensional photo-luminescence results show normal intensity over the entire region including into every corner and along the edge to within the resolution (20μm) of the measurement as shown in Figure 3.6.

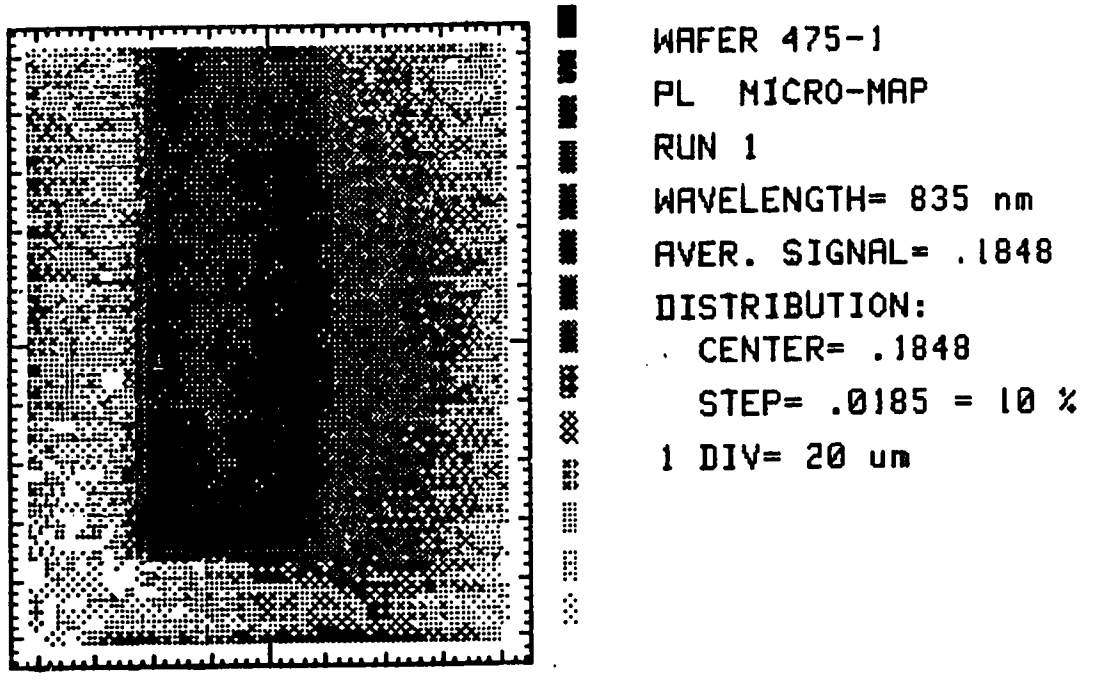


Figure 3.6 Two dimensional photo-luminescence result of a MBE regrown region (dark pattern in the center). The surrounding region is covered with silicon dioxide film.

However, electrical measurements of MODFETs fabricated on various sized patterned regrowth regions show that the crystal quality gets degraded when the pattern size is smaller than 80 μm square or when the distance of the device from the edge is below 40 μm. The crystal quality seems absolutely normal when the pattern size is larger than 120μm square or when the distance of an FET from the edge is greater than 60μm. The dependence of I-V characteristics on growth area size are shown in Figure 3.5.

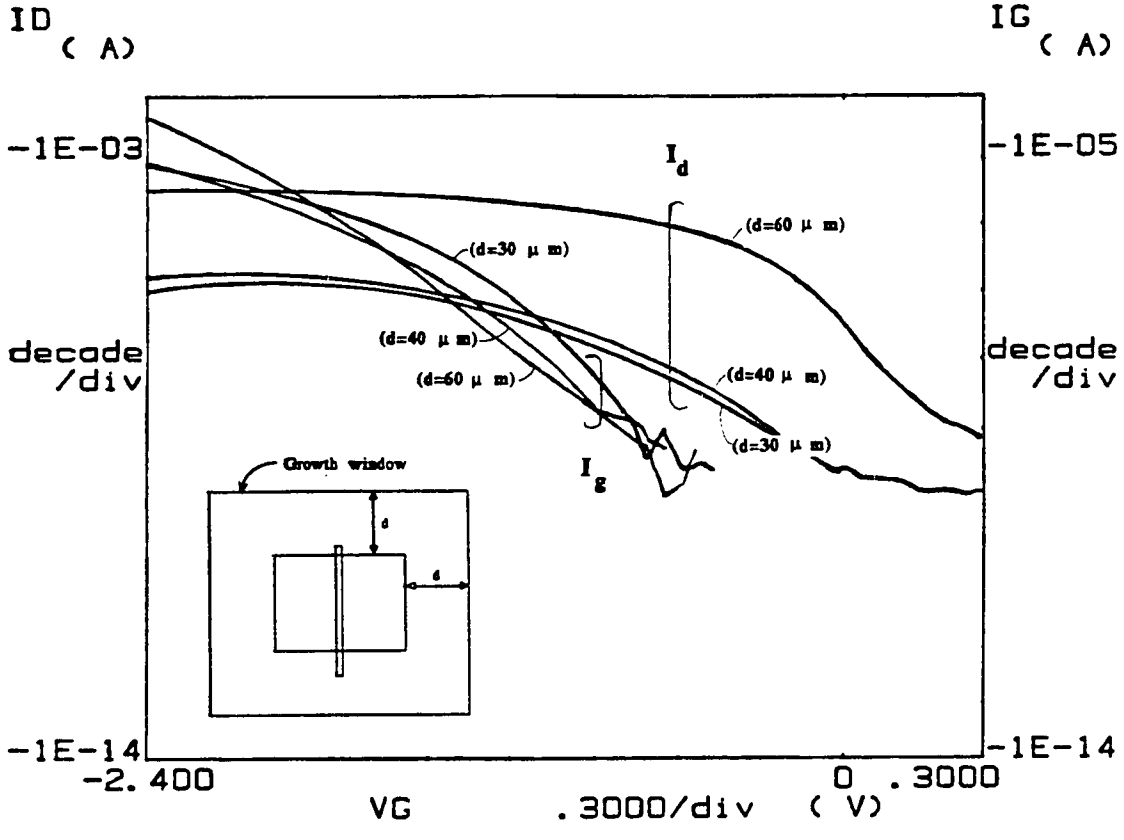


Figure 3.7 I_{ds}-V_{gs} characteristics (at 300°K) of p-MODFET formed on patterned regrowth region of various sizes. Distance between the outer edge of the device and the edge of the regrowth island is denoted by d.

Although the surface morphology and two-dimensional photoluminescence results did not show appreciable degradation in the crystal quality of the selectively grown area, electrical measurements using modulation-doped p-channel FETs in various island sizes showed significant drain-current collapse[YOH 88] in the small island where the distance between active area and the edge of the growth island is less than 40μm. Devices with larger island sizes showed as good I-V characteristics as normal MODFETs. These result suggest suppressed impurity incorporation of Be or compensation by increased deep level states near periphery of the growth island.

3.4 SUMMARY

In this chapter, we have compared various heterojunction FETs and chose the conventional MODFET structure as the best candidate to demonstrate the best complementary circuit performance. This approach is at the expense of increased process complexity, however it was a challenge that our Stanford MBE system was well suited to address. The fabrication process of our target structure for the first stage was described. Selective MBE was a key technology development and our process development was described. There is certainly far more to be studied on selective regrowth, but we had to stop at certain point where fabrication of our complementary circuit became possible in order to proceed with the primary project goal : to experimentally demonstrate the performance potential of complementary heterojunction FET circuites.

CHAPTER 4

ELECTRICAL MEASUREMENTS OF COMPLEMENTARY MODFETS

4.1 INTRODUCTION

The first version (2μm gate length) complementary MODFET circuits were fabricated using the processing technology described in chapter 3. Hall effect measurements of both n-MODFET and p-MODFET structures are discussed in the second section. In the third section, I-V characteristics of both p-channel and n-channel MODFETs are discussed. The forth section focuses on circuit performance of inverters and ring oscillators with first generation MODFET structures.

4.2 HALL-EFFECT MEASUREMENTS

Hall effect measurements were done on the two dimensional electron gas and hole gas system by van der Pauw method. The device structures are shown in Figure 3.2 (chapter 3). Note that the Hall samples have cap layers as well as thick AlGaAs layers because they are as grown samples. The Hall measurement results are summarized in Table 4.1. The dramatic increase of the electron and hole mobilities at 77°K indicate the successful formation of very good heterojunction interfaces and modulation-doped structures. The carrier concentration of the p-channel MODFET structure at room temperature is much higher than that at 77°K, while the electron concentration in the n-MODFET structure has a much smaller temperature dependence. Qualitatively, this is explained by the parallel conduction occurring in the thick AlGaAs layers of the Hall samples. In p-channel modulation-doped structures, the mobilities in p-AlGaAs (≈130 $cm^2/Vsec$) and the two-dimensional hole gas(≈400 $cm^2/Vsec$) in GaAs are of the same order, while the electron mobilities in n^+-AlGaAs(≈400 $cm^2/Vsec$) and the GaAs two dimensional electron gas (≈6000$cm^2/Vsec$) are much different even at room temperature. Note that the ionized donor and acceptor concentrations at room temperature in the AlGaAs layers are both $1.5x10^{18}/cm^3$. As a result, the conductivity in the p-MODFET at room temperature is dominated by an AlGaAs conduction term (≈$1.2x10^{13}/cm^3$) rather than by a GaAs channel

term ($\approx 10^{12}/cm^3$), while at 77°K, only the two dimensional hole gas contributes to the Hall-effect measurement. This is because of the freeze-out of the acceptors in the AlGaAs layer (less than 10 % of ionized acceptors at room temperature are ionized at 77°K) and also because of the mobility difference between the two layers (the two dimensional hole gas mobility is approximately 20 times higher than p-AlGaAs hole mobility). In the n-MODFET case, the parallel conduction has much smaller contribution to the resultant mobility and electron concentration because of the large mobility difference in the channel and the parasitic channel at both room temperature and 77°K. Another noticeable point is that the light effect on the n-MODFET is significant at 77°K as expected. This is caused by "DX centers"[LANG 79],[MORGAN 86],[THEIS 86] in n-type $Al_xGa_{1-x}As$ layers. This undesirable effect can be avoided in several ways, which will be discussed in Chapter 5. In summary, the Hall-effect measurement results at 77°K confirmed that with the target structures shown in Figure 3.2 very good mobility and carrier concentrations are possible for both n and p-channel MODFETs for complementary circuit applications.

	2D Hole Gas (p-MODFET)		2D Electron Gas (n-MODFET)			
			Light		Dark	
	300°K	77°K	300°K	77°K	300°K	77°K
Mobility ($cm^2/V*sec$)	137	3,629	6,804	118,430	6,805	108,908
n_s (cm^{-2})	$1.39x10^{13}$	$8.9x10^{11}$	$8.4x10^{11}$	$1.02x10^{12}$	$8.18x10^{11}$	$5.96x10^{11}$
$R_\square$ ($\Omega/\square$)	11.8 k	1.93 k	1,092	51.7	1,121	96.2

Table 4.1 Hall-effect measurement results of two dimensional electron gas and two dimensional hole gas in modulation doped stuctures.

4.3 TRANSISTOR I-V CHARACTERISTICS

4.3.1 Transconductance and Maximum Drain Current

Typical I-V characteristics of both p- and n-channel MODFETs with 2μm gate lengths are shown in Figure 4.1. Typical transconductances at 300°K are 2.5-3mS/mm and 85-90 mS/mm for p-channel MODFETs and n-channel MODFETs, respectively. Maximum drain currents are typically 1.7mA/mm and 55mA/mm for p-MODFETs and n-MODFETs, respectively. Both transconductance and maximum drain current ratios between n-MODFET and p-MODFET are about 30 at room temperature. The maximum drain current ratio can be reduced to a factor of 10 by making the transistor width ratio W(p)/W(n) to be three. At cryogenic temperatures, the ratio is expected to improve further because of the dramatic increase of the hole mobilities. At 77°K, characteristics of p-MODFETs improve dramatically as expected: the extrinsic transconductance increases to about 8m S/mm and the maximum drain current to be 5.3mA/mm as illustrated in Figure 4.2. On the other hand, n-MODFETs at 77K showed little improvement in terms of transconductance and maximum drain current , even when measured under illumination. When the n-MODFET sample is cooled down to 77K in the dark, the devices show typical drain current collapse caused by "DX centers" in the AlGaAs layers. This will be discussed in detail in section 4.3.2. Both ratios of transconductance and maximum drain current between p-MODFET and n-MODFET become about 10 at 77°K, thus making the drain current ratio 3 if the FET width ratio W(p)/W(n) is chosen to be 3, and if the devices are operated under illumination. Since the maximum drain current is the most important propagation delay determining factor in digital circuit applications rather than small signal transconductance, it is worth further discussion of our results. If the transistor width ratio between p-MODFET and n-MODFET is chosen to be unity, our results show that the maximum drain current ratio at 77°K is 10, while reported numbers from other labs are typically 15 for conventional MODFET structures. This does not mean that our p-MODFET is better than these outside results, but that our n-MODFET did not show any significant improvements when it was cooled to 77°K. Typically, n-MODFETs show about a 50% improvement upon cooling to 77°K when the DX center problem is not severe. Thus, our results would have been close to these typical values, showing maximum drain current ratio of 10 at 77°K if our DX-center problem was alleviated by decreasing the Aluminum compound ratio to 25% instead of the 30% value used in our structures.

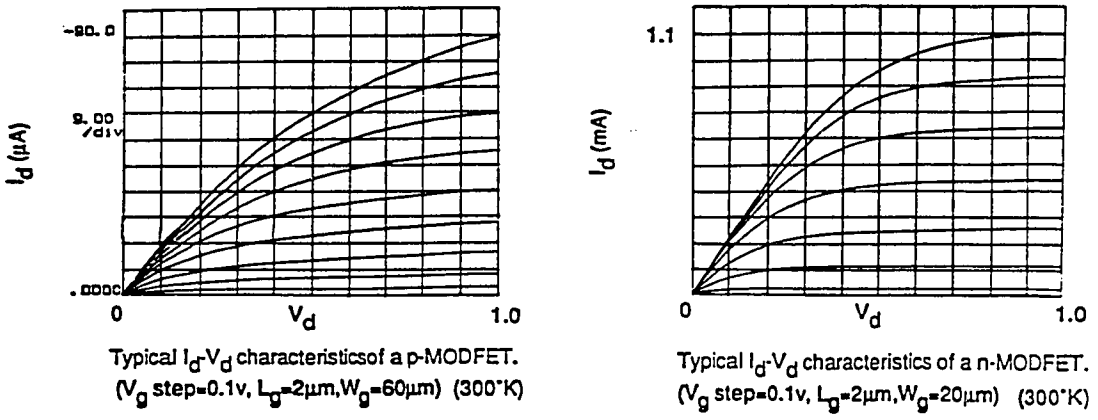


Figure 4.1 Typical I_{DS}-V_{DS} Characteristics of p-channel and n-channel MODFETs Measured at 300°K. The maximum forward gate voltages are +1v and -1v for n- and p-MODFETs respectively.

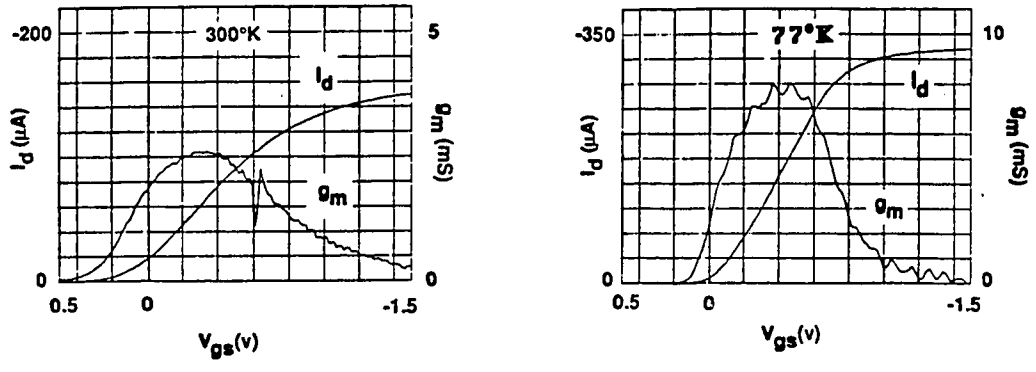


Figure 4.2 Transconductance and I_{DS}-V_{GS} Characteristics of p-channel MODFETs at 300°K (a) and at 77°K (b).

4.3.2 Drain Current Collapse

When an n-MODFET is cooled to 77°K in the dark, they often reveals the so-called, drain-current collapse, as shown in Figure 4.3. This phenomenon occurs when electrons in the channel acquire sufficient kinetic energy to surmount the AlGaAs/GaAs interface barrier and become trapped on the DX-centers in the silicon-doped AlGaAs layer. Normal characteristics are regained by shining a light on the cooled sample, thus detrapping the electrons from the DX-centers. Although our structure was designed to have 30% Aluminum in the silicon doped AlGaAs layer and photo-luminescence from the sample shows 28% Aluminum, which should be in safe range to avoid drain-current collapse, our n-MODFETs show drain current collapse. The density of deep levels associated with DX centers are reported to increase as the silicon donor concentration increases[ISHIKAWA 86]. The silicon donor concentration in our sample is relatively high($1.5x10^{18}/cm^3$). Thus, in order to alleviate the DX-center related problems, one has to reduce both the aluminum and silicon concentrations in the AlGaAs layer. This places relatively stringent constraints upon the structural device design. An alternative approach is to add Indium in the channel layer and make a so-called, pseudomorphic n-MODFET, whose name comes from the fact that the AlGaAs and InGaAs (or GaAs and InGaAs) layers are strained. P-channel MODFETs do not reveal current collapse nor PPC(persistent photo conductivity) effect because p-type dopants behave well in AlGaAs and do not create deep trap levels at high Aluminum concentrations.

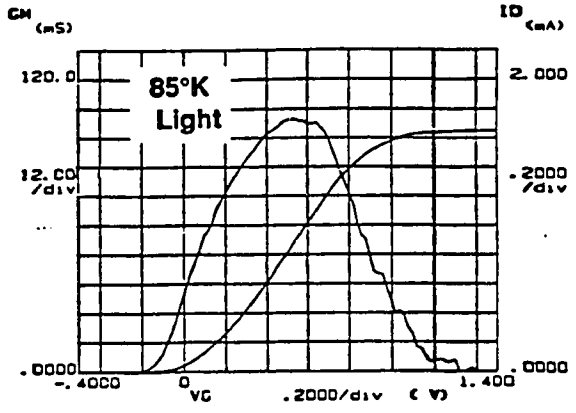
4.3.3 Subthreshold Current

The subthreshold current in MODFETs has not been studied extensively so far. However, its operational principle is the same as that of a MOSFET. The subthreshold current should be expressed as [BREWS 78],

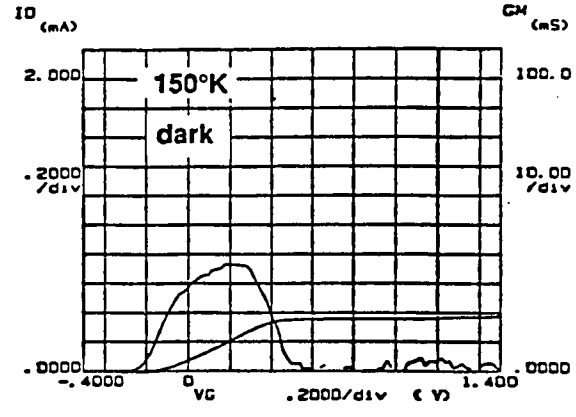
$$I_D = \mu_n\left(\frac{Z}{L}\right)\frac{aC_i}{2\beta^2}\left(\frac{n_i}{N_A}\right)^2\left(1-e^{-\beta V_D}\right)e^{\beta\psi_s}\left(\beta\psi_s\right)^{-1/2}, \qquad (4.1)$$

where C_i ($=\varepsilon_i/d$) is the insulator capacitance, $\beta=q/kT$, $a=\sqrt{2}\,(\varepsilon_s/L_D)/C_i=2(\varepsilon_s/\varepsilon_i)$, and ψ_s is the surface potential, which is expressed as,

(a)



(b)



(c)

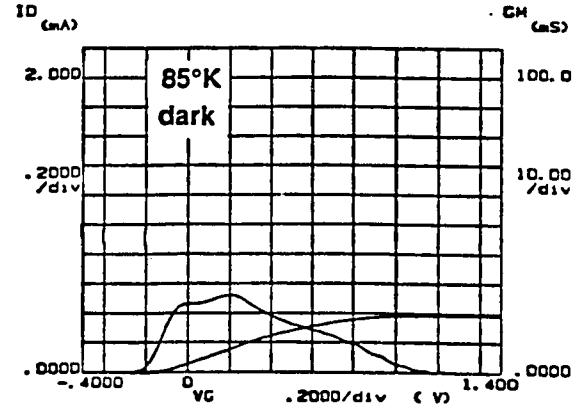


Figure 4.3 Drain-Current Collapse of an n-MODFET at low temperatures. (a) Cooled down to 77°K with light on,(b) cooled down to 150°K in the dark, (c) cooled down to 77°K in the dark.

$$\psi_s = (V_G - V_{FB}) - \frac{a^2}{2\beta}\left\{\left[1+\frac{4}{a^2}(\beta V_G - \beta V_{FB} - 1)\right]^{1/2} - 1\right\}.$$

Using this equation, we can define the gate-voltage swing S [SZE 81] as

$$S \equiv \ln 10 \cdot dV_G/d(\ln I_D). \tag{4.2}$$

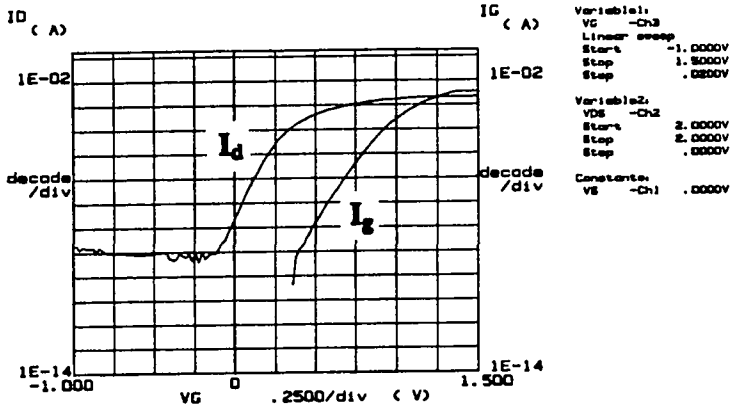
For $a >> (C_D/C_i)$, S can be approximated as,

$$S \approx (kT/q) \ln 10 \cdot (1+ C_D/C_i). \tag{4.3}$$

The background doping of MBE grown MODFET structures is of the order of low 10^{14} cm^{-3} and the samples grown in our system have 1 to 1.5 x $10^{14}cm^{-3}$ carbon background, which makes the above approxmation valid. Experimental subthreshold characteristics of one of our n-MODFETs is shown in Figure 4.4. The measured gate-voltage swings of the n-MODFETs are close to the value of kT/q at three different temperatures, i.e., 300°K, 150°K, and 77°K as shown in Figure 4.5. The interesting point to notice is that in MODFETs, at least in the gate-recessed structure; short channel effects are less pronounced than in MOSFETs. In Si MOSFETs, when the substrate doping level is 1x 10^{15} cm^{-3}, there is no short channel effect in the subthreshold region and the gate-voltage swing value is close to kT/q and the device shows good pinch-off characteristics. When the substrate doping is 1 x $10^{14}cm^{-3}$, then even a 7μm gate length Si MOSFET starts to show drain-induced-barrier lowering and poor pinch-off characteristics. In shorter gate length devices these problems are much worse, as shown in Figure 4.7. The reason n-MODFETs show better subthreshold characteristics with the identical light substrate doping comes from their structure. The two-dimensional electron gas is very thin between gate-to-source and gate-to-drain region as illustrated in Figure 4.6.

Subthreshold currents of p-channel MODFETs also show an exponential dependence on gate voltage, but the swing parameter, S, values are greater than kT/q by a factor of two. Although the buffer layer is lightly doped p-type, the entire layer(≈1μm) should be depleted because of the low doping. Thus, the mechanism should be similar to the n-MODFET case, yielding the swing parameter close to kT/q. The mechanism that gives rise to this high swing parameter in p-MODFETs is unknown.

(a)



(b)

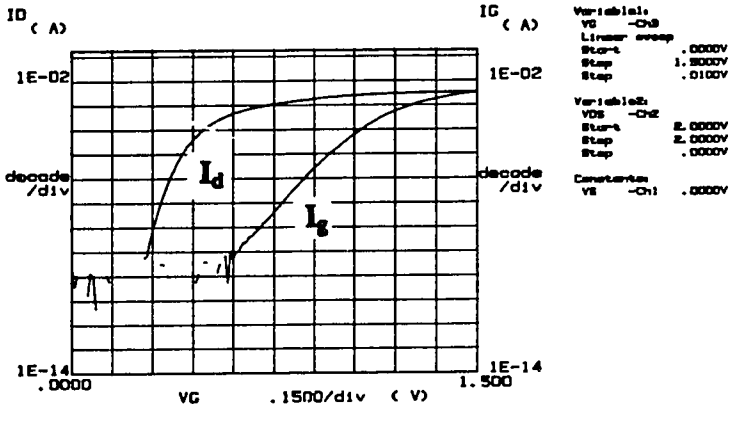


Figure 4.4 Subthreshold characteristics of an n-MODFET. Measured at (a) 300°K, (b) 77°K.

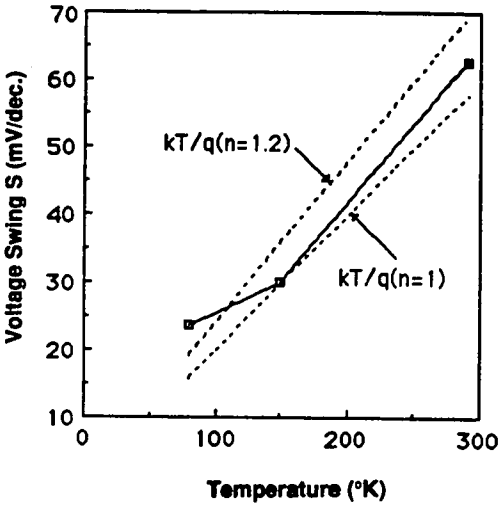


Figure 4.5 Gate-voltage swing of an n-MODFET versus temperature.

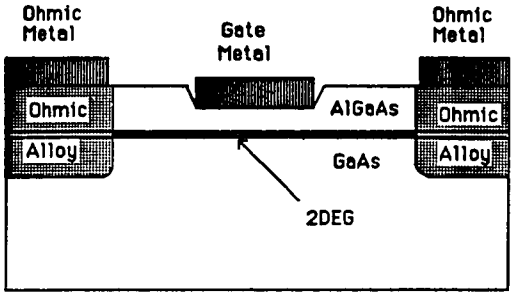


Figure 4.6 An n-MODFET structure.

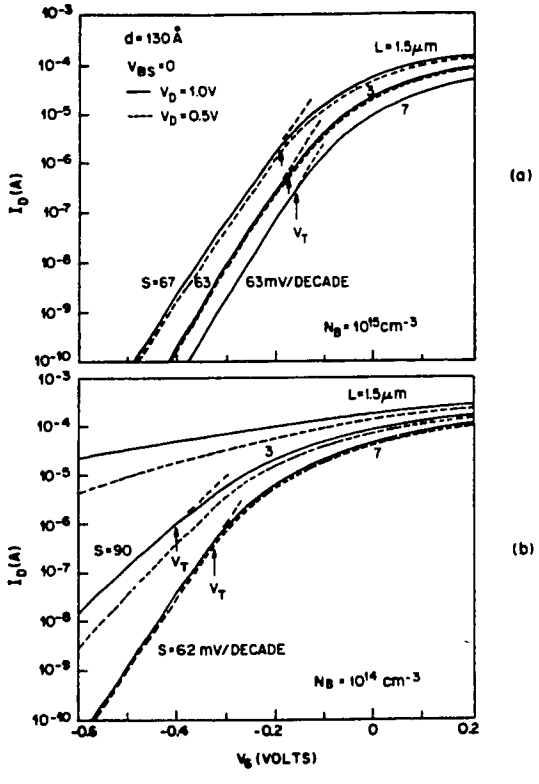


Figure 4.7 Gate-voltage swing of a MOSFET (After S.M.SZE). The substrate doping levels are (a) $N_A=10^{15}$ cm^{-3} and (b) $N_A=10^{14}$ cm^{-3} respectively.

4.3.4 Velocity saturation

The drain current vs gate voltage characteristics in Figure 4.8 show that the drain current of an n-channel device is linearly proportional to (V_g-V_{th}) while the drain current of a p-channel device is proportional to $(V_g-|V_{th}|)^2$ over a wide range of gate voltages. As the simple gradual channel model calculation indicates, these I-V characteristics show that the electrons in an n-MODFET are velocity-saturated while the velocity of holes in p-MODFETs is still in non-saturated velocity regime. These results suggest that further gate length reduction of the devices will still greatly enhance p-MODFET performance, however , a significantly less enhancement is expected for n-MODFETs, as compared to the long channel devices.

These results suggest a simple analytical circuit model for complementary MODFETs, consisting of a velocity saturated n-MODFET with a linear relationship between drain current and gate voltage and non-saturated velocity p-MODFET with a square law relationship between the drain current and the gate voltage.

(a)

(b)

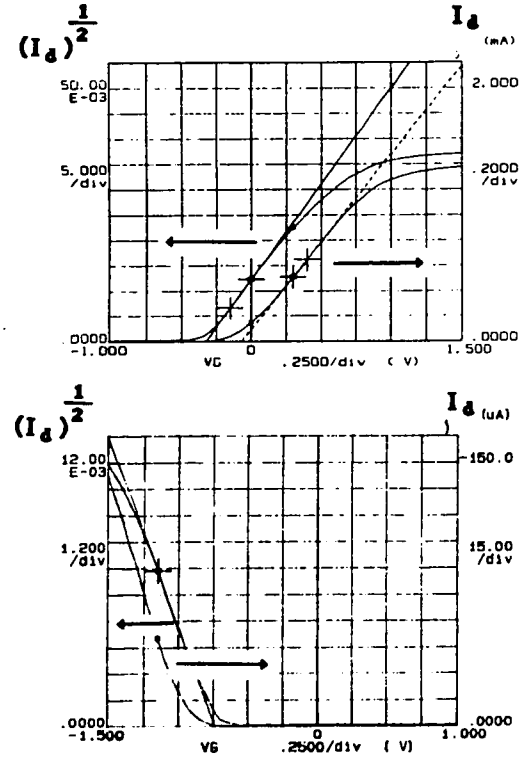


Figure 4.8 Drain current dependence on gate voltage. Right vertical axis indicates drain current and left vertical axis indicates square root of the drain current in both (a) n-channel MODFET and (b) p-channel MODFET.

4.4 CIRCUIT PERFORMANCE

In this section, inverter characteristics and ring oscillator results for complementary MODFETs are discussed. The gate length of the devices in this section is 2μm which was the value selected for the initial circuit fabrication and goes through this entire chapter. As pointed out in the previous section, significant improvement is expected for shorter gate length p-MODFETs and is one of the enhancements utilized in the second generation circuits described in Chapters 5 and 6.

4.4.1 Inverter Characteristics

The inverter transfer curves and short-circuit current at various supply voltages measured at room temperature are shown in Figure 4.9. Overall, the inverter characteristics show a sharp transition, as expected for a complementary inverter circuit. The high output level(logic "1") is slightly lower than the supply voltage because of the subthreshold tail current of the n-channel MODFET. Correction of this effect is just a matter of adjusting the threshold voltages such that at the desired operating temperature, the threshold voltage shift with temperature has been appropriately taken into account. The optimum device design is a compromise of the device threshold voltage such that it satisfies two contradictory demands : (i) that the threshold voltage is large enough to minimize static current, and (ii) that lower threshold voltage maximizes the drain current. At cryogenic temperatures, the inverter characteristics of the present device should improve because the threshold voltage of the n-channel MODFET increases by 0.2 to 0.3 volt when it is cooled to 77°K. Nonetheless, Figure 4.9 shows a high noise immunity of about 80% through a wide range of supply voltages, between 0.3 and 1.5 volt.

The peak short-circuit current and the stand-by current of an inverter circuit are plotted in Figure 4.10. Note also that the short-circuit current peak is generally a strong function of threshold voltages, although the figure shows the peak current dependence on supply voltage with a "constant" threshold voltage. The stand-by current of the logic "1" output voltage shows a sharp increase when the supply voltage becomes greater than 1 volt. This is due to the on-set of gate leakage current through the gate of the p-channel MODFET. The gate leakage current becomes almost half of the peak short-circuit current level at a

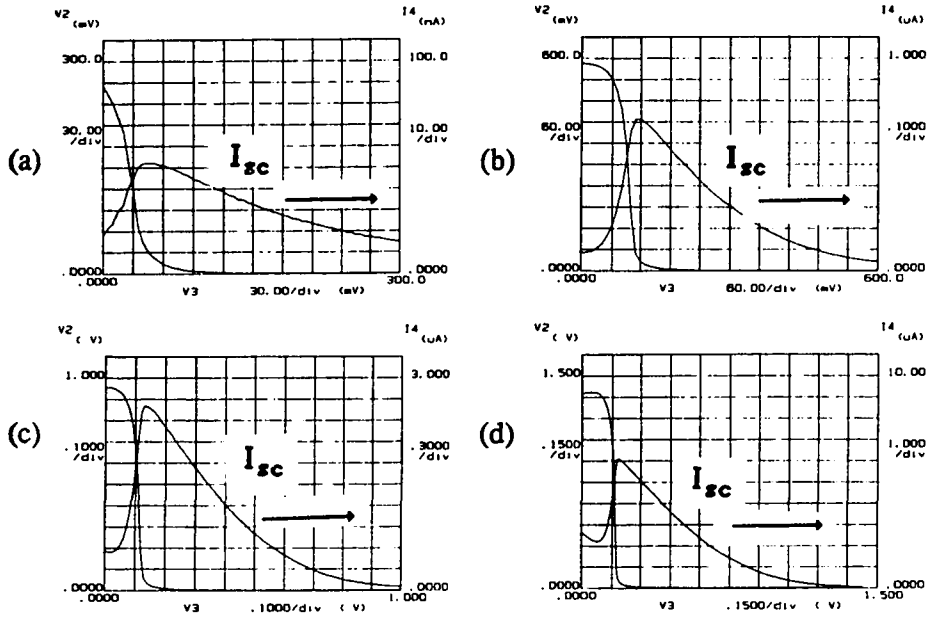


Figure 4.9 Inverter transfer characteristics and short-circuit currents at various supply voltages : (a) Vdd=0.3 volt, (b) Vdd=0.6 volt, (c) Vdd=1.0 volt, and (d) Vdd=1.5 volt.

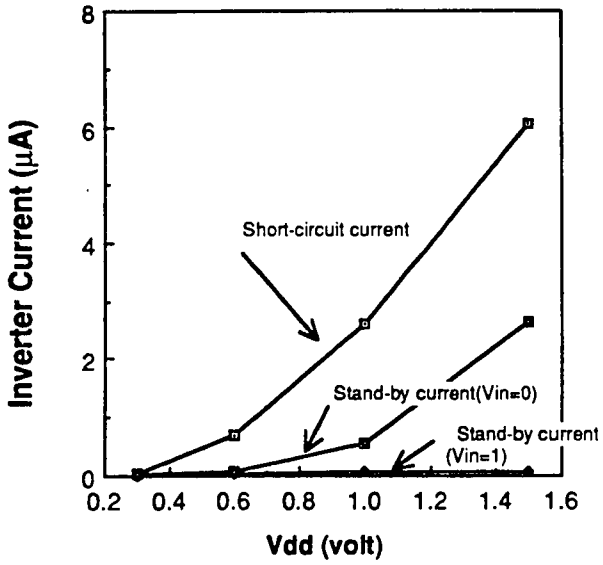


Figure 4.10 Peak short-circuit-current and satnd-by currents of a complementary MODFET inverter as a function of power supply voltage.

supply voltage of approximately 1.5 volt. The gate leakage current through the gate of the n-channel MODFET cannot be seen in the Figure 4.9 because the current has been measured at the voltage source end not at the ground end of the circuit. If we measure the current at the ground end of the circuit, we do observe the gate leakage current through the n-MODFET gate, however we lose the information of the gate leakage current through the p-MODFET gate. The short-circuit current will not be affected by the choice of the node at which the current is measured, as long as the the supply voltage is small enough not to cause a static current that is comparable to the peak short-circuit current.

4.4.2 Ring Oscillators

Seventeen stage ring oscillators were fabricated and measured to study the dynamic behavior of complementary MODFET circuits. The gate length of each device is 2μm. The gate widths of each inverter stage are 20μm and 60μm for n-channel and p-channel MODFETs, respectively. The measured propagation delay and power dissipation for the ring oscillator are plotted in Figure 4.11. Although the low power-dissipation nature of complementary MODFET circuits was clearly demonstrated in these circuits, the propagation delay is certainly not small enough to convince anyone that complementary MODFET is a useful "high speed" digital technology, even with the additional advantages of low power dissipation and high noise margin. The main factor that limited the high speed in these circuits was the low drain-current capability of the p-MODFETs. Reducing the channel length gives p-MODFETs a dramatic improvement in their performance, since the carriers are still not velocity saturated as described in section 4.3.4. This suggests making the gate lengths shorter. Other options, in addition to reducing the gate length, to gain higher p-MODFET performance are described in Chapter 5.

Wide operational voltage range: The ring oscillators described above demonstrated operation from 0.18 to 5 volts supply voltage. The low end, 0.18 volt, is only twice as high as the theoretical limit of complementary FET circuits[SWANSON 72]. The ring oscillator circuits also operate at large supply voltages, well above the on-set voltage (V_t) of gate leakage current. The internal voltage swing of the circuit is governed by a voltage divider formed by the n-MODFET and the source resistance of the p-MODFET, sandwiched by the Schottky diode. Since the source resistance of the p-MODFET is about an order of magnitude higher than the on-resistance of the n-MODFET, the high level of the internal voltage swing above V_t becomes approximately the Schottky diode forward voltage (V_F) of the p-MODFET gate, and the low level of the internal

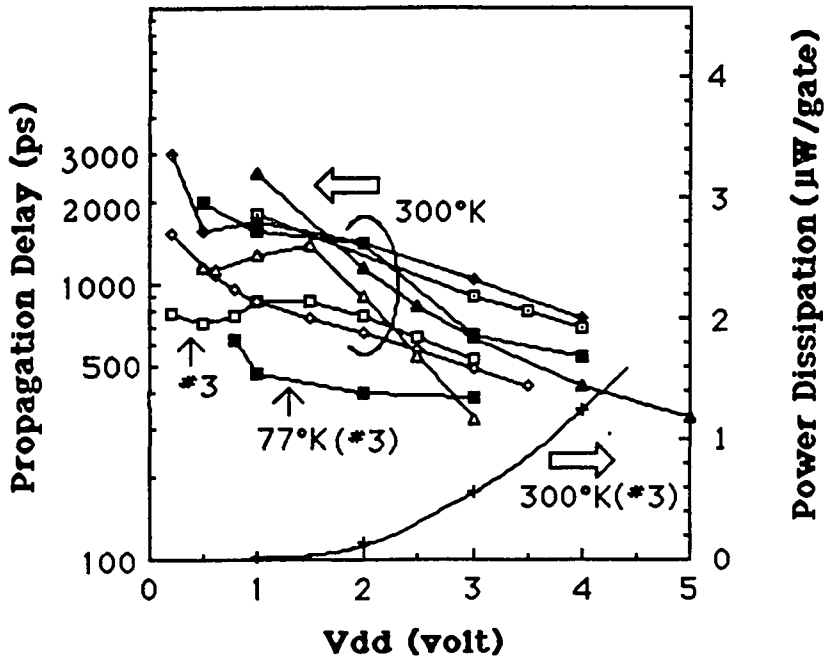


Figure 4.11 Propagation delay and power dissipation as a function of power supply voltage.

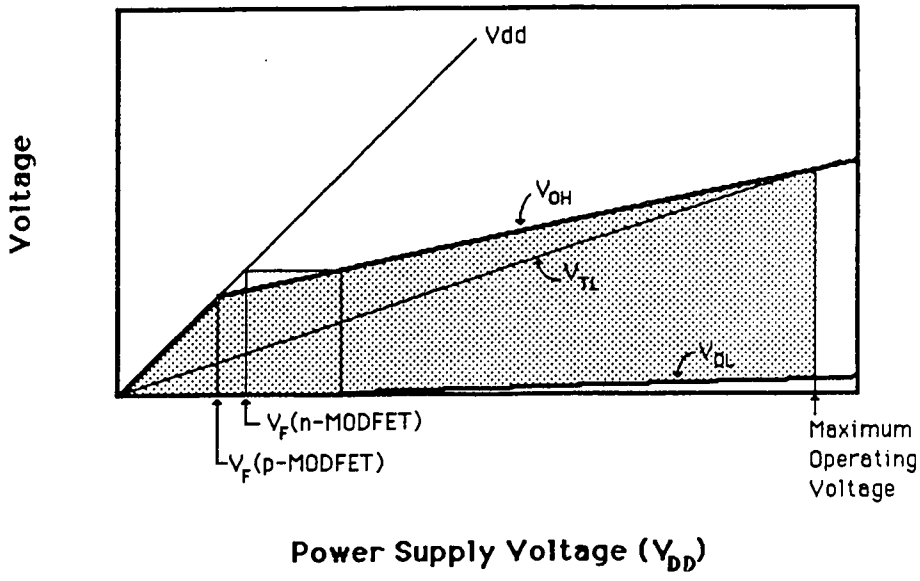


Figure 4.12 V_{OH}, V_{OL} and V_{TL} as a function of the power supply voltage.

voltage swing becomes nearly equal to zero (ground level) because the V_F of the n-MODFET is larger than that of p-MODFET. This result is indirectly confirmed by the observation of the output signal of the ring oscillators. Thus, the maximum operational voltage is found approximately where the logic threshold voltage, V_{TL}, crosses the V_{OH} of the internal voltage swing, as schematically illustrated in Figure 4.12. As we have seen previously in Figure 4.9, the logic threshold voltage, V_{TL}, of the inverter circuit is off-set from the mid-point value of V_{dd} toward ground level, making the V_{TL} slope on the supply voltage small. Hence, the supply voltage at the cross-point with the V_{OH} line becomes high. However, in spite of the large operating voltage range and the improved propagation delay time at higher supply voltages, the proper operational voltage of a complementary MODFET circuit should be limited to the region where there is no serious gate leakage current, and where we can make full use of the advantages of complementary circuits: low power dissipation, rail-to-rail voltage swing, and high noise margin. In this regard, the present circuits with 2μm gate length demonstrated all of the above advantages, but are not satisfactory in speed, even at cryogenic temperatures. This suggests that the complementary approach may still be valid, but improvements must be realized in the p-channel MODFETs in order to attain a useful high speed technology.

4.5 SUMMARY

We have demonstrated that both p-channel and n-channel MODFETs, grown by the selective MBE technology, have reasonable characteristics at room temperature. We observed, however, that the n-MODFET at cryogenic temperatures in the dark suffers drain current collapse. This can be avoided in several ways. The pseudomorphic structure approach was chosen in this investigation because it provides both improved structures and alleviates the DX center problems. These are discussed in Chapters 5 and 6. We also demonstrated that the holes in p-MODFETs are still not velocity saturated and that significant improvements are expected by making the channel length shorter ($\approx$2μm used here). Abrupt inverter transfer characteristics have been confirmed. Realization of very low static current has also been demonstrated when the circuit is operated at reasonably low supply voltages where small gate leakage current is expected. The seventeen stage ring oscillator demonstrated operation over a wide voltage range with extremely low power dissipation. The relatively large propagation delay suggests that p-MODFET improvements in drain current capability are essential and this is the major topic of the next chapter.

Chapter 5

STRUCTURAL IMPROVEMENTS

5.1 INTRODUCTION

In this chapter, various structural improvements, suggested by the initial results in the previous chapter, are developed. The first three sections (5.2, 5.3, and 5.4) deal with p-channel MODFET improvements, because they are the major limiting factor of the C-MODFET circuit performance. The relatively slow switching speed in our initial circuits was due to the low drain current capability of p-MODFETs, even at cryogenic temperatures, as we observed in the previous chapter. In order to improve the sheet resistance of the two dimensional hole gas, (2DHG), we have taken three approaches; a double heterojunction approach (section 5.2), a doped-channel approach (section 5.3), and a strained quantum-well approach (section 5.4). Each of the first two approaches improves the p-channel drain current capability by increasing the carrier concentration in the channel. The third approach tries to improve the hole mobility, while maintaining the high carrier concentration with a novel structure using new materials combinations, such as strained GaAs/InGaA/AlGaAs layers. Section 5.5 compares these three approaches and summarizes the p-MODFET improvements. The final topic of structural improvements for the pseudomorphic n-MODFETs as a solution to DX-center related problems under cryogenic temperature operation is described in section 5.6. Other improvements, such as optimization of the lithographic process conditions for the short channel (1μm) devices, are not explained explicitly because there is nothing substantially new to be discussed, but it should be pointed out that it plays an important role for improving the performance of both p- and n-MODFETs.

5.2 DOUBLE HETEROJUNCTION P-MODFET

The double heterojunction p-MODFET approach is a straight forward way to achieve high carrier concentration while keeping the high carrier mobility[YOH 86]. The approach is analogous to the double heterojunction n-MODFET[INOUE 84]. The structure has two layers of Be-doped AlGaAs on each side of the channel, supplying carriers from both

sides to the channel. In order to optimize the structure, we have measured van der Pauw samples with different channel thicknesses. Then, applying these results to FETs, we have confirmed the superiority of the double heterojunction p-MODFET in both maximum drain current and maximum transconductance over the single heterojunction p-MODFET.

5.2.1 Hall-Effect Measurement

The double hetero-junction structure for the Hall samples consists of the following layers : 5,000Å of undoped GaAs, 2,000Å of undoped $Al_{.4}Ga_{.6}As$, 250Å of $1.7x10^{18}$ cm^{-3} Be doped p-$Al_{.4}Ga_{.6}As$, 75Å of undoped $Al_{.4}Ga_{.6}As$, 100-400Å of undoped GaAs, 75Å of $Al_{.4}Ga_{.6}As$, 500Å of $1.7x10^{18}cm^{-3}$ Be- doped p-$Al_{.4}Ga_{.6}As$ and 50Å of $2.8x10^{18}$ cm^{-3} Be-doped p-GaAs. This structure is illustrated in Figure 5.1. The hole mobility and the hole concentration data are plotted in the Figure 5.2 as a function of channel layer thickness. The mobility of the structure, measured by the van der Pauw method is fairly constant over the wide range of the channel thickness and decreases only when the channel layer thickness falls below 100Å. This result may be attributed to increased surface roughness scattering. The measured mobility at 77°K is 3200 $cm^2/Vsec$ at the plateau, which is about 90% of that of a single heterojunction modulation-doped structure. The slight decrease in mobility may be indicative of the increased carrier scattering at the bottom hetero-interface. The increased carrier concentrations of $2\text{-}3x10^{12}$ cm^{-2} are far more than enough to cancel the slight mobility degradation. This yields about half of the sheet resistance compared with the single heterojunction case. The sheet resistance values are fairly constant over the quantum well range of our experiment, as shown in Figure 5.3. This result is promising to achieve an improved p-MODFET with an increased maximum drain current by a factor of two.

5.2.2 FET Performance

P-channel, double heterostructure MODFETs have been fabricated with conventional GaAs processing technology. Wafer preparation procedures for the MBE growth and the growth conditions are the same as those described in chapter 4. The quantum well thickness for the double heterojunction p-MODFET is 200Å and all the other parameters are the same as the Hall sample structures shown previously in Figure 5.1. We chose a moderate quantum well thickness of 200Å to make allowance for process tolerances as much as possible for our first trial, but a thinner well (e.g.100Å to 150Å) would be better in order to maximize the transconductance and provide a fully optimized structure.

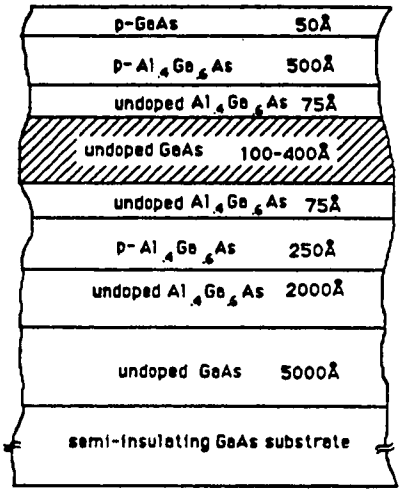


Figure 5.1 Cross sectional view of a double heterojunction p-MODFET

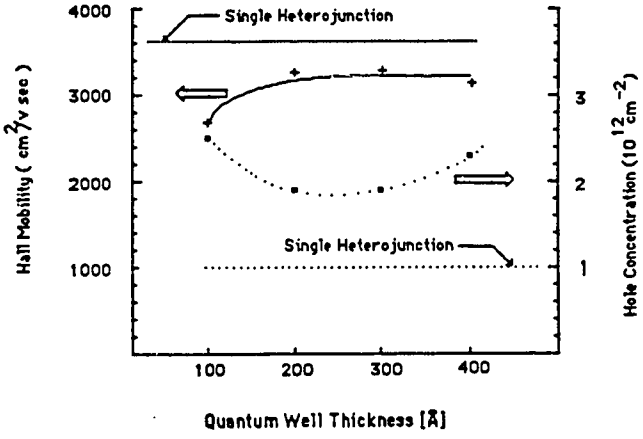


Figure 5.2 Hole mobility of double heterojunction modulation doped structure.

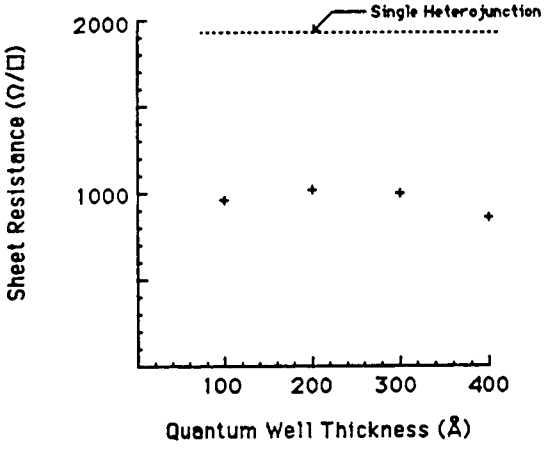
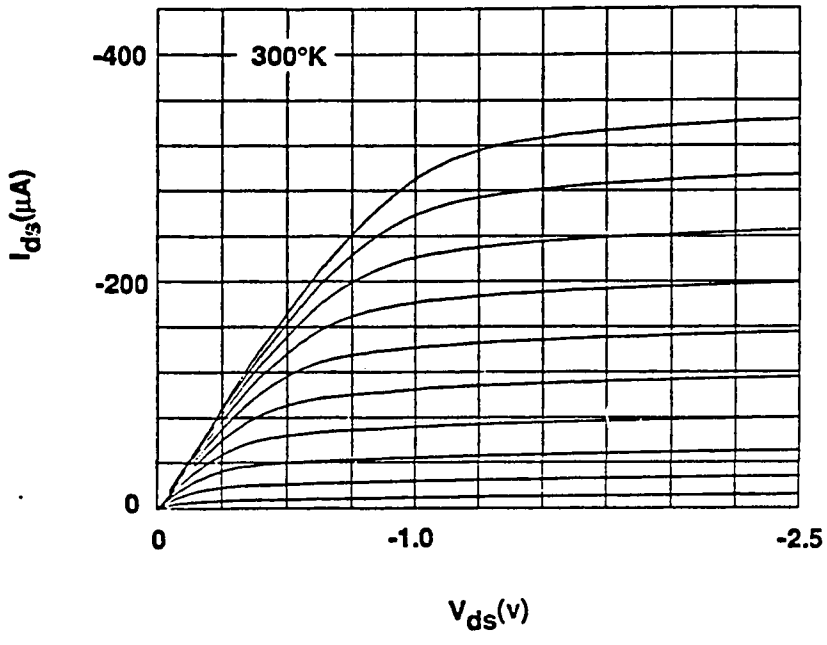
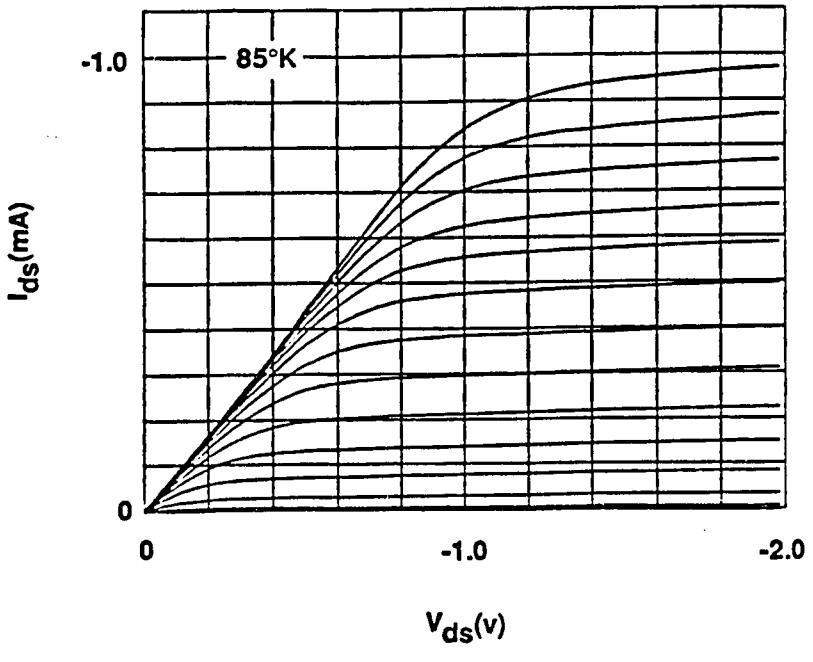


Figure 5.3 Sheet resistance of double heterojunction p-type modulation doped structures.



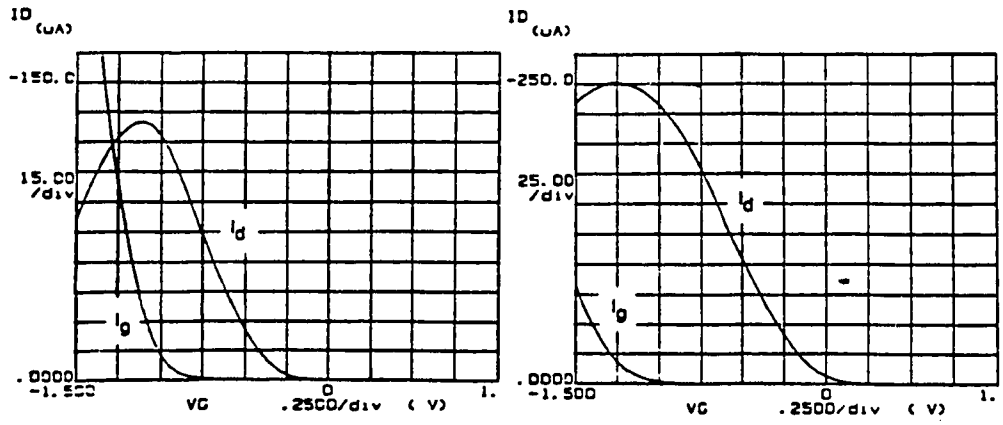
(a)



(b)

Figure 5.4 I_{ds}-V_{ds} relationship of a double heterojunction p-MODFET at (a)300°K and at (b) 85°K. Maximum forward gate voltage is -1.3v (-0.1v step).

The p-channel MODFET showed good pinch-off characteristics, even at room temperature as well as at 77K, as shown in Figure 5.4. The I_{ds}-V_{gs} and I_{gs}-V_{gs} characteristics at 300°K of a single heterojunction p-MODFET and a double heterojunction p-MODFET are compared in Figure 5.5. This shows that higher gate voltages can be applied to the double heterostructure MODFETs without causing severe gate leakage current. The amount of gate voltage gained for the double heterojunction structure roughly corresponds to a voltage drop across the channel layer at the threshold voltage condition. This result implies that the double heterostructure approach significantly reduces the gate leakage problem, which is inherent to all types of AlGaAs/GaAs MODFETs. Both transconductance and I_{ds}-V_{gs} characteristics of the double heterojunction p-MODFET at 300°K and at 85°K are



(a) (b)

Figure 5.5 A comparison of I_{ds}-V_{gs} and I_{gs}-V_{gs} relations between a single heterojunction p-MODFET (a) and a double heterojunction p-MODFET(b) measured at 300°K. Device sizes are identical (W/L=60μm/2μm) in both structures.

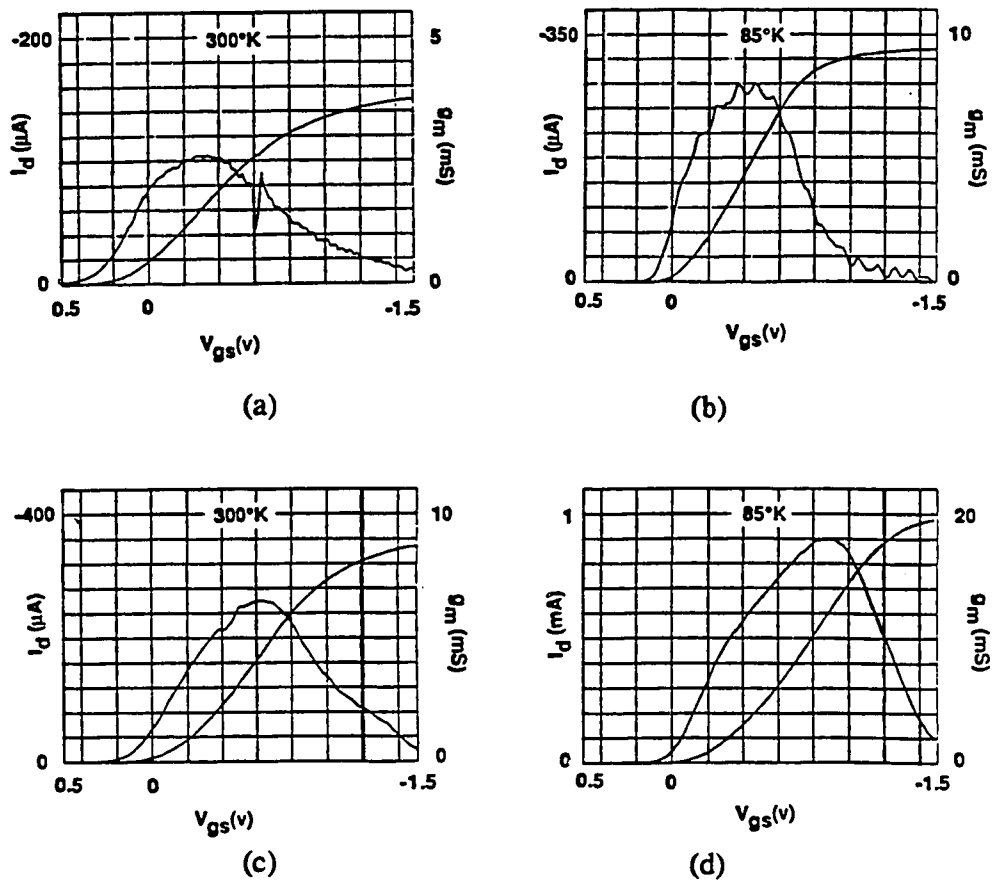


Figure 5.6 Transconductances and I_{ds}-V_{ds} characteristics of a single heterojunction p-MODFET at (a) 300°K, (b) 85°K, and a double heterojunction p-MODFET at (c) 300°K and (d) 85°K.

illustrated in Figure 5.6, where single heterojunction p-MODFET results are also shown as a comparison. From this figure, it is obvious that both tranconductance and the maximum drain current have been doubled at both room temperature and at 85°K by using a double heterostructure. The peak transconductances (7.8mS/mm at 300K, 19mS/mm at 77K at a drain voltage of 1.0 V) are not as high as the highest record [LEE 87], first, because of the long gate length (gate length=2μm, source-drain distance=6μm) and second, because of the measurement condition (V_{ds}=1V)* and third, because the g_m of an enhancement mode MODFET, which we use for C-MODFET, tends to be lower than for a depletion mode device. The threshold voltage of a double heterojunction p-MODFET

* It is commonly observed that the higher the drain voltage, the higher the transconductance. Thus, one tends to report higher transconductances using unreasonably high drain voltage conditions compared with the practical supply voltage which is limited to be low by the Schottky gate leakage current.

increases by 0.1 volt upon cooling to cryogenic temperatures, while a single heterojunction p-MODFET shows a threshold voltage increase of 0.2 volt. From Figure 5.6, it is clear that both drain current capability and the maximum transconductance, g_m, have been doubled by employing the double heterojunction in making the p-MODFET. An optimized short channel double heterostructure p-MODFET will lead to complementary circuits with switching speeds increased by a factor of two.

Source resistance and contact resistance : The measured source resistance and contact resistance of a double heterojunction p-MODFET are listed in Table 5.1 below, together with the data of a single heterojunction p-MODFET and a self-aligned p-MODFET using ion-implantation[CIRILLO 85],[OE 86]. Table 5.1 shows that a double heterojunction p-MODFET has the smallest gate-to-source resistance among these various p-MODFET structures. Since the souce resistance consists of contact resistance and gate-to-source resistance, the double heterojunction MODFET has a potential of having the lowest source resistance and high transconductance when the contact resistance is improved by optimizing the ohmic contact conditions to the level of self-aligned structure case.

ITEM		THIS WORK (2μm)		REFERENCE (1μm)	(*)NTT (**)Honeywell
		Single hetero-structure	Double hetero-structure	Single hetero-structure	Self-aligned Structure
$R_\square$ (kΩ/□)	300°K	20	6-7	41 (*)	4.4 (**) 3 (*)
	77°K	2.6	1.0	10 (*)	3.5(**) 3 (*)
R_{gs} (Ωmm)	300°K	40 (20)	12-14 (6-7)	41 (*)	4.4 (**) 3 (*)
	77°K	5.2 (2.6)	2 (1)	10 (*)	3.5 (**) 3 (*)
R_C (Ωmm)	300°K	52-82	7-20	—	14.4 (**) 3-4 (*)
	77°K	56-62	7-20	—	8.9 (**) 3-4 (*)
R_S (Ωmm)	300°K	92-122 (72-102)	19-34 (13-27)	—	18.6(**) 6-7 (*)
	77°K	57-87 (59-69)	9-22 (8-21)	—	12.0(**) 6-7(*)

Data in ( ) are projected values for 1μm spacing.

Table 5.1 Source and contact resistances of various p-channel heterojunction FETs.

Subthreshold current : I_{ds} -V_{gs} characteristics at 300°K and at 85°K are shown in the semi-log plot in Figure 5.7. Measured subthreshold slopes, S^{-1}, are 58 mV/decade at 85°K and 120 mV/dec. at 300°K. These numbers are large compared with the ideal q/kT

value observed for a single heterojunction n-MODFET (Cf. chapter 4). The reason for the large subthreshold slope,S^{-1}, of p-MODFETs (both double and single heterostructures) is unknown. However, the very large ideality factor of the Schottky gate leakage current (Fig.5.7) may be indicative of possible oxide formation between the gate metal (Ti/Pt/Au) and top $Al_{.4}Ga_{.6}As$ layer. When we compare this result with the single heterojunction case (Figure 4.4), one realizes the fact that the short channel effect is greatly reduced in a double heterojunction MODFET. This is presumably because the carriers are confined in the thin layer of the quantum well in the double heterojunction structure.

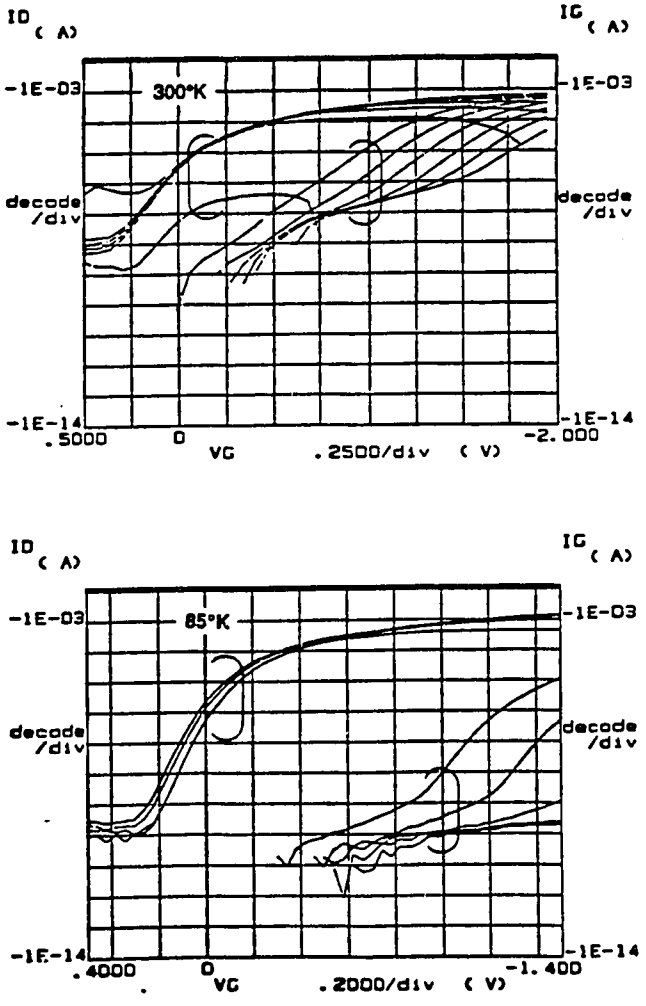


Figure 5.7 I_{ds}-V_{ds} and I_{gs}-V_{ds} characteristics of a double heterojunction p-MODFET

Light sensitivity : Unlike the n-MODFET, p-MODFETs do not suffer from serious drain current collapse at cryogenic temperatures. However, p-MODFETs do show some degradation in both maximum drain current and transconductance if the sample is cooled down to 77°K as shown in Figure 5.8. The threshold voltage change of a double

heterojunction p-MODFET is 0.43 volt toward minus direction when it is cooled in the dark. When we recall the threshold voltage change in the light is 0.1 volt, this large voltage change in the negative direction together with the slight degradation of drain current and transconductance, is indicative of the existence of either surface states or interface states at the interface between epi-layer and the substrate.

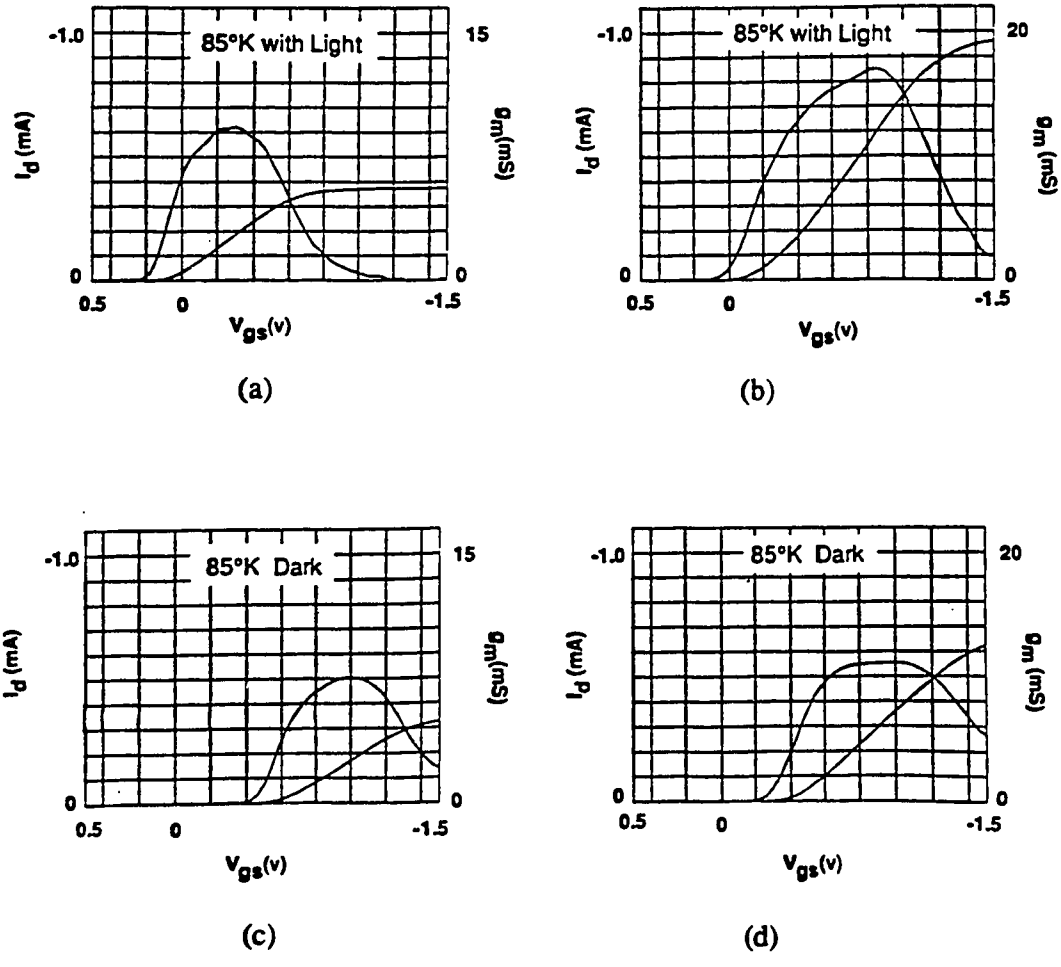


Figure 5.8 A "soft" drain-current collapse of p-MODFETs at 85°K in the dark: I_{ds}-V_{ds} and I_{gs}-V_{ds} characteristics of a single heterojunction p-MODFET cooled down to 85°K (a) under light and (c) in the dark, and double heterojunction p-MODFET (b) cooled down to 85°K under light and (d) in the dark.

5.2.3 Section summary

In summary, we have investigated the double heterojunction p-channel MODFET structure as one approach to improve the p-channel MODFET performance and found that the double heterojunction p-MODFETs improves both drain-current and the maximum transconductance by a factor of two. In addition, the maximum forward gate voltage is substantially increased, which widens the operating voltage range, hence greater noise margins. Table 5.2 below summarizes the electrical measurements of the double heterojunction p-MODFET (W/L=60μm/2μm). If the structure is optimized to achieve a high yield for a certain level of integration, this structure will drastically improve complementary MODFET performance.

ITEM		300°K	150°K (Dark)	85°K	
				Dark	Light
Id max		350μA	600μA	750μA	1mA
g_m (mS/mm)	g_m	6.5	10.7	11	18
	g_{m0}	7.8	13.6	14.5	30(60)
V_{th} (v)	linear	-0.14	-0.467	-0.460	-0.30
	sqrt	0.16	-0.196	-0.270	0.04
R_o(Ωmm)		184	—	—	65.3

Table 5.2 Summary of electrical characteristics of a doble heterojunction p-MODFET.

5.3 STRAINED SINGLE QUANTUM WELL P-MODFET

5.3.1 Introduction

As an alternative approach to enhance p-MODFET performance, we have focused an effort on a study of the (InGa)As/GaAs and (InGa)As/AlGaAs strained-layer single-quantum-well (SSQW) structures. Study on the strained (InGa)As/GaAs system has focused on the strained-layer superlattices[OSBOURN 82],[Schirber 85], in which the effective mass of light holes, of 0.14 m_0, has been measured, where m_0 denotes electron static mass in vacuum. A strained single quantum well p-MODFET [DRUMMOND 86] has been reported with a light hole mass of 0.154 m_0 and high hole mobility of 5700 $cm^2/Vsec$ at 77°K. However, this device did not show impressive FET result because of the low sheet carrier concentration ($3.4x10^{11}/cm^2$). In the next section (5.3.2), a GaAs/(InGa)As/GaAs Strained Single Quantum Well p-MODFET structure with high carrier concentrations will be studied . In section 5.3.3, the GaAs barrier layer will be replaced with an AlGaAs layer with an increased valence band discontinuity in order to achieve higher carrier concentration and reduced impurity scattering from the impurities in the barriers.

5.3.2. GaAs/(InGa)As/GaAs Strained Single Quantum Well p-MODFETs

Vertical structure : Growth layers consist of a 2500Å GaAs buffer layer, 75Å Be-doped ($2x10^{18}/cm^3$) GaAs, 50Å GaAs spacer layer, 50Å (InGa)As strained channel layer with 20% indium, 50Å GaAs spacer layer, and 500Å Be-doped ($2x10^{18}/cm^3$) GaAs as shown in Figure 5.9. The Indium mole fraction of 20% has been chosen so that the maximum stain can be achieved with the reasonable critical thickness (≈200Å). A Hall data of the increased doping in the barriers will be an interesting comparison to the existing data in a similar structure by Fritz[FRITZ 86]. With this mole fraction, the biaxial compression becomes 1.4% using standard elasticity theory.

MBE growth conditions : For $(In_xGa_{1-x})As$ layer, relatively low growth temperatures (450°C-510°C) are preferred* compared to GaAs or (AlGa)As growth because the congruent sublimation temperature for InAs is much lower (about 370°C

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* Most III-V binary semiconductor layers grown at temperatures significantly lower than the congruent sublimation temperature are severely degraded [MUROTANI 78].

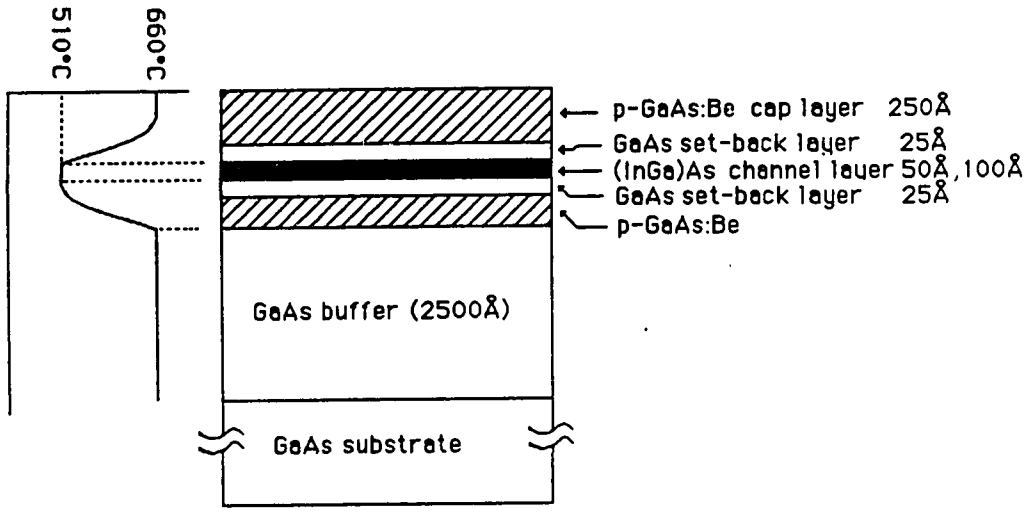


Figure 5.9 A cross section of GaAs/(InGa)As/GaAs SSQW p-MODFET structure.

[MILANO 78]) than that of GaAs (640°C [CHO 75]). The GaAs growth temperature was 660°C, and a lower growth temperature of 510°C was chosen for the $(In_{.2}Ga_{.8})As$ growth. We aimed at the higher side of the temperature range for the $(In_{.2}Ga_{.8})As$ growth in order to minimize the degradation of the adjacent GaAs film quality while the growth temperature is in transition from 660°C GaAs growth to that of the $(In_{.2}Ga_{.8})As$ growth, which is 510°C. The time constant of the Eurotherm substrate temperature by the controller is about 3 minutes. Growth rate of the epi-layer was 5000Å/hour and the flux ratio (J_V/J_{III}) was ≈20 measured by the beam flux gauge.

Hall-Effect Measurements : The Hall measurement results are shown in Table 5.3. Sample #400 has 50Å of strained $(In_{.2}Ga_{.8})As$ layer and sample #401 has 100Å of $(In_{.2}Ga_{.8})As$ layer. The mobility of sample #400, measured by the van der Pauw method, is 2,189 $cm^2/Vsec$ with a carrier concentration of $1.9x10^{12}/cm^2$ at 77°K. Because of the very thin (InGa)As channel layer of sample #400, the mobility may be degraded through surface roughness scattering. Sample #401 has sufficient thickness to avoid severe surface roughness scattering but it may be too thick to accommodate all of the lattice mismatch by the elastic strain, resulting in dislocations in the channel layer which causes mobility degradation even though the critical thickness for an $(In_{.2}Ga_{.8})As$ layer, calculated by the Matthews-Blakeslee expression is larger than 100Å (about 150Å). Since the Matthews-Blakeslee expression [MATTHEWS 76] of critical thickness was originally derived for strained superlattices, its application to a variety of other structures, including strained

single quantum well structures[Fritz 85] may not be valid. Our Hall-effect results are plotted in Figure 5.10, together with low carrier concentration data by Fritz*et al* [FRITZ 86]. It is empirically shown that the hole mobility is proportional to $p_s^{-0.59}$,where p_s denotes the hole concentration.

	#400		#401	
	300°K	77°K	300°K	77°K
Mobility (cm^2/V^*sec)	140	2189	128	606
p_s (cm^{-2})	$1.2x10^{13}$	$1.9x10^{12}$	$2.5x10^{13}$	$7.1x10^{12}$
$R_\square$ ($\Omega/\square$)	3.67 k	1.50 k	1.95 k	1.46 k
Strained Layer Thickness	50Å		100Å	

Table 5.3 Hall measurement results of single strained quantum well p-MODFET.

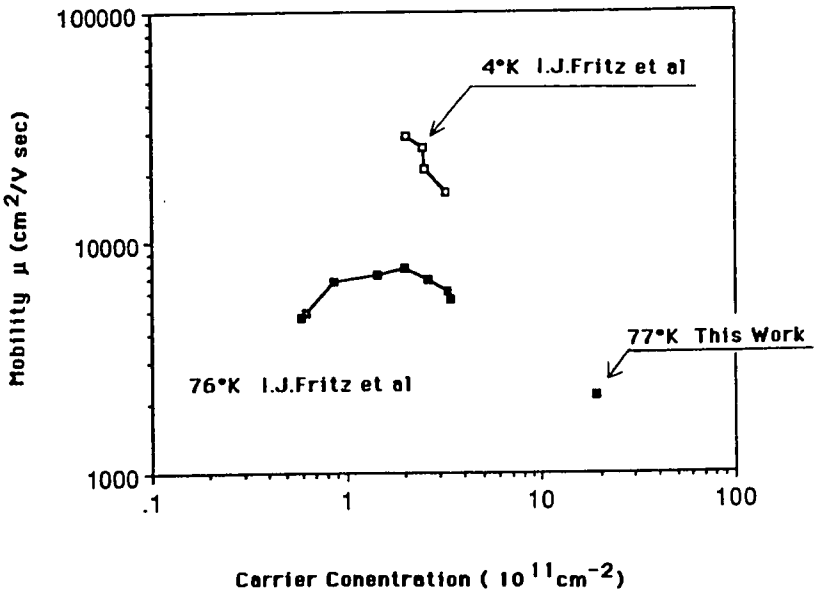


Figure 5.10 Hall mobility vs hole concentration for GaAs/$In_{.2}Ga_{.8}As$/GaAs strained single quantum wells.

FET performance : The processing details for these devices are the same as for the conventional p-MODFETs described earlier. The gate has been recessed to leave approximately 200Å of GaAs between the gate metal and the $(In_{.2}Ga_{.8})As$ channel layer. We have successfully made an enhancement mode strained single quantum well p-MODFET with a threshold voltage of -0.1volt. The structure is shown in Figure 5.11. The device showed excellent pinch-off characteristics and a reasonable transconductance of 5 mS/mm (Lg=2um,Wg=60um) at room temperature [YOH 87a] as shown in Figure 5.12. It is very encouraging that despite the low valence-band discontinuity (≈50meV), the devices showed reasonably high extrinsic transconductances which are comparable to p-MODFETs in the AlGaAs/GaAs system with the same device size.

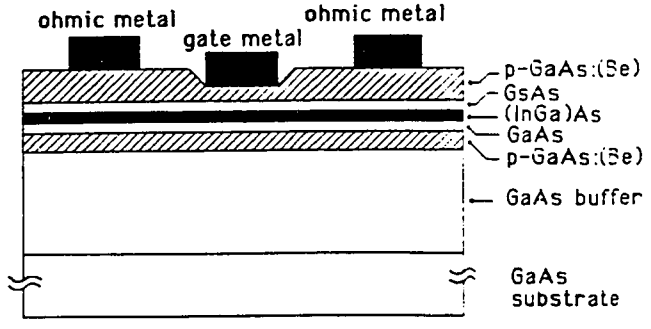


Figure 5.11 Cross sectional view of a GaAs/$In_{.2}Ga_{.8}As$/GaAs strained single quantum well p-MODFET

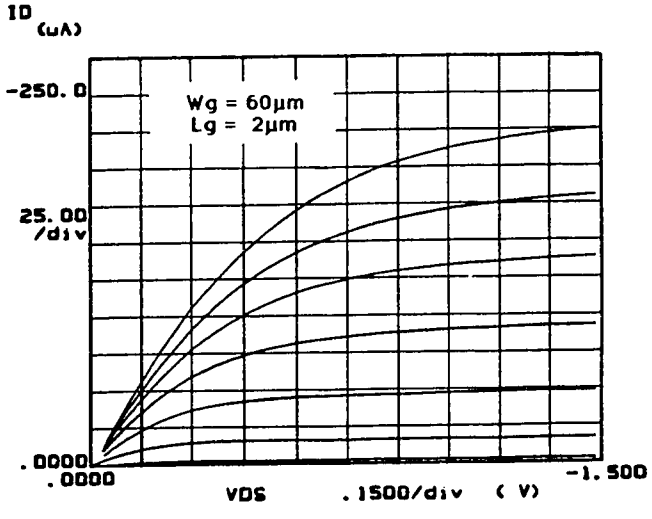


Figure 5.12 I_{ds}-V_{ds} characteristics of a GaAs/$In_{.2}Ga_{.8}As$/GaAs strained single quantum well p-MODFET. V_{gs} is varied from 0v to -1.2v in -0.2v steps.

5.3.3 (AlGa)As/(InGa)As/(AlGa)As Strained Single Quantum Well p-MODFETs

Optimization of the MBE growth conditions are required to minimize the surface roughness scattering and to maximize the (InGa)As thickness within the critical thickness calculated by Matthews and Blakeslee [MATTHEWS 76]. Superior results are expected using an (AlGa)As/(InGa)As/GaAs strained-layer single-quantum-well p-MODFET because it enables one to increase the valence band discontinuity by the amount of the (AlGa)As/GaAs valence band discontinuity. We have investigated several growth conditions to make Strained Single Quantum Well (SSQW) p-MODFETs with an enhanced valence band discontinuity. This approach has thus far not achieved a high enough 2DHG concentration to be used in a MODFET that would outperform the conventional structure [DRUMMOND 86]. Table 5.4 shows 77°K Hall measurement and photo-luminescence results of SSQW structures grown under various growth conditions, such as strained layer thickness and substrate temperature, in order to establish optimum conditions.

		#512	#525	#526
Mobility (cm^2/V^*sec)		2976	2287	6244
p_s (cm^{-2})		$1.56x10^{12}$	$1.52x10^{12}$	$7.1x10^{11}$
$R_\square$ ($k\Omega/\square$)		1.3	1.8	1.41
Strained Layer Thickness(Å)		100	75	75
Photo-Luminescence band width (at 77°K)		22meV Eg=1.328eV	53meV Eg=1.329eV	17.2meV Eg=1.34meV
Growth Temperature	InGaAs channel	520°C	520°C	570°C
	other layers	660°C	610°C	610°C

Table 5.4 Hall measurements and photo-luminescence results of AlGaAs/InGaAs/GaAs SSQW structures for p-MODFETs.

In Table 5.4, structures of #525 and #526 are identical except for the substrate temperature. Sample #526 gave the highest mobility and the narrowest photoluminescence line width at half maximum, however it had the lowest carrier concentration. The growth temperature transition during the epi-growth of #526 was the smallest, which may be contributing to a better interface, and hence a higher mobility. The low carrier concentration of #526, however, may be a result of the sublimation of indium atoms by the high substate temperature, 570°C, hence a lower In concentration and smaller valence band discontinuity. Samples #512 and #525 are different in both $(In_{.2}Ga_{.8})As$ layer thickness and substrate temperature. Let us assume that the thicker the film of $(Al_{.4}Ga_{.6})As$ grown with substrate temperature below 540°C, the rougher the interface between $(In_{.2}Ga_{.8})As$ and $(Al_{.4}Ga_{.6})As$. If this assumption is valid, then, the above result can be understood systematically. As shown in Figure 5.13, the order of the samples, according to the thickness of the poor quality $(Al_{.4}Ga_{.6})As$ layer, becomes #525,#512, and #526. The growth condition of #512 is perhaps the closest to the best growth conditions for the strained quantum well p-MODFET: (i) low substrate temperature (≈520°C or lower) for the InGaAs channel growth, and (ii) minimized low temperature growth of AlGaAs barrier layers.

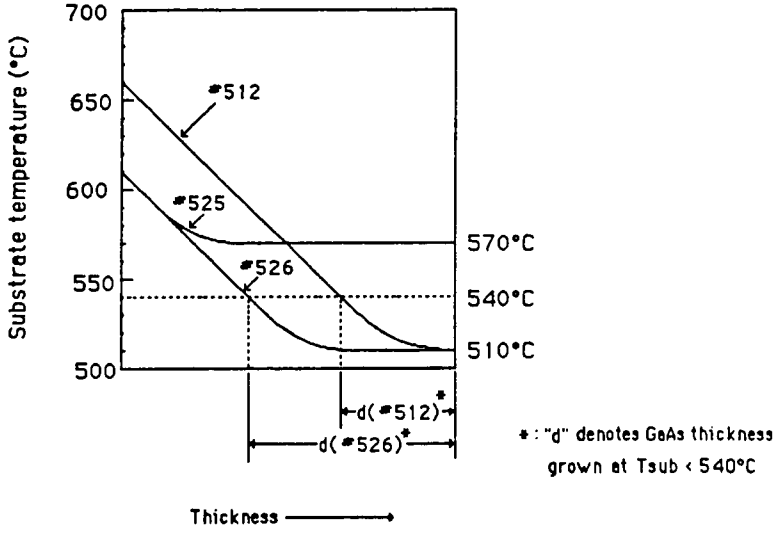


Figure 5.13 Schematic diagram of the substrate temperature transitions of AlGaAs barrier growth which is adjacent to the InGaAs channel layer. InGaAs channel layer starts at the right most edge of the figure.

FET performance : We have successfully made (AlGa)As/(InGa)As/GaAs SSQW p-MODFETs using the same growth conditions as #512 in Table 5.4 which produced the best sheet resistivity. The device structure is shown in Figure 5.14 and the measured I-V characteristics are shown in Figure 5.15. The MODFET performance was better than conventional p-MODFETs,but poorer than double heterojunction p-MODFETs at 80°K, however, it was the best device at room temperature. An extrinsic transconductance of 15 mS/mm was observed at room temperature. The threshold voltage shift with temperature is summarized in Figure 5.16. The threshold shift is as high as (0.35-0.38 volt) between 300°K and 80°K in both definitions of the threshold voltage (linear extrapolation or square

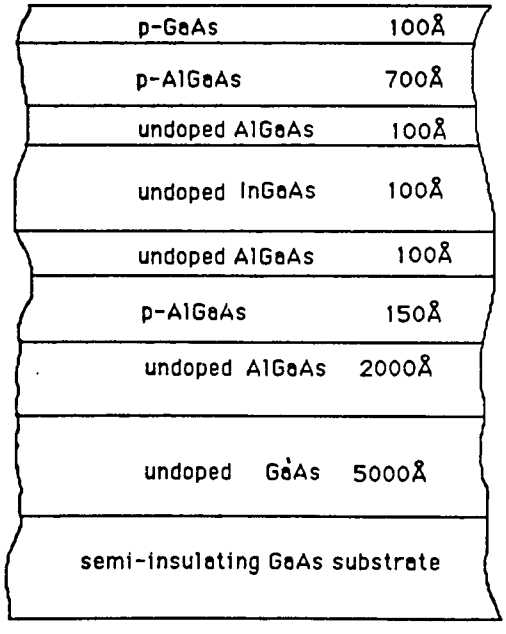
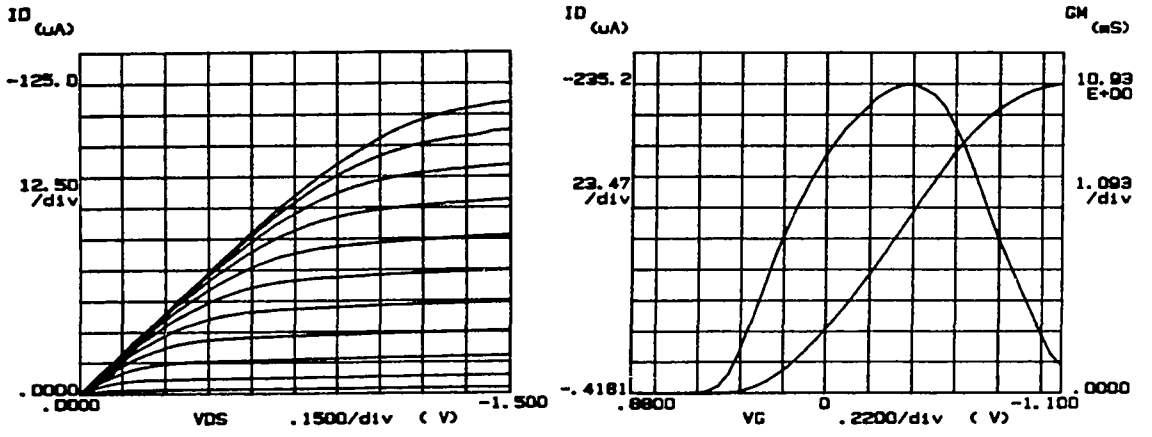


Figure 5.14 Cross sectional view of a strained single quantum well p-MODFET structure.



(a) (b)

Figure 5.15 (a) I_{ds}-V_{ds} characteristics ($V_{gs\ max}$ = -0.8v, -0.1v step), (b) I_{ds}-V_{gs} characteristics and extrinsic transconductance of a strained single quantum well p-MODFET. W/L=20μm/2μm.

	300°K	150°K	80°K	V_{th} (80°K)-V_{th} (300°K)
V_{th} (linear*)	0	-0.285	-0.352	-0.352
V_{th} (sqrt**)	0.337	0.104	-0.046	-0.383

* linear: Linear extrapolation

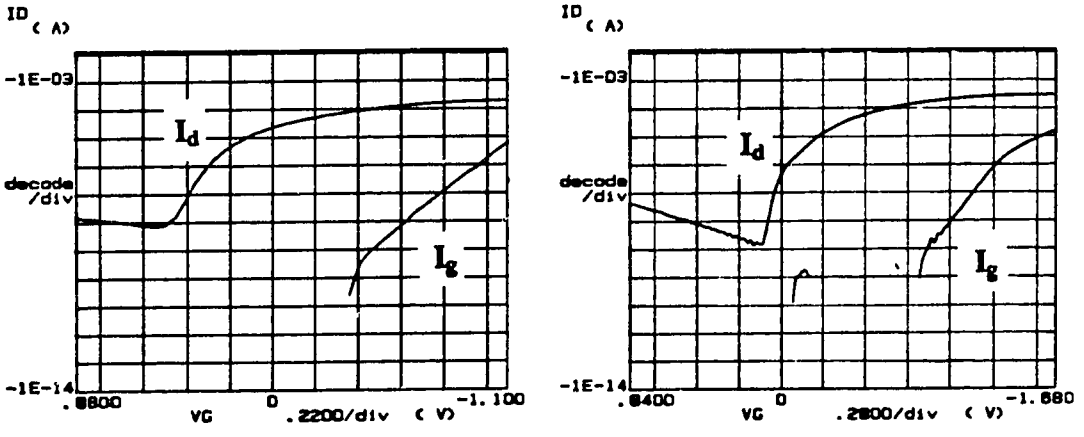
** sqrt: Square root extrapolation

Figure 5.16 Threshold voltage of strained single quantum well p-MODFETs at various temperatures.

root extrapolation). This result is smaller than the single heterojunction p-MODFET case (0.5volt shift) but larger than double heterojunction p-MODFET case (0.1-0.16 volt shift). There is no model to explain this result.

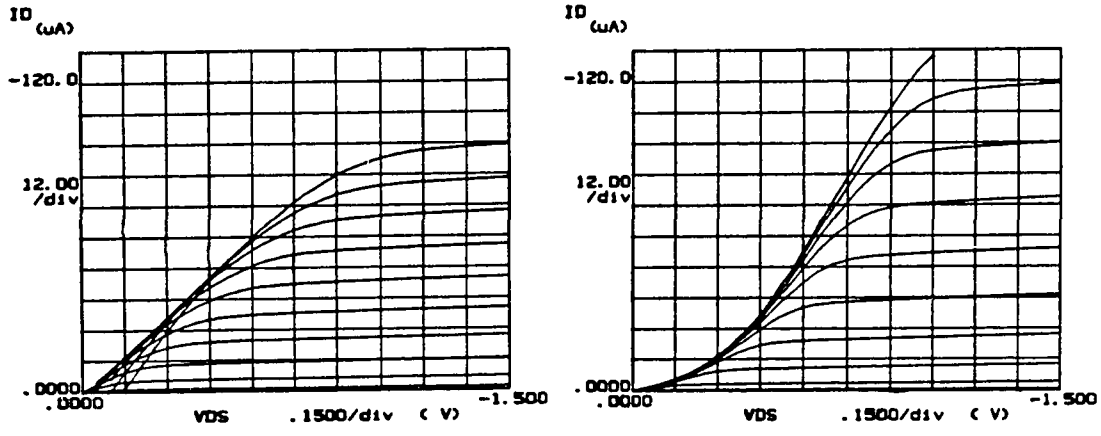
Subthreshold slope : The subthreshold slopes, S, were 85 mV/dec. and 35 mV/dec. for 300°K and 80°K, respectively, as shown in Figure 5.17. The slope at room temperature is, like the transconductances, better than either single heterojunction p-MODFET or double heterojunction p-MODFET. These result may indicate that the SSQW structure is promising at room temperature, but at cryogenic temperatures, the FET performance is limited by such mechanisms as alloy scattering, that become significant at low temperature.

Ohmic contact degradation : Ohmic contacts seem to degrade when the SSQW p-MODFET sample is cooled down to 80°K. Figure 5.18 illustrates this situation in its I_{ds}-V_{ds} characteristics. The reason is unknown yet, but the only structural difference between the SSQW and double heterojunction p-MODFET is the use of an InGaAs layer and the associated growth conditions, such as low substrate temperature growth.



(a) (b)

Figure 5.17 Subthreshold characteristics of a SSQW p-MODFET (a) at 300°K and (b) at 77°K.



(a) (b)

Figure 5.18 Ohmic contact degradation of a SSQW p-MODFET. (a) I_{ds}-V_{ds} characteristics at room temperature , (b) I_{ds}-V_{ds} characteristics at 77°K showing ohmic contact degradation compared to the room temperature curves.

5.3.4 Subsection Summary of Strained Quantum Well p-MODFETs

It is clear that the hole mobility decreases with increasing carrier concentration by the $p_s^{0.59}$ law. This creates a difficult compromise in achieving both reasonably high mobility and carrier concentration. Strained single quantum well p-MODFETs have been fabricated and show good FET performance, especially at room temperature. Various growth conditions suggest that the growth temperature of the barrier (AlGaAs) layers is the key point to get high FET performance. There is a trade-off between (InGa)As growth temperature and (AlGa)As growth temperature. The not-as-good FET results at cryogenic temperatures may come from such mechanisms as alloy scattering or scattering from defects in the strained layer (not a 100% accommodation of lattice mismatch by strain) or

some unknown deterioration mechanism of the ohmic contacts when the metal is alloyed on the (AlGa)As/(InGa)As system.

5.4 Channel-doped p-MODFET

5.4.1 Introduction

An alternative way to increase the carrier concentration in the channel of MODFETs is the δ-doped channel. By δ-doping at the center of the channel, the carrier concentration can be increased, while reducing impurity scattering by the screening effect. The δ-doping is an interesting technology of doping mono-layers of donor or accepter impurities in the host semiconductor which was developed in n-channel GaAs FET[SCHUBERT 86] and very high electron concentrations of $10^{13}\,cm^{-2}$ have been obtained [SCHUBERT 87]. The δ-doped GaAs FET is not a MODFET, but there is another study on doped-channel MODFET [INOMATA 86], in which higher performances (K-value and transconductance) are reported by reducing the AlGaAs thickness and compensating the carriers from the channel doping. We have combined this idea of a doped-channel MODFET and δ-doping in the MBE growth and applied them to a p-channel MODFET.

5.4.2 Device Structure and MBE Growth

The device structure is shown in Figure 5.19. It is basically a double heterostructure MODFET, but the $(Al_{.4}Ga_{.6})As$ layer under the channel is undoped. Instead, the structure utilizes pulse doping (or δ-doping) in the channel to compensate the lack of carriers from the backside $(Al_{.4}Ga_{.6})As$ layer. Thus, from the bottom to the top, the epi-layers of the device consist of a GaAs buffer layer, an undoped $(Al_{.4}Ga_{.6})As$ buffer layer, a δ-doped GaAs channel layer with Be, an undoped $(Al_{.4}Ga_{.6})As$ set-back layer, a Be-doped $(Al_{.4}Ga_{.6})As$ layer, and a Be-doped GaAs cap-layer. There has been no report on δ-doping with Be so far. However, reports of ultra-high doping (of the order of $10^{20}\,cm^{-3}$) with Be by conventional MBE growth technique suggest problems, including: interstitial Be incorporation [DUHAMEL 81], concentration dependent Be diffusion [Miller 85], and loss of crystal integrity [LIEVIN 85]. All of these suggest that low growth temperature (450°C-500°C) is required for high doping levels. Taking account of these results, we chose the following δ-doping procedure. Start ramping down the substrate temperature

(from 660°C to 470°C) during the growth approximately 5 minutes before the δ-doping starts. The growth is then stopped at the points where δ-doping is desired(two times) and the Be shutter is opened to create a partial mono-layer of Be. The shutter is then closed, the substrate temperature is returned to 660°C and growth of the remaining layers of the top $(Al_{.4}Ga_{.6})As$ and GaAs channel layer interface are resumed. The temperature profile is schematically shown in the Figure 5.19. The reason we ramp the substrate temperature down and up continuously during the growth as opposed to stopping the growth completely (for five minutes!) during the temperature transition period is to avoid the undesirable accumulation of impurities in the epi-layers. On the other hand, by this method, the quality of the epi-layers grown at low temperatures may become so poor as to seriously affect the transport. There is an alternative δ-doping procedure to avoid this risk. That is to grow all layers with normal substrate temperature except the mono-layer growth of δ-doping and use the growth interruption to change the substrate temperature. However, this method has a potential risk of introducing impurities and defects at the δ-doping plane.

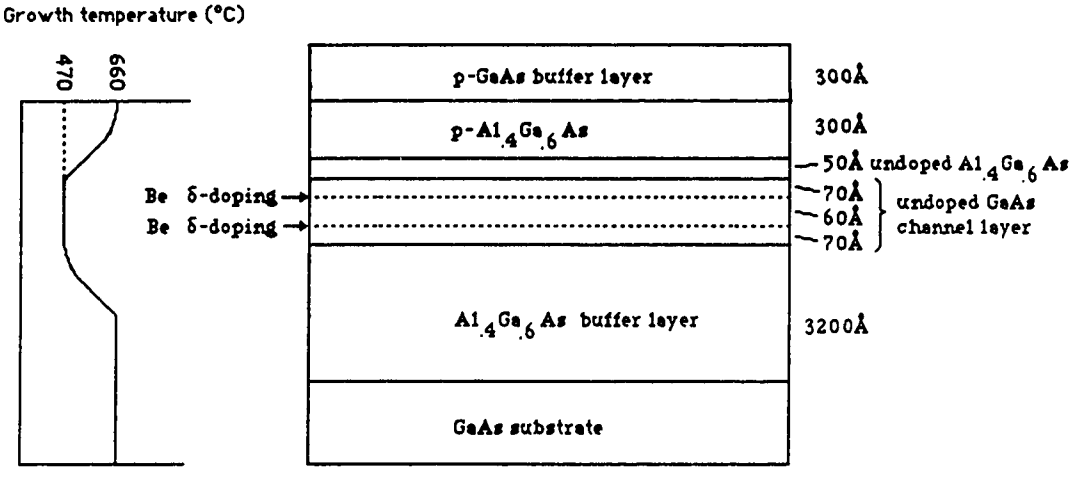
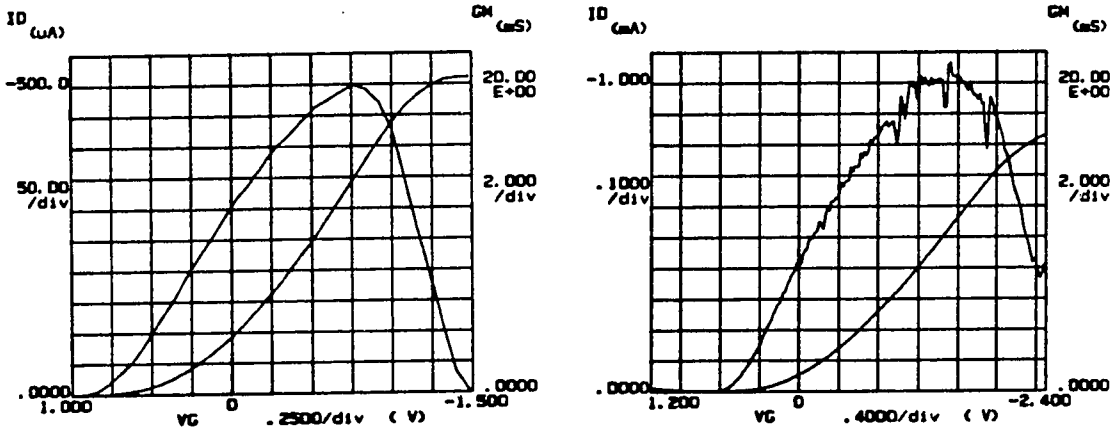


Figure 5.19 Cross sectional view of a δ-doped channel p-MODFET and the substrate temperature profile during the MBE growth.

5.4.3 Electrical measurements of δ-doped structures

The Hall-effect measurements showed very high carrier concentrations ; 9.4 x 10^{12} cm^{-2} and 1.04 x 10^{13} cm^{-2} at 300°K and 77°K respectively. However, these measurements showed low hole mobilities ; 98 cm^2/Vs and 132 cm^2/Vs at 300°K and 77°K respectively. The low hole mobility, especially at 77°K, may be caused by (i) the possibly degraded crystal quality resulting from the low temperature growth or (ii) impurity scattering by δ-doped ions which may have spread by diffusion. The high carrier concentration may play a more important role than low-field mobility in the short channel FET devices.

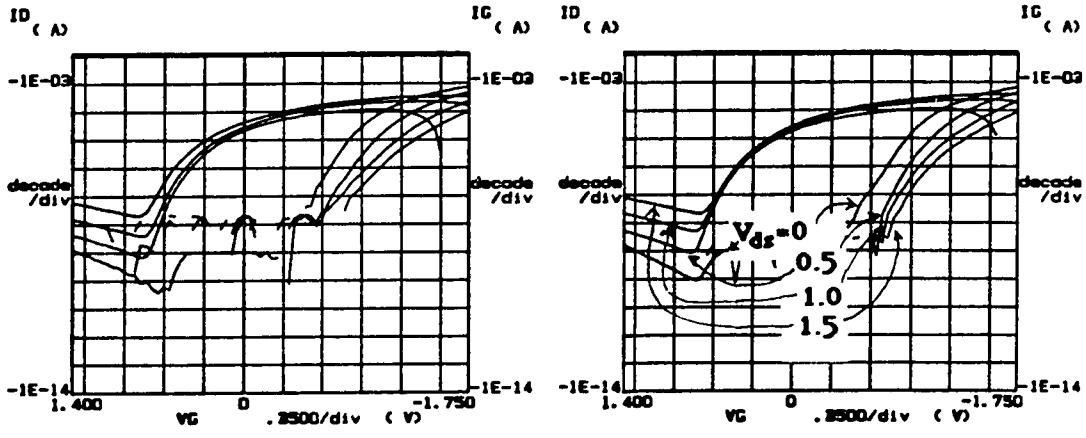
Transistor characteristics : The I_{ds}-V_{gs} characteristics at room temperature are shown in Figure 5.20. As expected from the Hall-effect measurement , the δ-doped channel p-MODFET shows high extrinsic transconductance (g_m=20mS/mm) and high maximum drain current (I_d=25.8mA/mm) at room temperature. However, at cryogenic temperatures, the maximum transconductance remained the same (20mS/mm) as at room temperature and the threshold voltage increased (in the negative direction) by 0.34 volt. This may be indicative of the possible freeze-out of the δ-doped impurities in the channel. The δ-doped channel p-MODFET seems to be attractive as far as room temperature operation is concerned.



(a) (b)

Figure 5.20 (a)I_{ds}-V_{gs}characteristics and g_m at room temperature, (b) I_{ds}-V_{gs} characteristics and g_m at 77°K.

Subthreshold current : The subthreshold current of a δ-doped channel p-MODFET also showed an asymptotic exponential dependence on gate voltage shown in Figure 5.21. The transition to the exponential dependent region seems to take place gradually, so that the slope does not seem to become constant. This is in contrast to the other p-MODFET structures, such as single and double heterojunction p-MODFETs and single strained quantum well p-MODFETs, which exhibited a much sharper transition, so that the slope of the asymptote could be found more easily. The temperature dependence of the short channel effect is also different from that of the other p-MODFET structures. In single and double heterojunction p-MODFETs, the short channel effect was more pronounced at 77°K and it was very small at room temperature. In the δ-doped channel p-MODFET



(a) (b)

Figure 5.21 Subthreshold characteristics (a) at room temperature, and (b) at 77°K. Drain voltage is varied from 0v to -1.5v by -0.5v step.

case, the situation is reversed; the short channel effect is much less obvious at 77°K. The physics behind this is not clear, but whatever the reason, it is unfortunate for the δ-doped channel p-MODFET that the short channel effect is more pronounced at room temperature where its performance is superior to other p-MODFET structures in both transconductance and maximum drain current.

Light sensitivity : Light exposure commonly induces photo-excited current so that the drain current of a MODFET tends to increase slightly upon exposure to light. However, the δ-doped channel p-MODFET showed the opposite reaction : reduction of the drain current upon exposure to a light. One can interpret this as an increase of the threshold voltage (by 0.2 volt in the negative direction) as is shown in Figure 5.22. This phenomenon is reproducible. The tendency seems to be inconsistent with the freeze-out assumption which was made to explain the threshold voltage dependence on temperature.

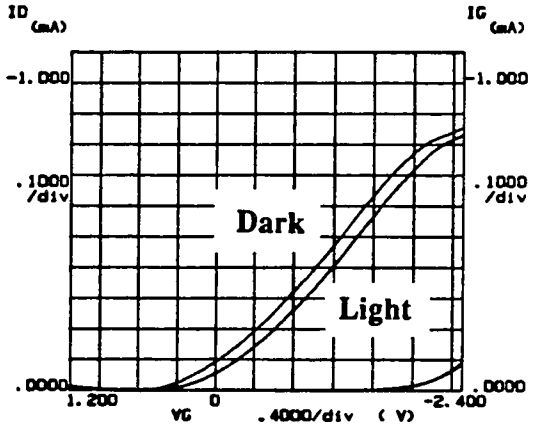


Figure 5.22 Light response of I_{ds}-V_{gs} characteristics of the δ-doped channel p-MODFET

5.4.4 Subsection summary

The δ-doped channel p-MODFET has been investigated as an alternative structure for the improved p-MODFET. This device demonstrates superior performance compared to other p-MODFET structures at room temperature, however, it showed no improvements at cryogenic temperatures. The background device physics for the unusual temperature dependences of the current-voltage characteristics is unknown yet. The freeze-out of the δ-doped impurities in the channel may well be one of the factors that make the device behavior unusual, but there must be some unknown factors yet to be discovered to solve the mystery.

5.5 COMPARISON OF VARIOUS P-MODFET APPROACHES

Three approaches have been investigated in order to improve p-channel MODFET performance. In this section, results of these approaches are compared and summarized in (i) low electric field characteristics (Hall-effect measurements) and (ii) high electric field characteristics (field-effect transistor measurements).

5.5.1 Low-Field Mobilities and Sheet carrier Concentrations of Two-Dimensional Hole Gases

Hall mobilities of the various modulation-doped structures measured at 77°K are plotted as a function of two-dimensional hole gas concentration in Figure 5.23. The diagonal lines indicate regions of constant sheet resistivity. Ordering the various p-MODFET structures by their sheet resistivity from the largest to the smallest are as follows : δ-doped channel p-MODFET, single heterojunction p-MODFET, strained single quantum well p-MODFET, and double heterojunction p-MODFET. The double heterojunction p-MODFET gives the smallest sheet resistivity and the δ-doped channel p-MODFET gives the largest sheet resistivity.

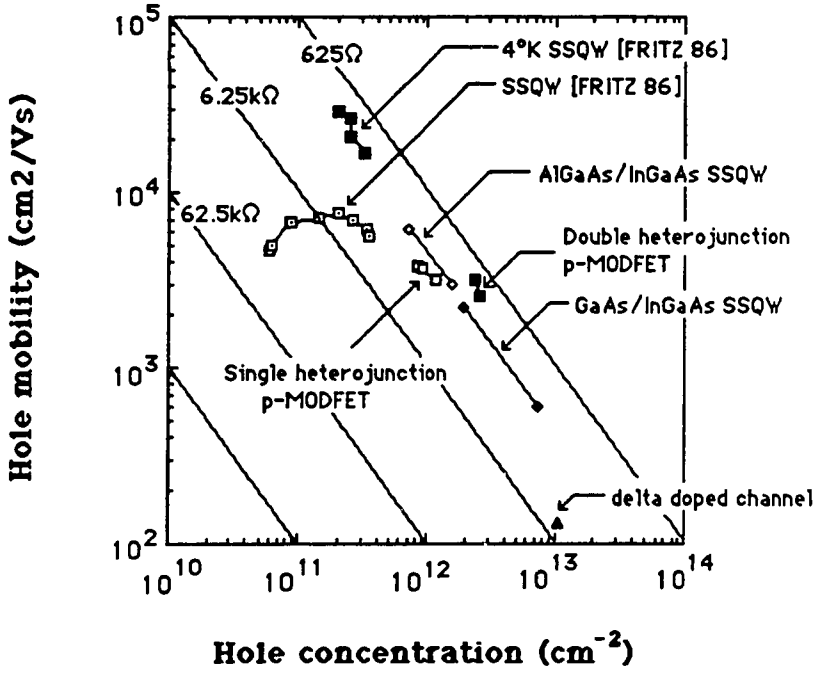


Figure 5.23 Hall mobilities of various modulation-doped structures measured at 77°K (unless explicitly stated) as a function of two-dimensional hole gas concentration.

5.5.2 High Electric Field Characteristics (FET transconductance)

The values of low-field mobility do not necessarily translate directly to improved FET performance because the electric-field in a short channel FET is of the order of 10^3 to 10^4 V/cm along the channel and velocity saturation effects may dominate FET performance. Transconductances (normalized to 1 μm gate length devices) of the various p-MODFETs are shown in Table 5.5. It shows that (i) double heterojunction p-MODFET is the best at 77°K, (ii) the δ-doped channel p-MODFET is the best at room temperature, (iii) strained quantum well p-MODFET is useful when high hole mobility is needed and high carrier concentration is unnecessary, such as an experiment of quantum Hall effect of holes.

	Transconductance (mS/mm)		
	300°K	150°K	77°K
DHP	13	21	36
SSQW	16.6	28	30
δ-doped	20	-	20

DHP : Double Heterojunction P-MODFET
SSQW : Strained Single Quantum Well p-MODFET
δ-doped : δ -doped channel DHP

Table 5.5 Summary of various p-MODFET structures.

5.6 PSEUDOMORPHIC N-MODFETS

5.6.1 Introduction

In order to eliminate the "DX center" related problems of conventional AlGaAs/GaAs MODFETs, pseudomorphic AlGaAs/ InGaAs single-quantum-well N-MODFETs have been proposed[MASSELINK 85]. This method is also suited for complementary MODFET circuit application because of its improved performance at cryogenic temperatures, including, elimination of current collapse and a small threshold voltage shift with temperature. This structure is superior to alternative methods of reducing the Aluminium mole fraction in the $(Al_xGa_{1-x})As$ layer because one does not have to reduce the conduction-band discontinuity so that high carrier concentration and good carrier confinement are still retained. For complementary circuit application, the device operations should be checked with high enough threshold voltages to confirm low power dissipation and full voltage swing.

5.6.2 Structure and Fabrication

The pseudomorphic device structure is shown in Figure 5.24. The idea is to lower the Aluminium compound ratio in the $(Al_xGa_{1-x})As$ layer to eliminate deep levels, while still maintaining the conduction-band discontinuity by introducing narrow-gap InGaAs for the channel layer. By correctly choosing the Indium mole fraction and the InGaAs layer thickness, the $(In_yGa_{1-y}As)$ layer can accommodate the lattice mismatch by the strain rather than misfit dislocations. The substrate temperature (T_{sub}) dependence on electron mobility and sheet carrier density have been investigated by changing the combination of low T_{sub} for the $(In_yGa_{1-y}As)$ layer and high T_{sub} for the other layers. The best Hall-effect measurement results have been obtained with the T_{sub} condition illustrated in Figure 5.24. The electron mobilities of 3010 cm^2/Vs and 18700 cm^2/Vs with an electron sheet carrier concentrations of $5.1x10^{12}$ $/cm^2$ and $2.2x10^{12}$ $/cm^2$ have been obtained at 300°K and 77°K, respectively.

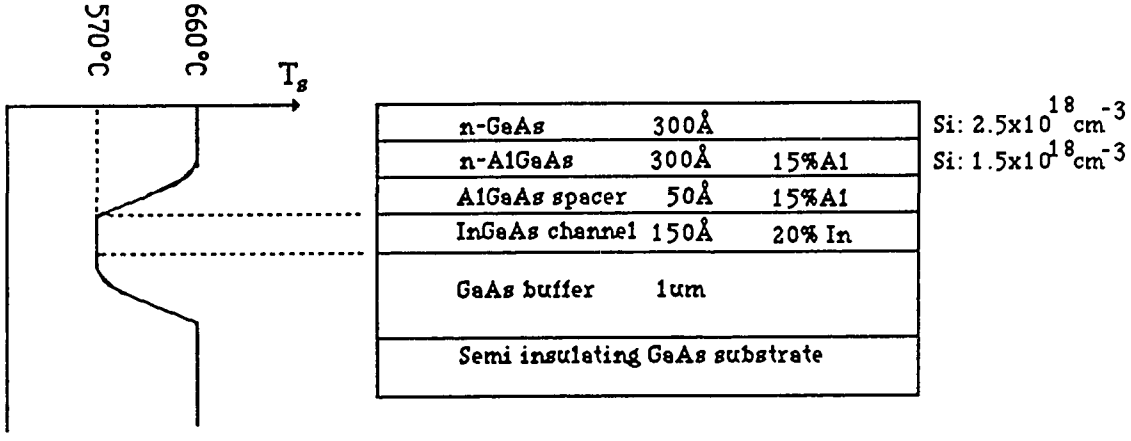


Figure 5.24 A cross section of a pseudomorphic n-MODFET structure. The substrate temperature profile is also shown on the left hand side of the cross section.

5.6.3 Pseudomorphic N-MODFET performance

Typical I_{ds}-V_{ds} characteristics of an enhancement pseudomorphic n-MODFET are shown in Figure 5.25. The transconductance and maximum drain current have been increased by 1.72x and 2.28x, respectively, upon cooling to cryogenic temperatures as shown in Table 5.6. These devices showed virtually no deep level effect at cryogenic temperatures in the dark, as expected. The gate length of the device is 1.5 μm. The threshold voltage shift (increase) from 290°C to 77°C was 0.156 volt which is small compared with that of the conventional structure (0.25-0.3 volt). The dramatic increase of both transconductance and maximum drain current make a clear contrast with conventional n-MODFET performance, which showed virtually no improvement in transconductance and maximum drain current when the device was cooled down to 77°K, even under illumination. This has been discussed in chapter 4. The best results of our

pseudomorphic n-MODFET device with lower threshold voltage showed transconductances of 220 mS/mm and 350 mS/mm, and maximum drain currents of 170 mA/mm and 380 mA/mm at 300°K and 77°K, respectively. These results compare favorably with the best results reported [MASSELINK 85] for similar structures. The quality of our material and devices has been confirmed with this comparison, however, because of the higher threshold voltages desired for complementary circuits, they do not yield the best results reported.

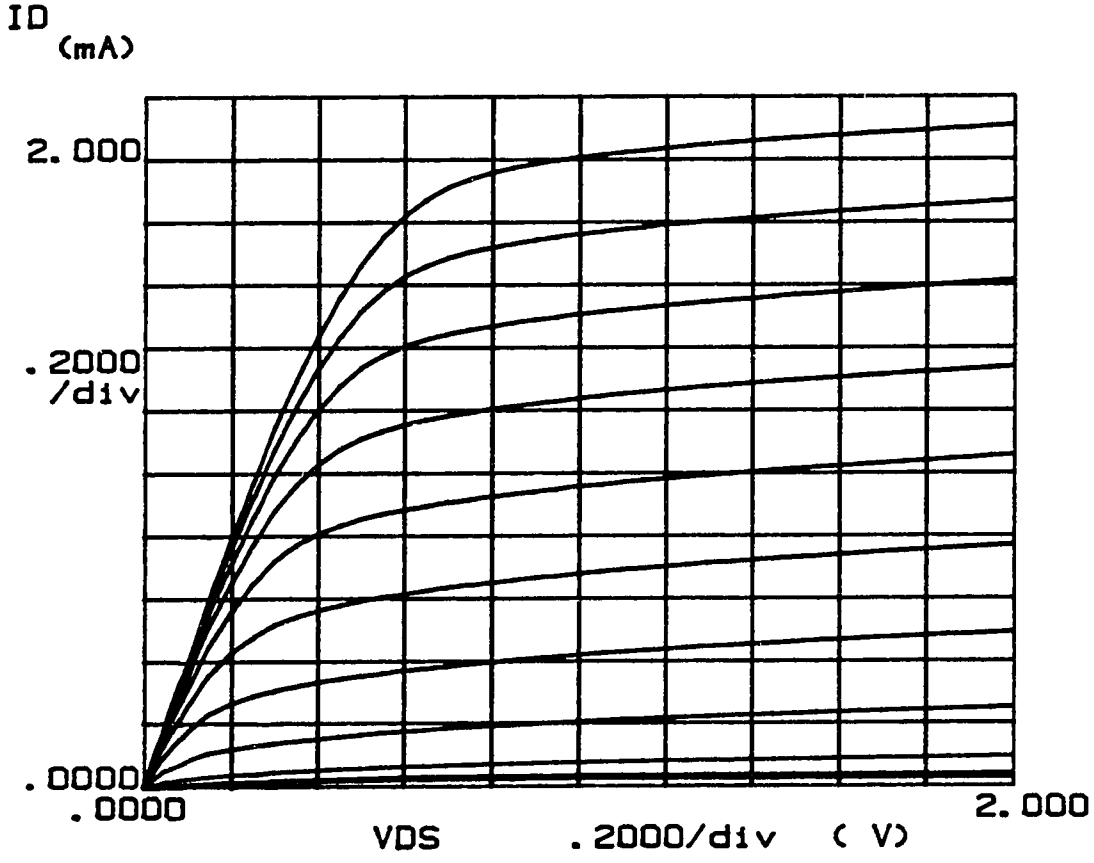


Figure 5.25 Typical I_{ds}-V_{ds} characteristics of an enhancement pseudomorphic n-MODFETs. V_{gs} is varied from 0v to 1.0v (0.1v step).

	300°K	77°K
Hall mobility (cm^2 /vsec)	3010	18700
Sheet Carrier Concentration (/cm^2)	$5.1x10^{12}$	$2.2x10^{12}$
Transconductance (mS/mm)	220	350
$I_{ds\ max}$ (mA/mm)	170	380

Table 5.6 Pseudomorphic n-MODFET performance.

5.6.4 Subsection summary

Enhancement pseudomorphic n-MODFETs with sufficiently high threshold voltage for complementary circuit use, have been successfully fabricated. Excellent I-V characteristics with no DX center related problems, such as drain current collapse or serious threshold voltage shift, have been confirmed.

5.7 SUMMARY

In this chapter, improvements of both p-MODFET and n-MODFET have been investigated. Various approaches have been investigated to find the best method to improve the p-MODFET, which is the key to significantly improve complementary MODFET circuit performance. A straight double heterojunction p-MODFET shows the best electrical performance among the four different approaches (including conventional p-MODFET and three new approaches described in this chapter). The double heterojunction p-MODFET structure needs to be refined for integrated circuit application because the fabrication of enhancement type double heterojunction MODFETs (n-MODFET as well [INOUE 87]) produce large threshold voltage variations unless structural optimization is done very thoroughly. From these investigations, I have selected the double heterojunction p-MODFET and pseudomorphic n-MODFET as the best candidates for investigation in a complementary circuit architecture to further test its potential performance for high speed digital logic applications.

Chapter 6

IMPROVED COMPLEMENTARY MODFETS

6.1 INTRODUCTION

Improved structures for both p-channel MODFET and n-channel MODFET have been investigated in the previous chapter. For improved complementary MODFET circuits, the double heterojunction p-MODFET and pseudomorphic n-MODFET were chosen to evaluate the performance of C-MODFET circuits based upon the optimum devices currently available. Because gate length plays such a crucial role in high speed FET performance, particularly where velocity saturation is not achieved, the gate length of both types of MODFETs were laterally shrunk to 1μm, and the drain to source distance is decreased to 3 μm for these second generation circuits. Other details of the structures are described in section 6.2. Circuit performance, including inverter transfer characteristics and ring oscillator results are discussed in section 6.3. Data from another complementary circuit structure, using a δ-doped channel p-MODFET is also compared. These new structures showed the smallest propagation delay among all complementary heterojunction semiconductor circuits[YOH 87b] at 77°K. The power delay product of the circuit achieved an order of magnitude improvement compared to the previous record because of our choice of device structures, which allowed optimization of the threshold voltages. Finally, these results are compared with Low Temperature CMOS, which would be a competing technological approach for many applications.

6.2 A NEW COMPLEMENTARY MODFET STRUCTURE

A new target structure for improved complementary MODFET circuits is shown in Figure 6.1. It consists of a double heterojunction p-MODFET and a pseudomorphic n-MODFET. The double heterojunction p-MODFET shown in this figure has a slightly different structure from the one described in chapter 5. This structure does not have Be doping in the $(Al_{.4}Ga_{.6})As$ layer under the channel. This is because an "enhancement type" double heterojunction p-MODFET with p-type doping on both sides of the channel

requires such precise control of doping and thickness to control the threshold voltage, that it was judged too risky to be applied to integrated circuits of even ring oscillator level integration*. A mere 17 stage ring oscillator, for example, is composed of 28 transistors, including output buffers. All transistors must have well controled threshold voltages and I-V characteristics in a complementary configuration. The enhancement type double heterojunction p-MODFET, at least in our laboratory, is not sufficiently refined to be applied to an integrated circuit. Thus, the ultimate target structure, using a complete double heterojunction p-MODFET, must be postponed for future work. A "modified" double heterojunction structure is shown in Figure 6.1 and it is used for our present experiments. The gate length of both types of MODFET is 1μm and the drain to source distance is 3μm. The Be-doped cap layer thickness is increased to 300Å and the Be-doped $(Al_{.4}Ga_{.6})As$ layer is decreased to 300Å for the purpose of obtaining better ohmic contacts. The undoped $(Al_{.4}Ga_{.6})As$ spacer layer is designed to be 50Å in thickness so that higher carrier concentration is achieved. The fabrication process is identical to the one described in chapter 3, except the MBE growth procedures which was explained in chapter 5.

6.3 CIRCUIT PERFORMANCE

6.3.1 MODFET Performance

Based on the fabrication technologies described in the previous chapters, double heterojunction p-MODFETs and pseudomorphic n-MODFETs have been integrated to form a complementary circuit using selective MBE. The current-voltage characteristics of both types of MODFETs from the C-MODFET wafer are shown in Figure 6.2. The threshold voltages at 77°K are 0.46 volt and -0.5 volt for the n-MODFET and the p-MODFET respectively. These values are slightly higher than optimum for highest speed, but suitable to investigate complementary circuit operation and they are not a serious problem for lower drain currents due to high threshold voltages. The maximum drain currents are 1.5 mA and 400 μA for n-MODFET and p-MODFET, respectively. The ratio of the drain currents is approximately four, which would have been reduced to two if an optimum double heterojunction p-MODFET, with precisely controlled threshold voltages

* Similar difficulty is found in double doped n-channel MODFETs [INOUE 87].

could be reliably fabricated with the channel width ratio of three (60μm/20μm) between p- and n-MODFET.

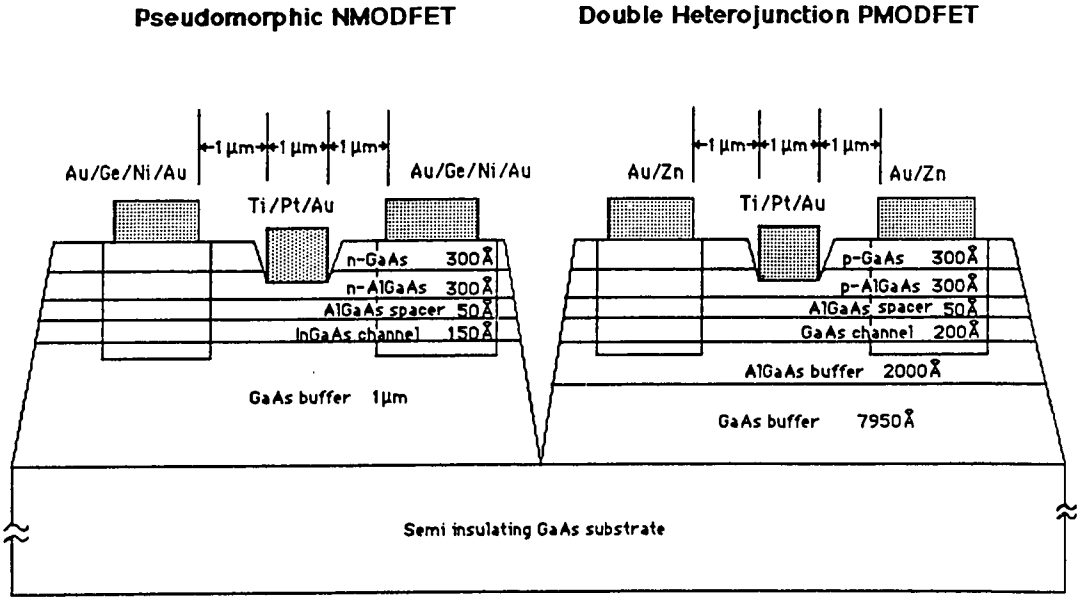
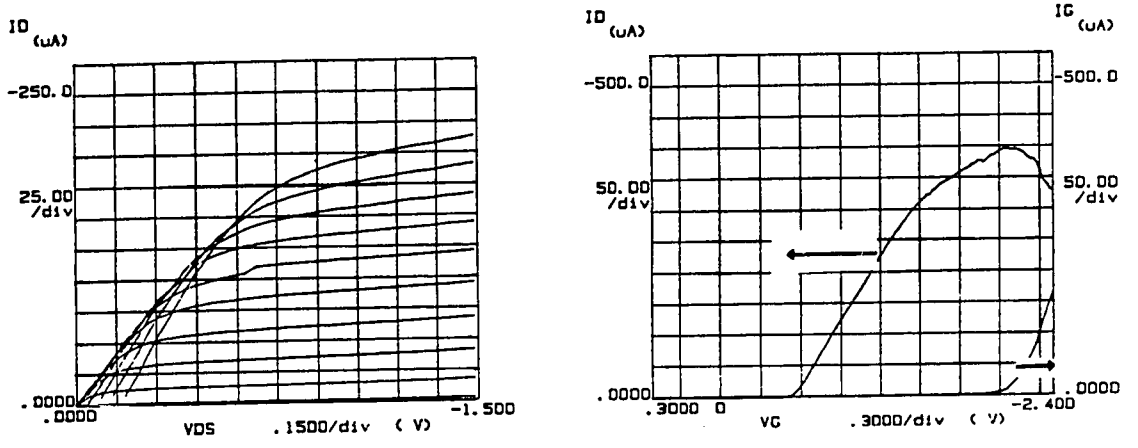
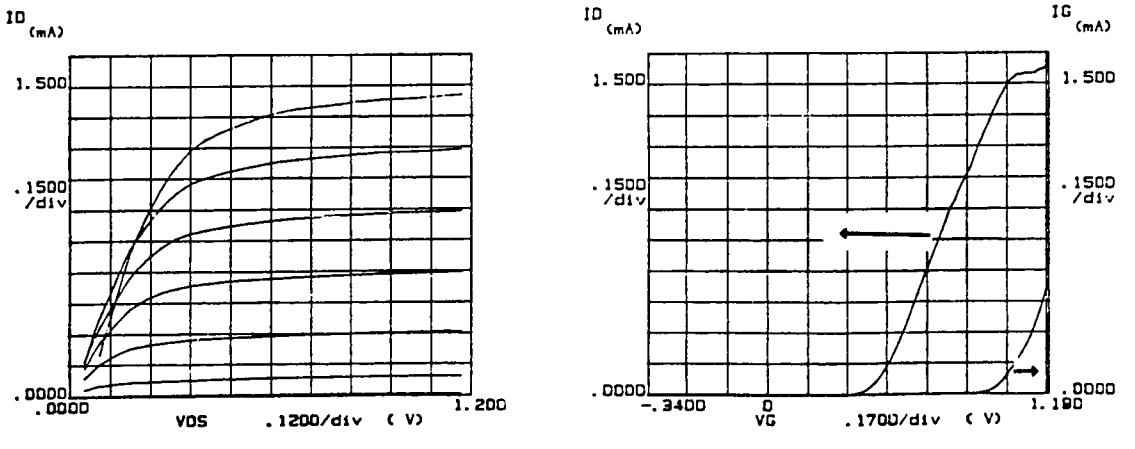


Figure 6.1 Cross section of an improved complementary MODFET structure



(a)



(b)

Figure 6.2. Current-voltage characteristics of (a) a double heterojunction p-MODFET and (b) a pseudomorphic n-MODFET. $(W/L)_p$ = 60μm/1μm, $(W/L)_n$ = 20μm/1μm. Maximum forward gate voltages are 1.0 v and -1.3 v for n- and p-MODFET respectively. Voltage steps are 0.1v for both n- and p-MODFETs.

6.3.2 Inverter Characteristics

The inverter transfer characteristics of the improved complementary MODFETs measured at 77°K are shown in Figure 6.3. The (W/L)'s of the MODFETs used in the inverter are 100μm/1μm and 20μm/1μm for the p-MODFET and the n-MODFET, respectively. The transfer curve shows ideal complementary inverter circuit characteristics because of the sufficiently high threshold voltages which are matched between p- and n-MODFETs. Noise immunity of 94 % has been achieved. When the supply voltage exceeds one volt, one can notice that the stand-by gate current starts to pull the output voltages. If we closely examine the transfer curve, one notices that the amount of voltage pulled up from output low level is larger than the amount of voltage pulled down from output high level. This indicates that the on-set voltage for gate leakage current through the n-MODFET gate is smaller than that through p-MODFET gate. This is consistent with the I_{gs}-V_{gs} characteristics shown in Figure 6.2.

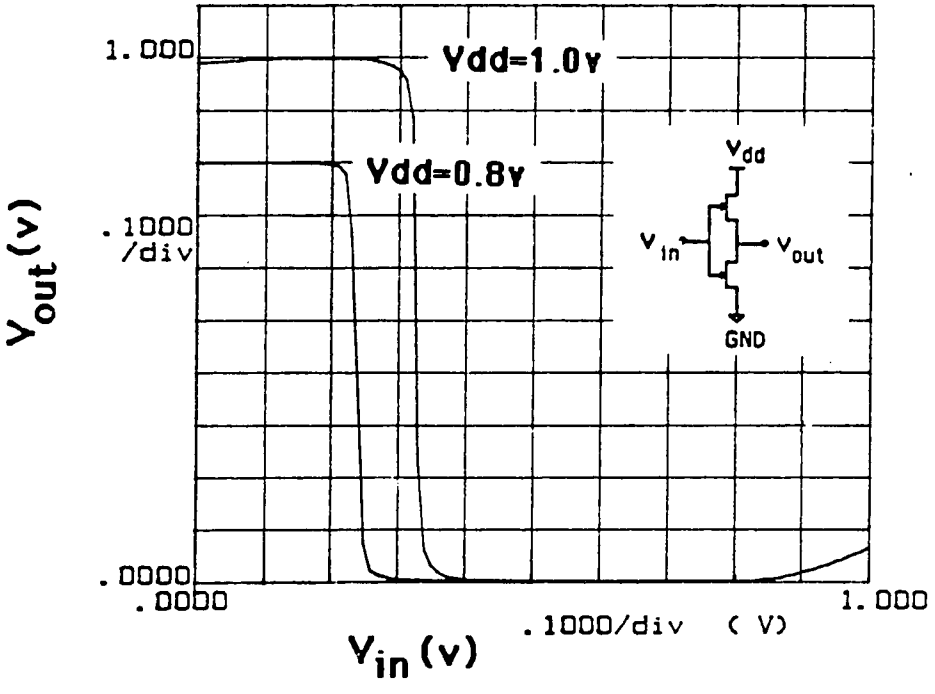


Figure 6.3 Inverter transfer curves of a complementary MODFETs measured at 77°K. W(p)/W(n) = 100μm/20μm.

6.3.3 Ring Oscillator Results

Seventeen stage ring oscillators have been fabricated and the propagation delay time and power dissipation have been investigated. Figure 6.4 shows a SEM microphotograph of a ring oscillator. The room temperature results in Figure 6.5 show the values of propagation delay and average current consumption per stage as a function of supply voltage.

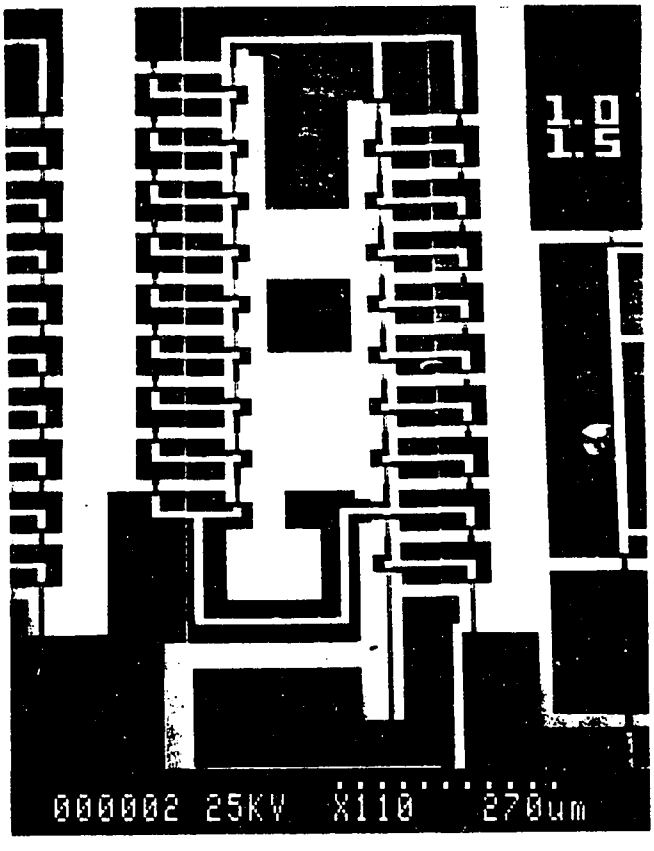
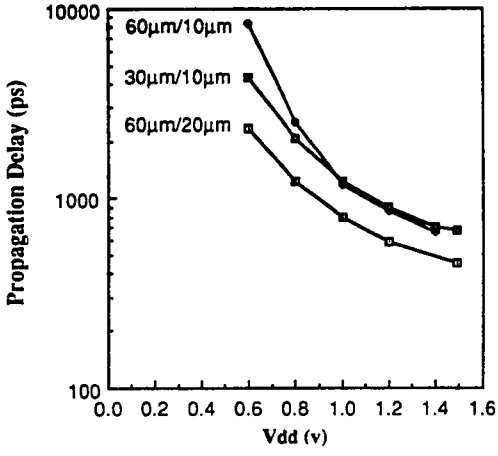


Figure 6.4 SEM microphotograph of a 17 stage ring oscillator.

Ring oscillator performance at room temperature : The room temperature delay [Figure 6.5(a)] time has been improved by a factor of two compared with that of the 2μm gate length devices discussed in chapter 4. This result compares favorably with the low temperature(77°K) results of the 2μm devices. It should also be noted that the operational voltage margin has become narrower, compared with 2μm devices. This reduction is caused by the increased logic threshold voltage slope [Cf.Figure 4.12, p43] due to the improved 1μm gate length p-MODFET. This indicates that the p-MODFET improvement has been more pronounced than the n-MODFET improvement. Another notable point in Figure 6.5(a) regards the propagation delay dependence on the W/L inverter ratio. When we compare the two ring oscillators [W_p/W_n=60μm/10μm and W_p/W_n=60μm/20μm] which have nearly equal input capacitance, the smaller W/L ratio between p- and n-MODFET[W_p/W_n=60μm/20μm=3] gives a smaller gate delay as can be seen in Figure 6.5(a). When two ring oscillators with the same W/L inverter ratio [W_p/W_n=30μm/10μm and W_p/W_n=60μm/20μm], but different sizes, the ring oscillator with larger gate width [W_p/W_n= 60μm/20μm] gives the smaller gate delay. This suggests the existence of appreciable parasitic capacitance of the interconnects. The current dissipation dependence on power supply voltage [Figure 6.5(b) and (c)] has an overall linear relationship, except for an exponential dependence in the small V_{dd} region. This indicates that the total power dissipation is limited by the on-resistance of the MODFETs in the circuit. The gate leakage current path at high supply voltages, beyond the Schottky diode forward voltage, flows either through the p-MODFET of the previous stage inverter and the Schottky gate of the present stage n-MODFET or vice versa. This interpretation further suggests that if the Schottky diode forward voltage of the n-channel gate is smaller than that of p-channel one, then the power dissipation through the Schottky gates will be limited by the on-resistance of the p-channel MODFET. Figures 6.5(b) and 6.5(c) support this prediction.: ring oscillators with 60 μm width p-MODFETs consume approximately twice as much power as the ring oscillator with 30μm width p-MODFET.

Ring oscillator performance at cryogenic temperatures : The propagation delay improves dramatically when the circuits are cooled to cryogenic temperatures, as shown in Figures 6.6 and 6.7(a). The operational voltage region shifts slightly towards higher voltages due to the threshold voltage increase at low temperatures. The dramatic increase of the speed is due to the dramatic improvement of p-MODFETs at cryogenic temperatures. This result will be in clear contrast with the C-MODFET ring oscillator result using δ-doped channel p-MODFETs which is discussed in the next section. The δ-doped structures exhibit virtually no improvement at cryogenic temperatures.

(a)



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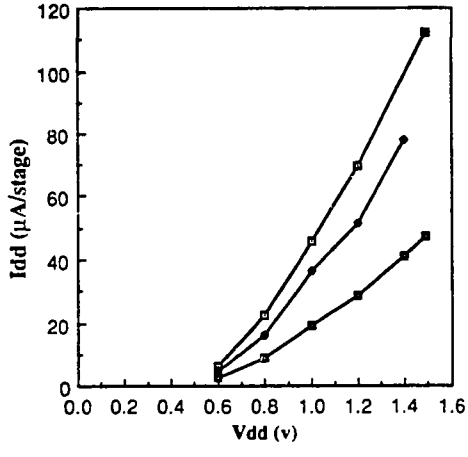

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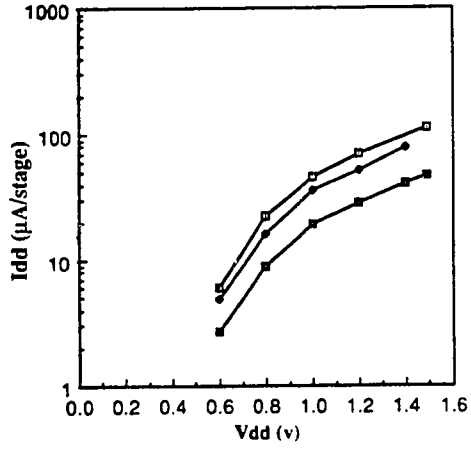


Figure 6.5 Seventeen stage ring oscillator results at room temperature for various inverter sizes. (a)Propagation delay (logarithmic scale) vs supply voltage,(b) current dissipation vs supply voltage and (c) current dissipation (logarithmic scale) vs supply voltage .

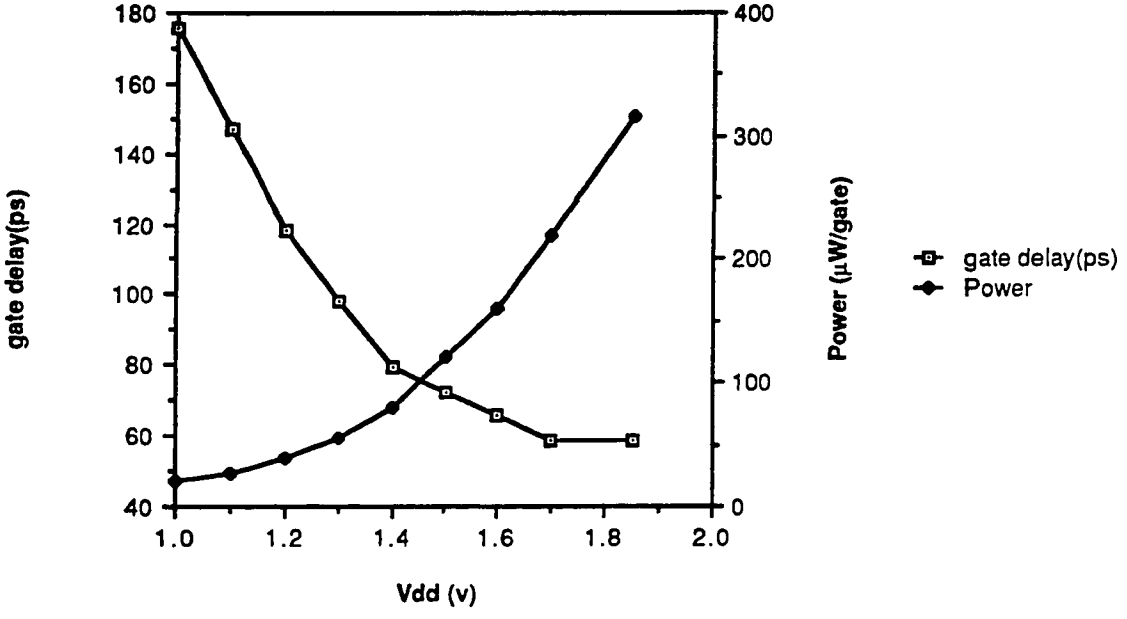
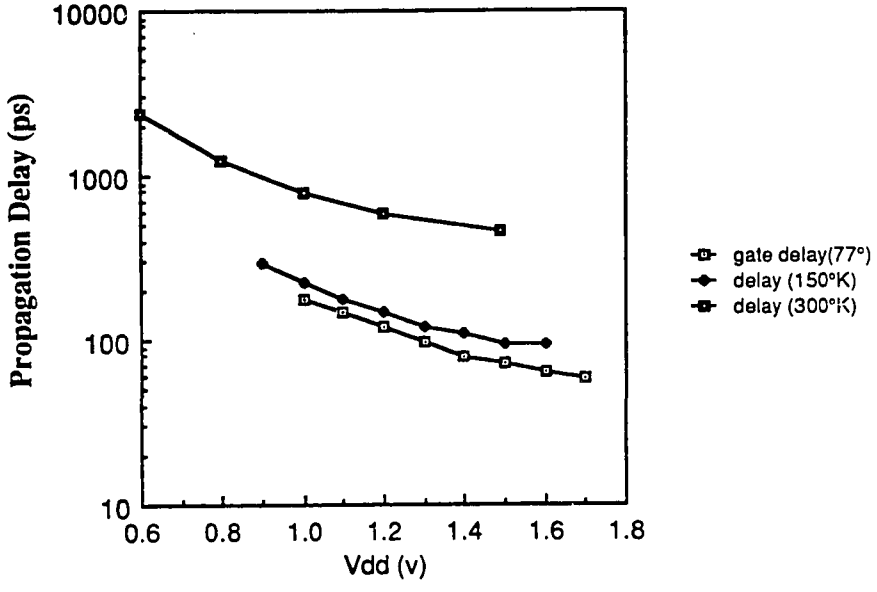
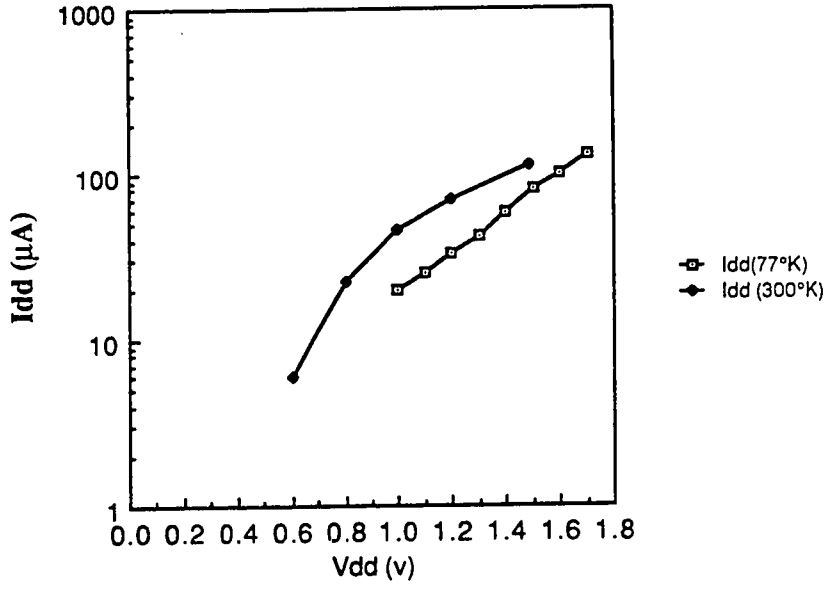


Figure 6.6 Propagation delay and current dissipation of a seventeen stage ring oscillator measured at 85°K.

Figure 6.7 shows the current dissipation dependence on power supply voltage in a semi-logarithmic plot. Room temperature results are plotted as a reference. It is remarkable that the power dissipation remains almost constant, even with the dramatic increase of circuit speed and oscillation frequency of the ring oscillator. This agrees well with CMOS results [HANAMURA 87] which will be discussed in section 6.6.



(a)



(b)

Figure 6.7 (a) Propagation delay and (b) current dissipation as a function of supply voltage for a seventeen stage ring oscillator measured at 85°K.

Comparison with other complementary heterostructure approaches : The propagation delay dependence on power dissipation of various complementary heterostructure FETs is shown in Figure 6.8. Our circuits demonstrated the best results for both propagation delay and power dissipation among the various complementary heterostructure FETs. One notices that the propagation delay time improvement is not dramatic between these various device structures, however, there is a significant difference in the power dissipation. One notices also the propagation delay dependence on W/L ratio between p-channel and n-channel FETs. The propagation delay of the Honeywell data [DANIELS 86] shows that the smaller the W/L ratio, the smaller the propagation delay. This result is consistent with the NTT result [MIZUTANI 86]. Our result may have been better if we had designed the W/L ratio to be one. The reason for not choosing the ratio of W/L to be unity was that our objective was not to break the ring oscillator speed record, but to evaluate a new technology in a real life configuration . In application to an integrated circuit, the circuit should drive a large load capacitance, including parasitics, associated with the wiring. Thus, a W/L ratio of 1 is too small to be used in a real integrated circuit. The compromised value of 2 or 3 increases the p-channel FET driveability. Regarding the superiority of power dissipation of the C-MODFET over other structures, the complementary MIS-like heterostructure [MIZUTANI 86] has been achieved by introducing the n^+ doped Ge gate on an n-channel heterostructure FET. The MISFET-like structure has inherently high threshold voltages, as discussed in section 3.2. Typical threshold voltages are 0.8 volt for n-channel FETs and -0.6 volt for p-channel FETs. The n^+ doped Ge gate thus solves only the n-channel FET problem. Thus, the imbalanced threshold voltages cause increased leakage current. The present C-MODFET approach, on the other hand, minimizes the gate leakage current factor by (i) adjustable threshold voltage, and (ii) improved gate leakage characteristics of a p-MODFET at cryogenic temperature, as we have seen in section 6.3.1. For the rigorous comparison between various complementary heterojunction FETs, all the power dissipation should have been normalized according to the number of stages of each ring oscillator. However, it turns out that the number of the stages used by various authors (13, 15, 17) are quite similar and the adjustments from this difference would be small and has been neglected.

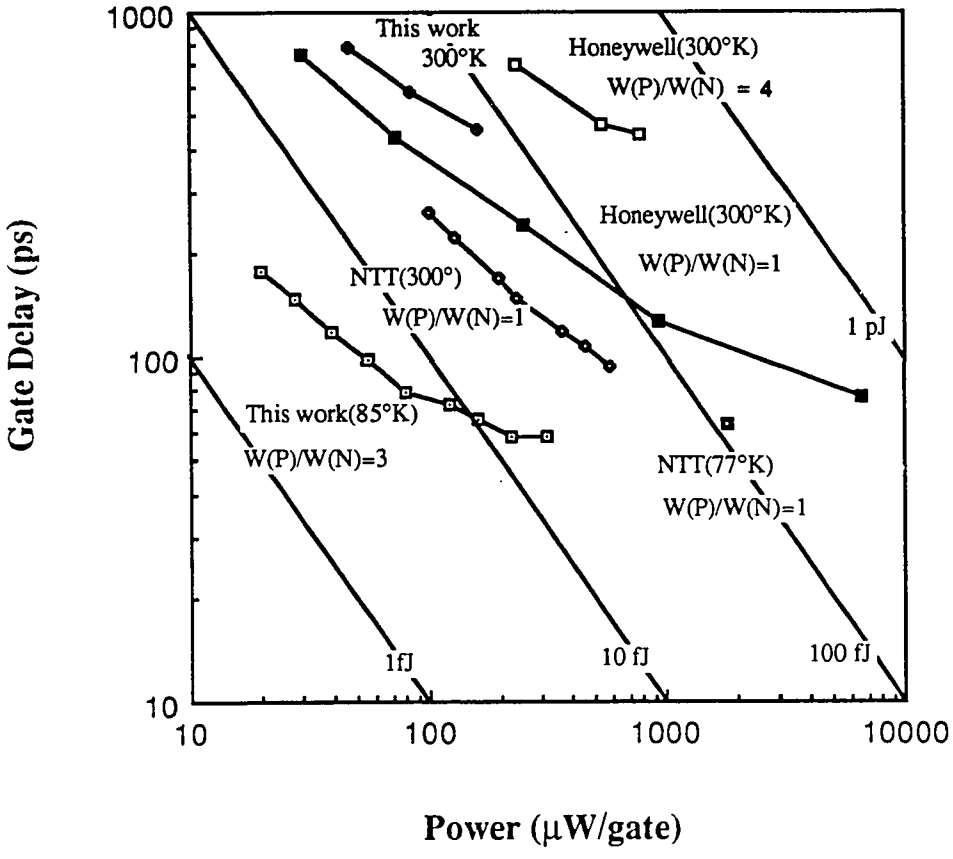


Figure 6.8 The propagation delay and power dissipation of various complementary heterojunction FET circuits.

6.4 C-MODFET circuit using δ-doped channel as a p-MODFET device

A complementary MODFET circuit has been fabricated using pseudomorphic n-MODFET and a δ-doped channel p-MODFET. Since the best room temperature p-MODFET performance was the δ-doped structure, we chose to examine this combination for room temperature C-MODFET circuits. The fabrication method was described in chapter 5. The current voltage characteristics of the p-MODFET and n-MODFET are

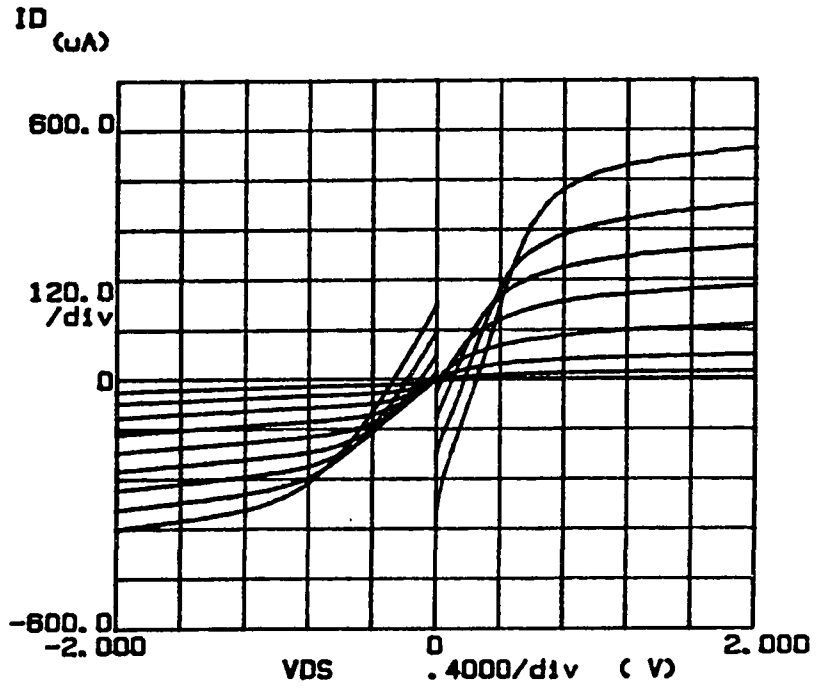


Figure 6.9 Current-voltage characteristics of a δ-doped channel p-MODFET and pseudomorphic n-MODFET integrated on a C-MODFET wafer. Gate voltages are taken up to 1.0v (+0.1v step) for n-MODFET and down to -1.3v(-0.1v step) for p-MODFET.

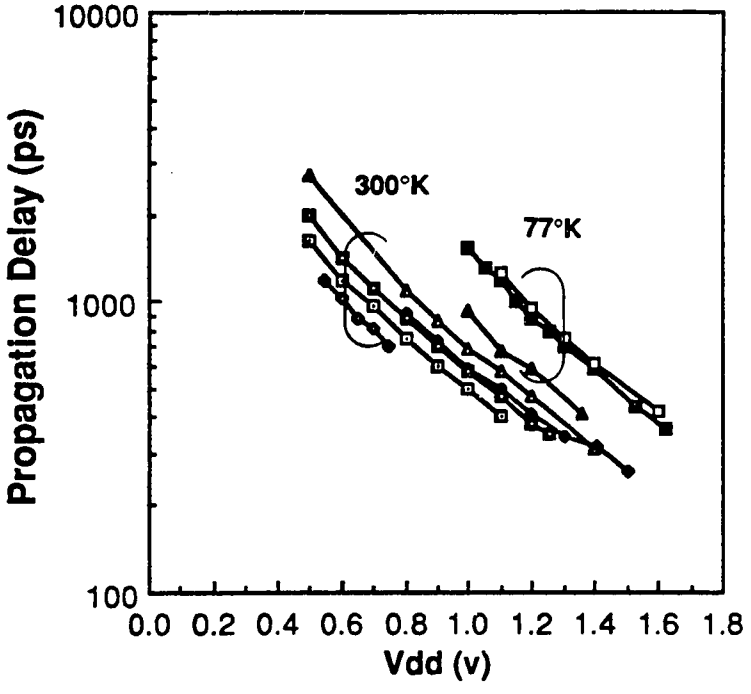


Figure 6.10 Propagation delay of a C-MODFET consisting of a pseudomorphic n-MODFET and a δ-doped channel p-MODFET as a function of power supply voltage.

shown in Figure 6.9 and the seventeen stage ring oscillator result is shown in Figure 6.10.

The propagation delay at room temperature for these circuits is significantly smaller than the values achieved with the new C-MODFET approach optimized for 77°K operation and described in the preceding sections. This result agrees well with the δ-doped channel p-MODFET performance discussed in chapter 5. The high speed demonstration at relatively low supply voltages at room temperature may indicate that this approach is a good candidate for high speed complementary heterostructure circuits at room temperature. The cryogenic temperature operation of these circuits showed no improvements in speed, however, the operation voltage shifts towards higher voltages with the same speed. This result again agrees well with the δ-doped channel p-MODFET performance discussed in chapter 5. The ionized impurity scattering dominates hole transport at cryogenic temperatures, thus preventing improvements of propagation delay at cryogenic temperatures.

6.5 COMPARISON WITH LOW TEMPERATURE CMOS

The improved performance of low temperature CMOS is approaching the high speed performance of GaAs digital integrated circuits [AOKI 87], however, the GaAs devices are still operating at room temperature. It is useful to compare the performance between Low Temperature CMOS (L-T CMOS) and complementary MODFETs because the C-MODFET has demonstrated the smallest speed-power product [YOH 87b]. With optimization of the adjustable threshold voltage and the small gate leakage current of the p-MODFET, these circuits are presumably close to the maximum intrinsic performance of complementary heterostructure FETs. Figure 6.11 shows the comparison of L-T CMOS and C-MODFET in propagation delay as a function of the power dissipation.

The superiority of C-MODFET over L-T CMOS in propagation delay by a factor of 2-3 has been confirmed. The physical reasons for this difference are related to the material differences of these devices. There are many material and structural differences in these two approaches, such as, dielectric constant of the gate insulator (≈12 of AlGaAs vs ≈4 of SiO_2), and interface roughness of AlGaAs/GaAs vs SiO_2/Si. However, assuming the same saturated electron (and hole) velocities between AlGaAs/GaAs and SiO_2/Si systems, C_0/g_m (or n_s/I_{ds}), the figure of merit of the circuit speed (neglecting interconnection capacitance for the moment), turn out to be the same, except for the field effect mobility term. Interface roughness scattering appears to cause a significant reduction of the field effect mobility in the SiO_2/Si case, especially when the vertical

electric field is high. One of the advantages of C-MODFETs over CMOS for 77°K operation is that the threshold voltages of C-MODFETs are more accurately controlled by modulation doping, in spite of the relatively deep (≈30meV) acceptor level. Because of the superior V_{th} control, lower values of both V_{th}, and supply voltage, V_{dd}, can be used for MODFET circuits. The higher threshold voltages of CMOS result in higher vertical electric fields which reduce the low field carrier mobility. The higher V_{th} also lowers the drain currents by a factor of $(V_{dd} - V_{th})^2$ for the same value of V_{dd}. In addition to interface roughness scattering, ionized impurity scattering in the channel of CMOS may also be contributing to lower the field effect mobility. Another factor for comparison is the subthreshold current. Because the substrate is undoped in MODFETs, the standby

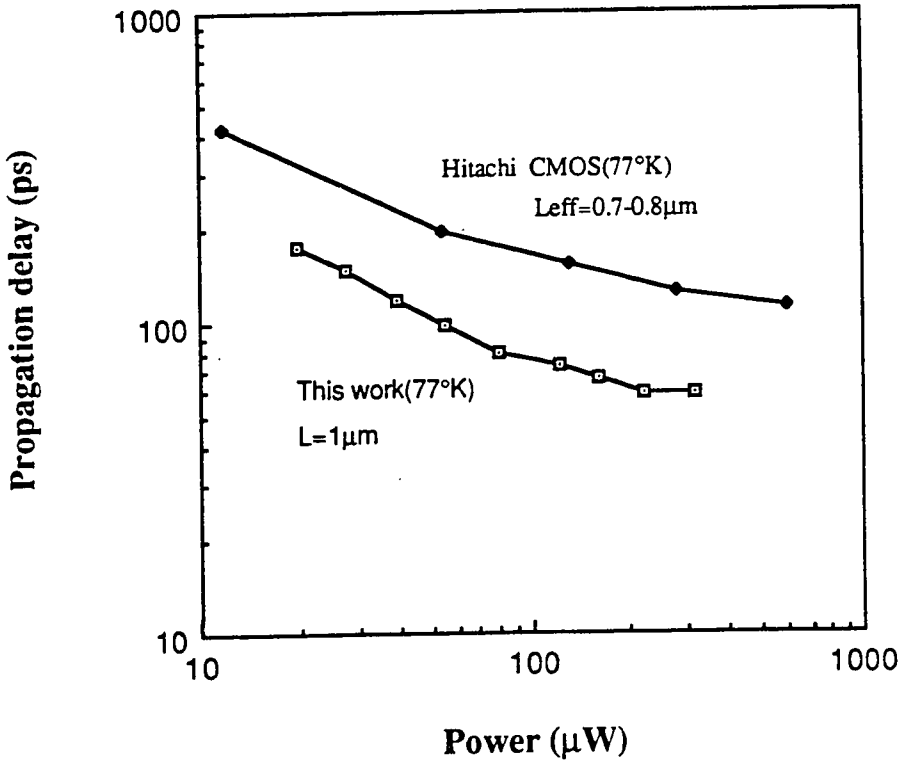


Figure 6.11 A comparison of propagation delay vs power dissipation for Low Temperature CMOS and C-MODFETs.

current is of the order of 10^{-8} A/gate due to space-charge-limited current [SCHOCKLEY 53]. Because of the insulator in CMOS, the standby leakage current is as small as 10^{-14} A/gate. This high leakage current of C-MODFETs precludes the use of line memories in IC design and hence limits application of simplified dynamic circuits based upon of transmission gates. However, this limitation does not preclude the use of C-MODFET circuits. High speed application of C-MODFETs with the design constraints of static only circuits is still attractive. If the design feature sizes are equal, the integration level of C-MODFETs will still be lower than CMOS (perhaps by a factor of ≈ 2 at most) because static circuits require greater area. Thus circuit density appears to provide the fundamental limit for integration level rather than power dissipation.

6.6 SUMMARY

Experimental results of improved C-MODFET structures have been shown. The fastest complementary FET circuit at 77°K has been demonstrated. The power-delay product of this circuit is the smallest ever reported of all semiconductor devices (as of December 1987). Comparison with Low-Temperature CMOS shows a factor of 2-3 superiority of C-MODFET in speed for the same power consumption at 77°K. An alternative approach, using a delta-doped channel p-MODFET was demonstrated and seems to be more suitable for room temperature application.

Chapter 7

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

7.1 CONCLUSIONS

- SPICE simulation showed that the C-MODFET is a potentially high speed and low-power circuit with high noise margins. It makes low voltage operation realistic.

- SPICE simulations also predict that C-MODFET circuit speed could exceed E/D type MODFET (HEMT) circuits if the Schottky barrier heights (for both electrons and holes) could be increased to greater than 1.5eV. This increase in barrier heights is both the greatest technological challenge and the one with the greatest performance benefit.

- Various new p-MODFET structures, such as; double heterojunction p-MODFET, strained single quantum well p-MODFET, and delta-doped channel p-MODFET were investigated. The double heterojunction p-MODFET exhibited the highest drain current and transconductance at cryogenic temperature operations, while the delta-doped channel p-MODFET showed the best transconductance at room temperature.

-Selective, multiple MBEgrowth technique were developed and C-MODFET circuits were successfully fabricated and demonstrated which exhibited the following:
(i) sharp inverter transition characteristics and noise immunity of 94%, and
(ii) the fastest propagation delay among all complementary FET circuits and the lowest power-delay product of any IC technology todate.

-Circuit speed and power of C-MODFET circuits were compared with that of Low-Temperature CMOS and showed a superiority of a factor of 2-3x over CMOS. Modulation doping was crucial to adjust threshold voltages at cryogenic temperatures to realize this performance advantage. The ideal AlGaAs/GaAs heterojunction interface was also helpful to minimize interface roughness scattering and improve the carrier mobilities.

7.2 SUGGESTIONS FOR FUTURE WORK

As demonstrated by the SPICE simulation, the enhancement of the Schottky barrier height is the key point to be overcome. Another suggestion from the power-delay comparison between C-MODFET and CMOS at 77°K is the use of a good interface between barrier and channel layers lattice matched or unmatched(comensurate) in new material systems.

7.2.1 Structural Improvements For Higher Schottky Barrier Height

- Utilize camel diode type of barrier height enhancement[SHANON 76]. This approach requires very heavy doping in thin layers. Threshold voltage control and suppression of intermixing/interdiffusion must be solved.

- Optimize double heterojunction structures for both p- and n-channel devices with either MODFET or MISFET approach. Threshold voltage control[Chapter 5] and good ohmic contact [KINOSHITA 84] are the two key technological problems.

- Utilize a thin oxide layer as the gate barrier material (AlGaAs). The oxide must be thin enough for the Fermi level of the gate metal to be pinned directly to the AlGaAs surface layer, but thick enough to suppress gate leakage current.

- Utilize a dielectric film rather than AlGaAs as a high barrier material. This material must leave the surface "unpinned" in any method, which means interface state less than 10^{11} cm^{-2}. Reduction of the interface states has been the main issue for this approach. More attention must also be paid to seek a material with a high dielectric constant because interface roughness will limit the field-effect mobility under high vertical electric fields unless a better dielectric is found.

- Investigate the AlInAs/InGaAs system lattice matched to InP. The key question which must be resolved for this system is whether or not a high barrier height for holes is possible.

7.2.2 New(Old?) Materials For Higher Carrier Mobility

- Utilize a Germanium MOSFET. High mobilitiy of both electrons and holes makes Ge very attractive to use for complementary circuits. Formation of a stable oxide [CRISMAN 87] has been the main issue since the 1950's. A heterojunction approach may solve the problem.

- Investigate SiGe/Ge heterojunction FET using pure Ge as a channel layer. Selective etching of the SiGe over Ge and relatively low Schottky barrier height are likely the major concerns.

7.2.3 New Combination of Devices to Compensate low current capability of p-channel HFETs.

- Monolithically integrate E/D and complementary circuits. By using E/D circuits at the output stage of each unit logic block, it is possible to minimize major propagation delays at nodes of heavy capacitive loads while still maintaining the high noise margins possible with complementary circuits.

- Monolithically integrate n-channel FETs and a negative resistance load, such as a resonant tunneling device [LEAR 88].

7.2.4 Device Scale-Down

- Straight scale-down of the devices will continue to improve p-channel FETs because the hole velocity in the channel is still not saturated at 1μm gate lengths. Again, the difference between GaAs heterojunction C-FET and CMOS will be the field-effect mobility or effective channel mobility difference. One of the advantages of C-HFETs over CMOS at 77°K operation in the short channel extreme is that the thresholds of the C-HFET's are adjustable, by modulation-doping.

APPENDIX A

Noise Margin of Integrated FET Circuits

The definition of noise margins in logic circuits by "Mirror-and-Maximum-Square method" [HILL 68] is the worst case static series-voltage noise margin which can be found graphically as shown in Figure A1. This definition is over cautious in two senses. One is that it assumes that a noise signal of opposite polarity occurs at every node of the series of identical inverters, which is extremely unlikely to happen. Secondly, the noise is assumed to be static, which always causes the poorest result compared with dynamic noise, which is most likely to occur through capacitive coupling in an integrated circuit. The alternative definition is noise immunity, which was defined in chapter 2: the voltage distance from a latch level to the nearest unity gain point of an inverter transfer curve. This definition makes more sense in a way, in that it assumes a one-shot noise at the output node of a latch because the signal level of the second stage should be pretty much recovered from the first noise. This method is applicable to our E/D and complementary GaAs circuits as long as the operational voltages are kept in the range where the gate leakage current is not severe. In order to simulate noise margins into the high gate leakage region, one could use the flip-flop method[LOHSTROH 79] which is applicable to the low impedance gate system.

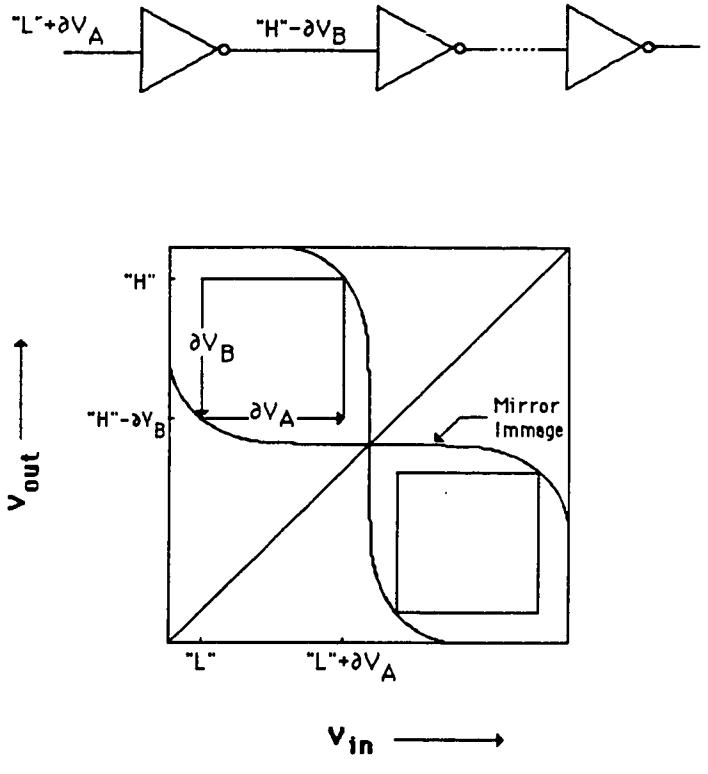


Figure A.1 Noise Margin Definition of " Mirror-and-Maximum-Square"

APPENDIX B

Power Dissipation of Complementary FET Circuitry

B.1 Power Dissipation of a Complementary FET inverter.

Power dissipation of a complementary FET circuit consists of the following two components:

$$P_1 = C_L V^2 f , \qquad (B.1)$$

$$P_2 = I_{mean} V , \qquad (B.2)$$

where C_L is the is the load capacitance and V_{dd} ,the supply voltage, I_{mean} , the mean value of short circuit current, and f, the operating frequency. The first component is the dynamic dissipation, and the second component is the short circuit dissipation. The short circuit component (B.2) is approximated as [VEENDRICK 84],

$$P_2 = \frac{ß}{12}(V_{dd} - 2V_{th})^3 \frac{\tau}{T} , \qquad (B.3)$$

where ß denotes a gain factor($\mu A/V^2$), V_{th} , the threshold voltage, τ, the average rise and fall time of the signal, and T the period-time of a signal (=1/f). If we approximate τ as

$$\frac{C_L V_{dd}}{ß (V_{dd} - V_{th})^2} \approx \frac{C_L}{ß} \frac{A}{V_{dd} - 2V_{th}},$$

where

$$A = \frac{V_{dd}(V_{dd} - 2V_{th})}{(V_{dd} - V_{th})^2} \approx 1 \quad \text{when } V_{dd} >> V_{th.}$$

Then equation (B.2) can be rewritten as,

$$P_2 \approx \frac{C_L}{12}(V_{dd} - 2V_{th})^2 f \qquad (B.4)$$

Thus, the total power can be approximated by

$$P = P_1 + P_2 \approx C_L V^2 f (1 + \frac{1}{12}).$$

P_2 is now shown to be of the order of 10% or less in the case of a chain of inverters with identical capacitive loads at each node.

B.2 Power Dissipation of Complementary FET Logic.

Power dissipation of a complementary FET circuit is not a multiple of total power dissipation of the previous result, but a weighted average of each component by the effective frequency of logic state transition. Two example calculations are shown below.

Example 1. 8 K Gate CMOS Gate Array (Toshiba), ISSCC '85, p260

$f_{eff} = P_d / C_L V^2 = 2.18$ MHz $= 0.174\ f_{CLK}$,

where the following parameters are used. $P_d = 300$mW was measured at 12.5 MHz clock frequency. Average load capacitance, C_L, was calculated as

$C_L = 3\ C_{in} + 2\ C_W = 917$ fF,

where C_{in} is the average gate input capacitance calculated as

$C_L = 2\ C_0\ (A_n + A_p)$,

$C_L = 115$ fF/mm,

using the following gate area and gate capacitance:

$A_n = 1.8\mu m \times 39.3\mu m$,

$A_p = 1.9\mu m \times 39.3\mu m$

$C_0 = 7.87 \times 10^{-8}$ F/cm^2.

The average interconnect metal length is assumed to be 2mm.

Example 2. 8X8 Multiplier , ISSCC '85, Transaction Electron Devices vol.ED-34, p94, 1984.

The circuit consists of 64 Full-Adder/Half-Adders (consisting of 11 gates) and 31 buffers.

$f_{eff} = P_d / C_L V^2 = 1.85$ MHz $= 0.185\ f_{CLK}$,

where power dissipation was 5.05 mW measured at 5v and 10 MHz. The total capacitive load, C_L, is calculated as follows:

$C_L = 11 \times 64 \times C_g + 31 \times C_g \times 3 = 797\, C_g = 109$ pF,

(F.A./H.A.) (Buffers)

where gate capacitance per gate (equivalent of two nands), C_g, was calculated using

$C_g = 4\, A_g \times C_0$,

$C_0 = 1.771 \times 10^{-7}$ F/cm^2,

$A_g = 1.3\mu m \times 15\ \mu m$.

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